

Research Article

Design MIMO Switch Architecture Based IEC 61850 Standard of Substation Automation Systems

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Abstract: Recently, there has been a tremendous change in the development of many protocols in electrical substation automation such as robust communication among control centers (GOOSE). It is a challenge to implement critical time operation such as tripping based on GOOSE protocol when the protocol is not tested in a wide area multi-substations environment. Another reason is the function of the packet forwarder may fail under a very high traffic condition with the constant generation of GOOSE packets due to multiple events. This study investigates the performance of packet forwarder in terms of packet loss under different models configurations. The investigations carried out on various switch configurations and architectures to reduce the number of dropped packets. The results showed that the architecture of two-switch system is the best performance in which the packet loss can be reduced by 2.9% in comparison with two buffer switches and 11.8% in comparison with the to original standard.

Keywords: Drop packet, GOOSE, IEC 61850, queue, smart grids, standards, substation automation system

INTRODUCTION

Technology development has undergone tremendous changes in recent times. The enormous changes in various areas often makes one wonders what new innovations are in store for future developments (Nordin *et al.*, 1992). The changes has resulted in the development of many protocols in electrical substation automation. These protocols are used for the provision of faster and more robust communication among control centers (SCADA Masters), Remote Terminal Units (RTUs) and Intelligent Electronic Devices (IEDs). Therefore, it is necessary to set up a standard for sub-station automation. The particular standard that meets the requirement is IEC61850 (Adamiak *et al.*, 2000).

IEC 61850 is used mainly for substation and feeder automation (and if properly extended, it can be used in many other domains). Due to its applications many believe that the use of IEC 61850 is only limited in the substation and not as a protocol among the substations and control centers (Wester and Adamiak, 2012). However, the availability of new high bandwidth communication mediums which is a result of the advances in technologies, IEC61850 has extended its function to become an inter-substations protocol. In fact, IEC 61850 is an innovative approach that requires new ideas on how to automate substations (Wester and

Adamiak, 2012). As expected, this object oriented approach requires higher bandwidth, but with significant cost savings due to reliability (repeatability) and scalability of applications this approach is worth the investment. Nowadays the trend is for additional object models that can bring benefits to the industries when these models are realized by vendors. Examples of industrial that engage in object oriented approach are the water industry, as well as the oil and gas industries. Therefore, IEC 61850 is not just a communication protocol, but it is also a comprehensive standard for the design of automation systems (although currently the standard is more specific for substation automation). It adds format and structure to data which was traditionally unformatted. It is also a collection of multiple protocols and concepts that can facilitate design, implementation and operation of these systems (IEC, 2003-04).

The primary objective of IEC 61850 is to introduce control intelligence in the network for the purpose of managing the remote devices and to operate on protocols of top standard communication. If IEC 61850 is used correctly, it will simplify the engineering and integration of the system and device (data). Also, it will reuse the interoperability of models with different vendors system (Kuffel *et al.*, 2010). Thus, with IEC 61850, it is crucial to abide by the design rule that requires proper modeling and consistent configuration of the system, together with application of objects, with

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an exchange of I/O and Meta data. If these guidelines are used, the true value of IEC 61850 can be realized in terms of ease in implementation, expansion and scalability (IEC, 2003-04; Kuffel *et al.*, 2010).

In this study, three studies were conducted to determine the performance of switches with different architectures. All three studies were carried out based on the traffic of 2000 packets/sec. This is in compliance with the GOOSE requirement of 4 msec inter-packets time. The other simulation parameters are service time of 20 msec and the buffer of 2 Mbits. All the parameters abide the regulations for a standard industrial switch. The results obtained from testing the implementation of the proposed switch in handling GOOSE protocol followed by an analysis of the finding. The results comprise the performance of various proposed switch architectures.

MATERIALS AND METHODS

GOOSE protocol: GOOSE is an acronym for Generic Object Oriented Substation Event. It supports the exchange of a wide range of possible common data that is organized by a DATA-SET such as in synchronized circuit breaker switching, distance protection and over current protection (Ali and Thomas, 2011; Sidhu *et al.*, 2011). As the operation of the electrical substation automation is time critical, there is a demand for high reliability and availability of the Substation Communication Network (SCN) (Montignies *et al.*, 2011). These requirements can be fulfilled by IEC 61850 standard as it is able to send off fast response data via the Generic Substation Events (GSE) for a peer-to-peer communication mode by GOOSE protocol. Also the data for GOOSE is embedded directly in Ethernet data packets that works on publisher-subscriber mechanism with multicast or broadcast MAC addresses (Nguyen-Dinh *et al.*, 2007).

In fact, GOOSE has been designed to operate in a fast and reliable manner over the substation process bus. Meanwhile, KEMA a global energy consulting company with its headquarters stationed in Arnhem, Netherlands conducted tests on IEC61850 devices from

different vendors. The findings indicated that reliable tripping of breakers were accomplished using the GOOSE messages. All these devices fulfill the 4 ms from fault to the trip operation as required by IEC61850 protocol. Thus, maintaining the integrity of the specifications (Apostolov, 2004; Nguyen-Dinh *et al.*, 2007).

Switch architecture: The function of a switch is to receive arriving packets at its input ports and forward them to its output ports. As long as only one packet arrives at a given time interval, there will be no collision and the packets are forwarded with minimum latency. Unfortunately, as the traffic (events) increases, so does the probability of collision. When two packets destined for the same output port arrive at different input ports of a switch at approximately the same time, both cannot be forwarded immediately. Only one packet can be transmitted at a time from an output port, hence one of the two packets must be stored at the buffer for later transmission. The maximum rate at which a switch can operate depends directly on the efficiency of the switch in storing and resolving the collision between packets. In all switch architectures the parameters of the design are chosen as follows: processor service time 20 msec (Kalyanaraman *et al.*, 2000), buffer capacity 164 packets/sec (RuggedSwitch, 2014), inter-arrival time between packets of 4 msec (Wester and Adamiak, 2012).

Design of a switch architecture: The input for the architectural design is represented by a group of signal generators which work to produce signals for the whole system. In this design, any signals or messages that are derived from the input are assumed as events. All the events from the generators are combined into one path by a path combiner block. Consequently, there is only one path or stream of events to the next subsequent processing functional blocks. The events in the path combiner are processed by a processor (CPU), after which they are forwarded to output ports. In this proposed model, there are two main simulation parameters, namely delay at functional block and

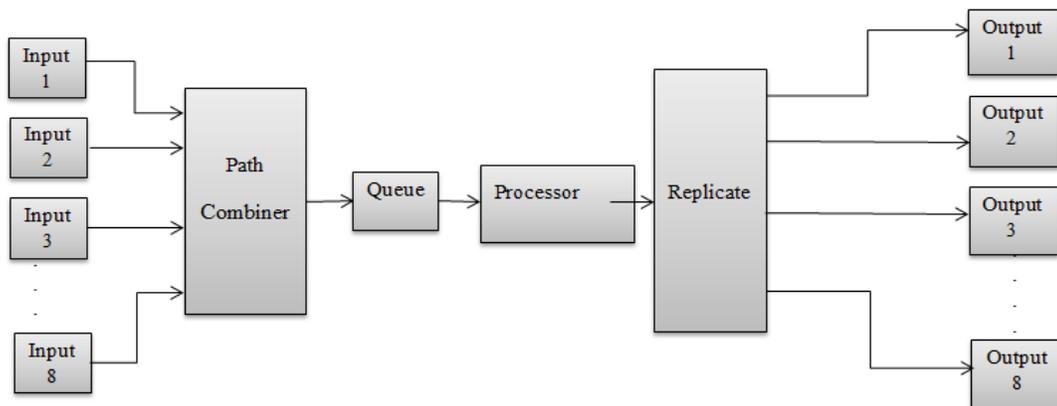


Fig. 1: Block of MIMO switch architecture

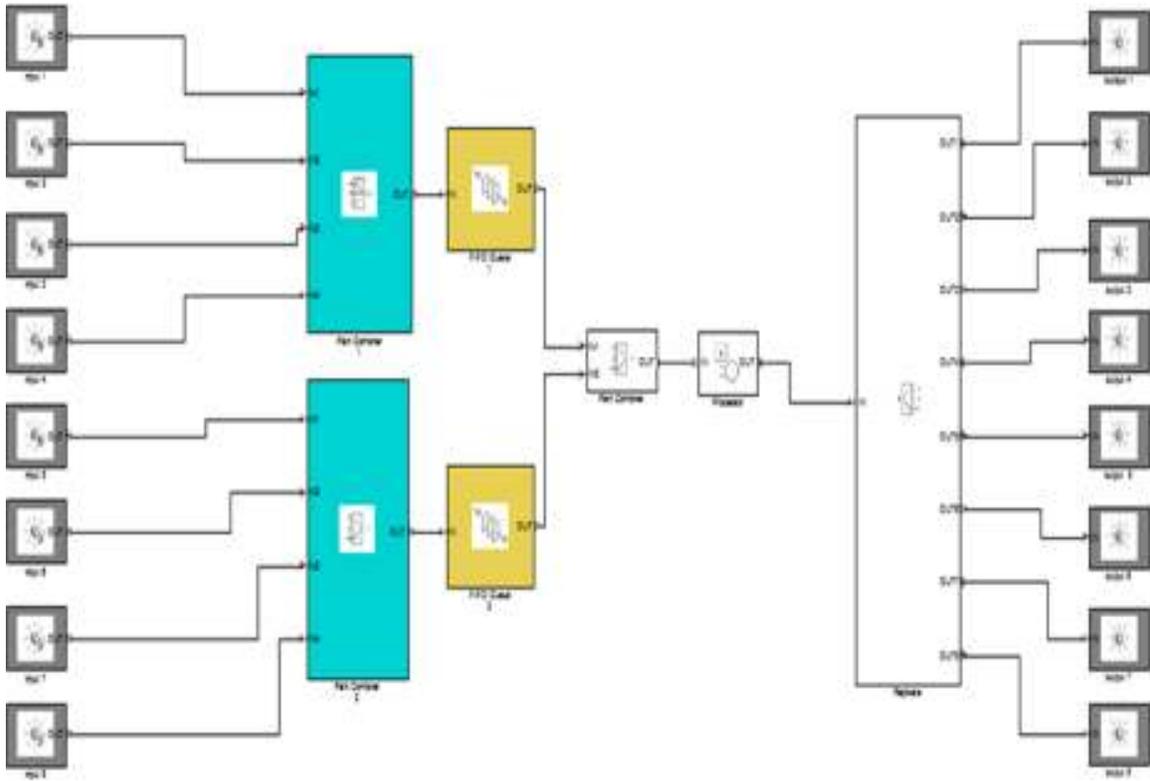


Fig. 2: Two buffers queue

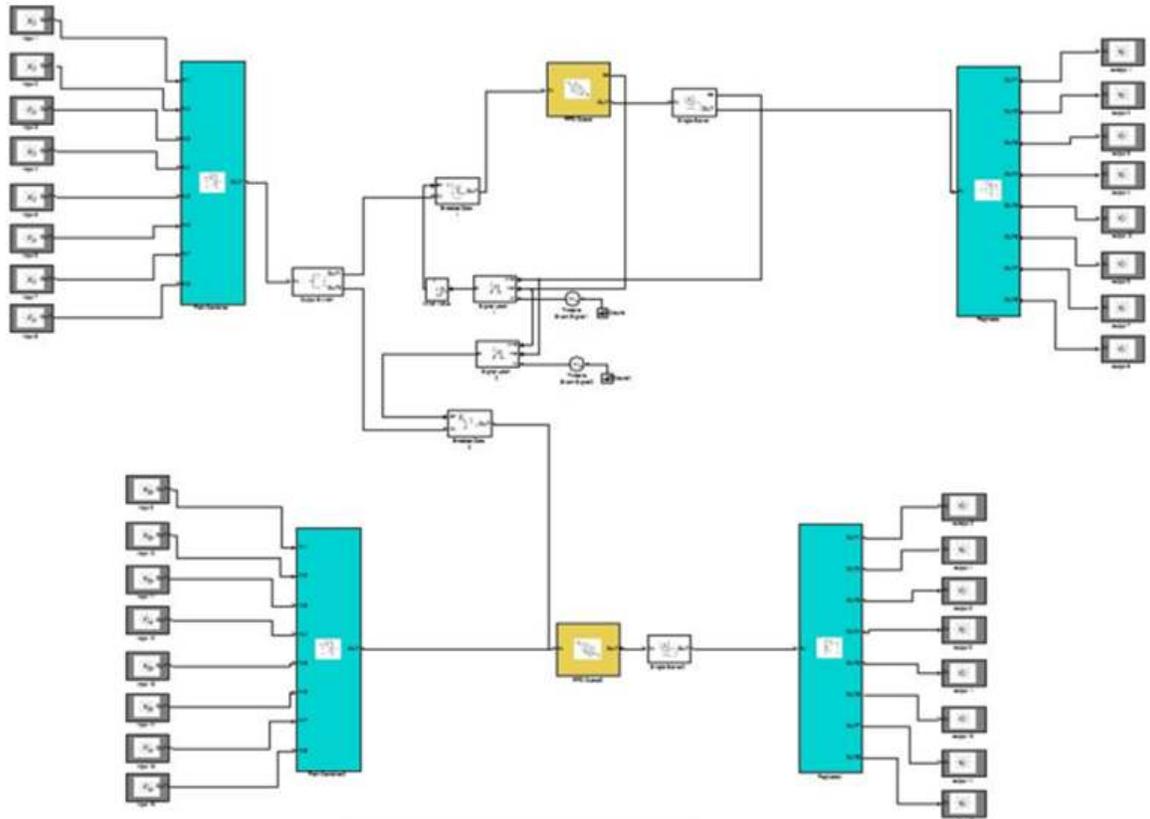


Fig. 3: Connections of double switches and controller in SIMEVENTS

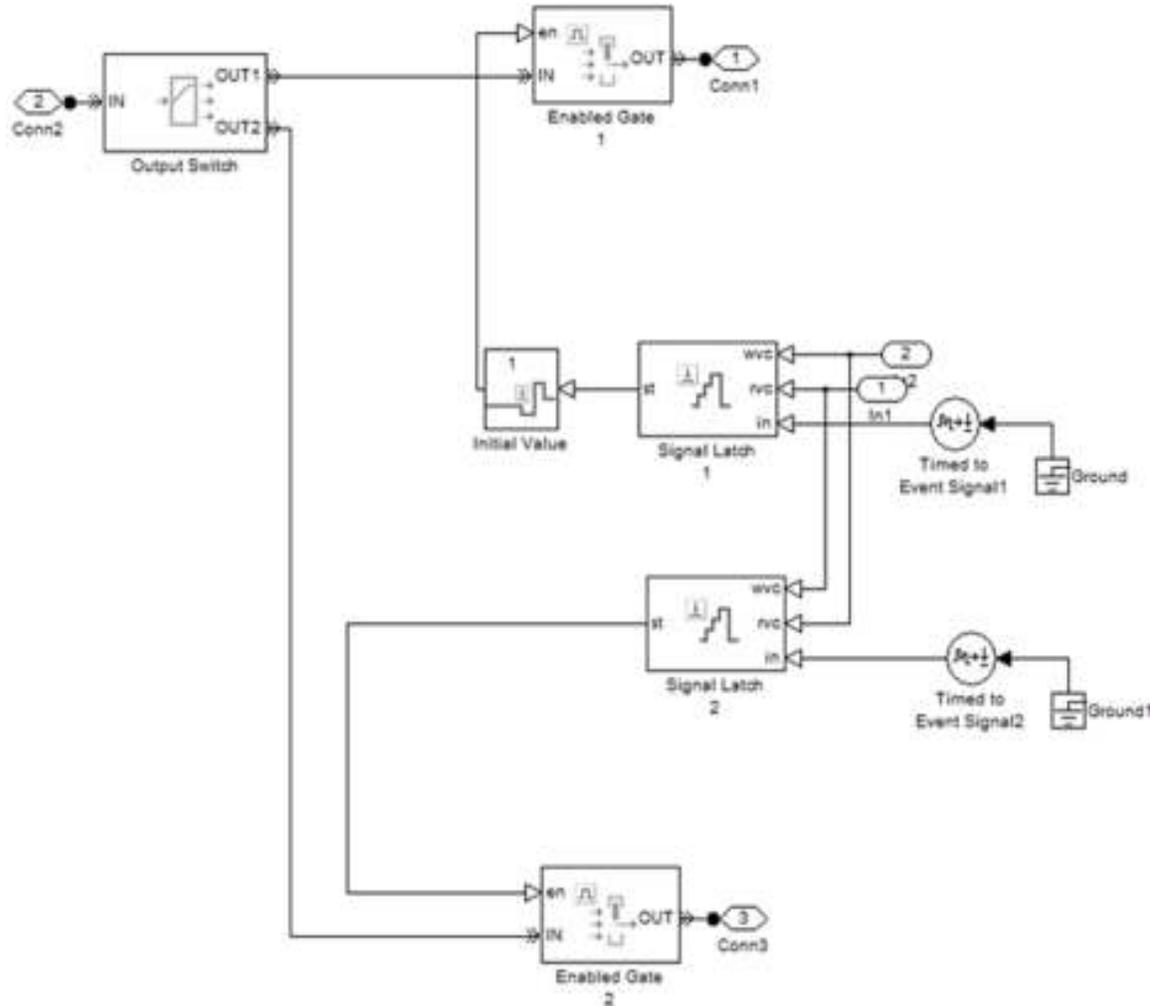


Fig. 4: Internal controller block design implemented in SIMEVENTS

the number of events from each input node. The question that arises at this stage is what would happen if the events arrive during the time interval when the CPU is processing other events? The other question is what would happen to these events if the processor input is blocked? The answer is these events would simply be dropped. If the number of packet drop accumulates, the reliability of this system is compromised. To avoid this problem a queuing block of finite size is introduced between the path combiner and CPU. Physically, it is a memory block to buffer GOOSE packets while waiting for the CPU to free and ready to receive the packets. The starting point of the queuing size in the model is based on an industry switches i.e. RUGGEDCOM switch in this case (RuggedSwitch, 2014). How long do the events (packets) wait inside the queue depends on the speed of the processor speed. The proposed architecture of the switch is depicted in Fig. 1.

Queuing with two buffers: The study of two buffers switch is included as switch performance shows improvement with a larger amount of buffer. Additional

buffer means the provision of more free space to hold events while waiting for processing by CPU. This scheme reduces the chances of the occurrence of drop packets. Figure 2 shows the switch design of a queue with two buffers.

Two switches mechanism: The two switch mechanism is proposed as it is now an improved system. These two switches are connected to the same network as a single system. This mechanism helps in balancing the traffic load and at the same time increases the reliability of the network. For the implementation of this system a controller and an inter-switch interface are employed for the distribution of events between switches. Figure 3 illustrates the representations of the two switch block. Figure 4 shows the implementation of the controller block.

RESULTS AND DISCUSSION

The testing of the design packet forwarding system, especially the switch design in IEC61850

Table 1: Simulation parameters for one buffer switch architecture

Inter-events time in msec	Buffer capacity	Service time of processor in msec
4	164	20

Table 2: Ratio of drop packets in single buffer

Inter-events time	Number of generated packets from 8 ports	Number of drop packets	Drop packets (%)
200 msec	400	236	59.00
400 msec	800	636	79.00
600 msec	1200	1036	86.30
800 msec	1600	1436	89.75
1 sec	2000	1786	89.30

Table 3: Two buffers with capacity 164 packets

Inter-events time in msec	Buffer capacity	Service time of processor in msec
4	2×164	20

Table 4: Ratio of drop packets in two buffers

Inter-events time	Number of generated packets from 8 ports	Number of drop packets	Drop packets (%)
200 msec	400	72	18.00
400 msec	800	472	59.00
600 msec	1200	872	72.66
800 msec	1600	1272	79.50
1 sec	2000	1622	81.10

Table 5: Comparison ratio of packet loss between one buffer capacity and two buffers capacity

Inter-events time	One buffer (%)	Two buffers (%)	Reduction (%)
200 msec	59.00	18.00	41.00
400 msec	79.00	59.00	20.00
600 msec	86.30	72.66	13.64
800 msec	89.75	79.50	10.25
1 sec	89.30	81.10	8.20

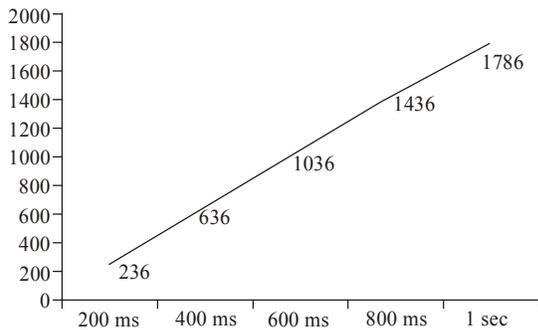


Fig. 5: Number of drop packet using single buffer switch

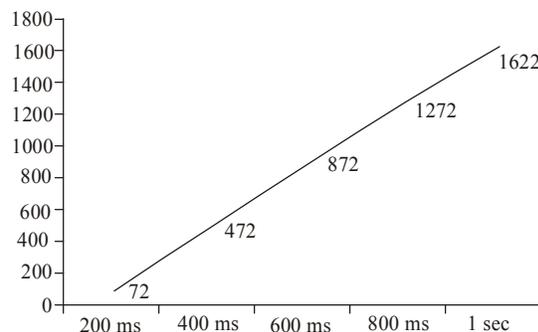


Fig. 6: Number of drop packet using two buffers switch

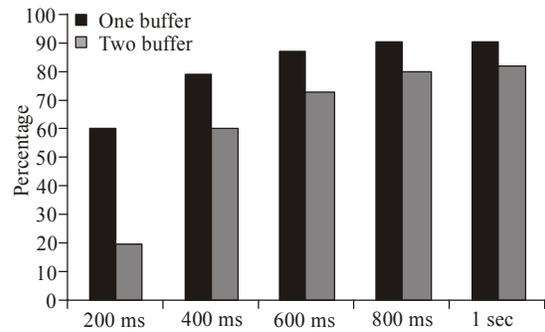


Fig. 7: Drop packets comparison ratio between one buffer and two buffers

substation automation environment. The main consideration is the performances of GOOSE packets in terms of packet loss. The arrival of GOOSE packets are modeled as events that are produced from a collection of generators. These generators and subsequent processing functionalities are designed, modeled and implemented using MATLAB/SIMEVENTS.

One buffer witch architecture: In this simulation, the switch architecture is based on an industrial switch manufactured by RuggedCom (Table 1). The buffer size of this switch is 2 Mbits, in terms of packet, the calculation is as follows:

$$2 \text{ Mbit} = 2 * 10^6 / (1518 * 8) = 164 \text{ packets} \quad (1)$$

The service time of 20 msec was used for this simulation as a worst case scenario. Figure 5 shows that the number of drop packets increases linearly with time. Table 2 shows that the capability to forward the packets collapsed after 400 msec (80%) of the traffic.

Two buffers switch architecture: The two buffers switch is more complicated study. Both have identical buffer size of 164 packet capacity. Testing is carried out to determine the characteristic of drop packet. The parameters for simulation are shown in Table 3 and Fig. 6 shows the number of dropped packets by using two-buffer switch.

Table 4 shows that the ratio of two buffers switch of drop packets has reduced significantly in comparison to the number of drop packets tabulated in Table 5 and Fig. 7. The reduction of packet drop ranges from 41 to 8.2%. However, the switch system will collapse if the time duration exceeds 1 sec.

Integrated two-switch architecture: This section studies the architecture of a complex and integrated two-switch system. This two-switch system involves the mechanism of distributing the network load and helps to provide an alternative route for the incoming packets from the input source. The simulation

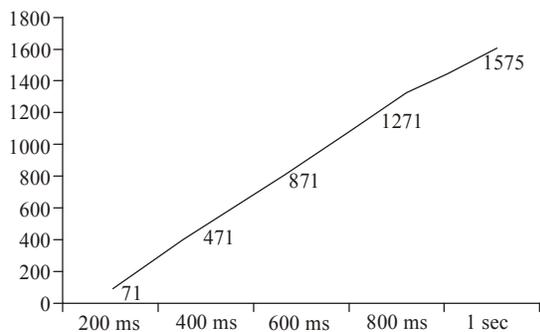


Fig. 8: Number of drop packets versus simulation time for two-switch architecture system

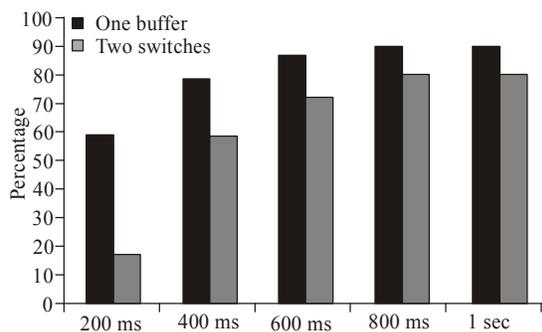


Fig. 9: Drop packets comparison ratio between one buffer and two switches

Table 6: Two switches parameters

Inter-events time in msec	Buffer capacity	Service time of processor in msec
4	164	20

Table 7: Percentage of drop packets in two switches

Inter-events time	Number of generated packets from 8 ports	Number of drop packets	Drop packets (%)
200 msec	400	71	17.7500
400 msec	800	471	58.8750
600 msec	1200	871	72.5800
800 msec	1600	1271	79.4375
1 sec	2000	1575	78.7500

Table 8: Comparison number of drop packets between one buffer, two buffers and two-switch architectures

Inter-events time	One buffer	Two buffers	Two switches
200 msec	236	72	71
400 msec	636	472	471
600 msec	1036	872	871
800 msec	1436	1272	1271
1 sec	1786	1622	1575

Table 9: Comparison ratio of packet loss between one buffer capacity and two switches

Inter-events time	One buffer (%)	Two switches (%)	Reduction (%)
200 msec	59.00	17.7500	41.2500
400 msec	79.00	58.8750	20.1250
600 msec	86.30	72.5800	13.7200
800 msec	89.75	79.4375	10.3125
1 sec	89.30	78.7500	10.5500

parameters are the same as in the previous two cases. Table 6 shows the simulation parameters for the two-

switch architecture system, while Table 7 tabulates the percentage of drop packets in a two-switch system. Figure 8 and Table 8 shows a comparison on the number of drop packet based on standard switch, two buffers and two-switch architectures. Figure 9 and Table 9 show that the use of more complicated architectures reduces the number of drop packets up to 41.3%.

CONCLUSION

This research is a study of the issues and performance of a of packet forwarder in term of packet loss in the substation automation communication network. The loss occurs because the switch is unable to cope with the high volume of incoming traffic. In the substation automation communication network, data delivery is very crucial for proper functioning of the system. Consequently, high speed Ethernet network based on high performance switches is required to ensure optimum operation. Only such a high quality network can fulfill the requirements of IEC61850 GOOSE requirement of below 4 msec delay for any operation. Investigations were also carried out on various switch configurations and architectures to reduce the number of drop packets. The investigation was implemented on two-switch architecture. Both the switches have the same characteristics, based on the specifications of RUGGEDCOM RS940G Switch. These switches are integrated using a controller the capability to distribute the load among them. All the proposed architectures were implemented by MATLAB SimEvent blocks and subsequently all the simulations were carried out on this platform. In conclusion, all the objectives of this research had been successfully achieved. In terms of architecture, the two-switch system showed the best performance. The analysis and investigation show that the packet loss can be reduced by 2.9% in comparison with two buffer switches and 11.8% in comparison with the original standard.

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