

Research Article

Design and Implementation of High Speed and Low Power Modified Square Root Carry Select Adder (MSQRTCSLA)

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Abstract: Multiplication and Accumulation (MAC) unit is recognized as high potential in every Digital Signal Processor (DSP). In MAC unit, both Multiplication and Accumulation functions are involved, but the performances of MAC unit is mostly depends on dataflow structure of Accumulation unit. In this study, Modified Square Root Carry Select Adder (MSQRTCSLA) is designed through Very Large Scale Integration (VLSI) System design environment. In the proposed design, Half Adder (HA) and Full Adder (FA) circuits are realized and identified the redundant logic functions. Hence, a new half adder named “Reduced Half Adder (RHA)” and a new full adder named “Reduced Full Adder (RFA)” are proposed in this study. Further the design of RHA and RFA is integrated into Binary to Excess-1 Converter (BEC) based SQRT CSLA architecture to improve the accumulation function of MAC unit. A new BEC based SQRT CSLA architecture is named as “Modified Square Root Carry Select Adder (MSQRTCSLA). Low power consumption, High Speed and Less area utilization are the main key factors in VLSI System design environment. Therefore, Minimizing the Area-Delay Product (ADP) of MSQRTCSLA is the main goal of this study. MSQRTCSLA based accumulation structure offers 22.86% reduction of delay and 8.87% reduction power consumption than conventional BEC based SQRT CSLA based accumulation structure.

Keywords: Binary to Excess 1 Converter (BEC) based Square Root Carry Select Adder (SQRT CSLA), Modified Square Root Carry Select Adder (MSQRTCSLA), Reduced Full Adder (RFA), Reduced Half Adder (RHA), Very Large Scale Integration (VLSI) system design environment

INTRODUCTION

In VLSI System design environment, reducing the chip size, power consumption and increasing the speed are the main goal. High speed VLSI Systems are increasingly used in Multimedia devices, Multi-standards, Portable Mobile devices, Signals and Image Processing approaches. Memory and Processor Core are the main key factors which make VLSI System as powerful one. In case of Memory Core VLSI System design, less and utilization sharing based Reduced Instruction Set Processors (RISC) processors are used to reduce the chip size (in terms of Memory and Look-Up Table (LUT)) and power consumption. Like Memory Core, Processor Core also used to reduce the chip size (in terms of Slices and Registers). Unlike Memory Core, Processor Core uses reduced logics based RISC Processors. In every Processor Core, both Arithmetic and Logic Unit (ALU) and Multiplication and Accumulation (MAC) unit performs most of logic functions. Hence, ALU and MAC units are called as heart of every processor. In both ALU and MAC, most of the logics are performed only based on accumulation structures. Hence, an efficient structure of accumulation is the important essential part in VLSI Core design.

One of the basic VLSI based Accumulation structures is Ripple Carry Adder (RCA). It performs the accumulation function very well, but in every stage it must be wait for generating carry from previous stage. Hence, RCA accumulation structure causes more Carry Propagation Delay (CPD) to perform binary addition. In order to reduce the CPD Delay, Carry Look-ahead Adder (CLA) is designed in Wang *et al.* (2002). CLA adder effectively reduces the CPD delay, but it utilizes more hardware to reduce the delay. But, reducing both hardware utilization and delay consumption is the essential part of VLSI System core design. A lot of research works have been suggested the Carry Select Adder (CSLA) to reduce both hardware utilization and delay consumption of Accumulation structures. For instance, best Square Root Carry Select Adder (SQRT CSLA) is designed in Mohanty and Patel (2014).

In this research work, Modified Square Root Carry Select Adder (MSQRTCSLA) circuit is designed with the help of Verilog Hardware Description Language (Verilog HDL). Evaluated Synthesis Performances are better than conventional Binary to Excess-1 Converter (BEC) based SQRT CSLA designed in Mohanty and Patel (2014). In the proposed designed a new half adder

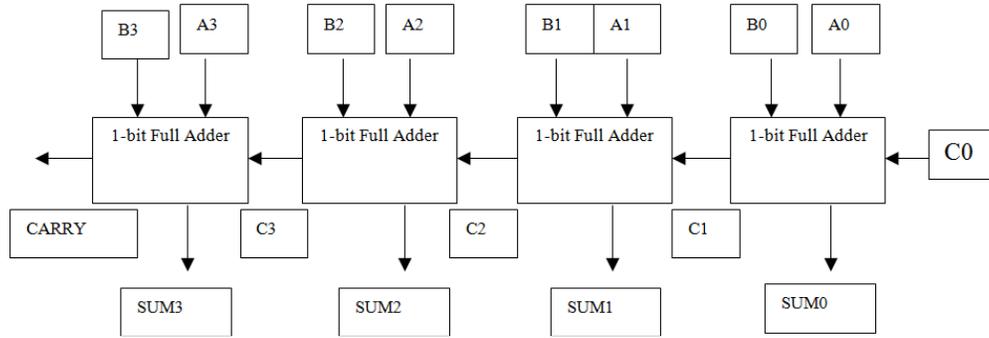


Fig. 1: Architecture of 4-bit Ripple Carry Adder (RCA)

and full adder circuits are introduced to reduce the complexity of data flow structures.

LITERATURE REVIEW

The design of hybrid Carry Look-ahead Adder (CLA) is done in Wang *et al.* (2002). In this review, 56-bit hybrid CLA adder is designed with the help of static CMOS design. The critical path of this design reduces 2/3 of the critical path lengths of RCA adder. However, it consumes large area utilization than RCA circuit. In order to reduce this problem, CSLA Adder has been suggested by large endeavours. Tyagi (1993), a reduced area scheme for CSLA adder has been proposed. In this review work, delay has been reduced to 25 ns for performing two 16-bit addition operations. This review uses combined structure of carry skip and parallel prefix adder to perform the addition operation of CSLA. Power consumption has been increased due to using skipping adder. In order to overcome this problem Power-Delay efficient hybrid adder structures are developed in Nève *et al.* (2004) and He and Chang (2008). In those adder structures, 2's complement functions are used to develop the hybrid CLA and CSLA structures. In addition, Variable Length (VL) - Adder design has been proposed in Chen *et al.* (2010) with the help of hybrid structures proposed in Nève *et al.* (2004) and He and Chang (2008). Ramkumar and Kittur (2012) group structures based SQRT CSLA adder has been proposed for reducing the gate count of adder design. More than 50% of gates are reduced in the design of Ramkumar and Kittur (2012) than design of proposed previous adders. Based on this adder structures, effective parallel adder structures has been proposed in Mary and Renji (2014), Moosalrshad *et al.* (2014) and Mohanty and Patel (2014).

In Mohanty and Patel (2014) and Avuthu *et al.*, (2015), an efficient design of Full adders and Half adders based group structures are proposed for BEC based SQRT CSLA architecture. This is the best work in 2014 for adding two N-bit binary data. In this research work, design of Mohanty and Patel (2014) is considered as conventional technique. Further Multiplexer based Full Adder used in Anna *et al.* (2015) for digital FIR Filter is also considered. In this

modification, delay for accumulation function has been reduced to 21.816ns. Further the enhanced low power Gate Diffusion Input (GDI) logic based adder has been proposed in Anitha *et al.* (2015). GDI based CSLA adder produce 455 mW power, which is better than RCA adder power.

Ripple carry adder: Ripple Carry Adder (RCA) is one of the best VLSI based Adders which performs two N-bit binary additions with the help of N Full adder circuits. Most disadvantage of this accumulation structure is CPD delay. This delay has been occurred in each stage due to waiting for generating carry bit from previous stage. The architecture of 4-bit RCA is illustrated in Fig. 1.

In Fig. 1, Carry output of second 1-bit full adder must be waiting for generating Carry Input (C1) from first 1-bit full adder. Similarly third and fourth 1-bit full adder must be waiting for generating carry input (C2) from second and third 1-bit full adder respectively. Hence, RCA adder requires more CPD delay for performing N-bit addition process. In order to reduce this problem, Carry Select Adder (CSLA) is preferred in lot of endeavours.

Carry select adder: Carry Select Adder is a type of parallel adder in which N-bit binary data is divided into \sqrt{N} groups for performing addition process. Each and every group can execute concurrently based on inputs. Hence, CPD delay can be reduced to \sqrt{N} times than RCA circuits. Hence, it is used to alleviate the architectures in terms of VLSI main concerns. It has two general architectures named as "Dual RCA Based Carry Select Adder" and "BEC Based Carry Select Adder".

Dual RCA based carry select adder: The structure of dual RCA based CSLA circuit is illustrated in Fig. 2. As the name itself, it uses the dual sets of RCA to perform the addition operation. For instance, in 16-bit dual RCA based CSLA circuit uses four groups to perform addition operation. Each group can be executed in a parallel manner. Each and every group has dual RCA pairs for $C_{in} = 0$ and $C_{in} = 1$ respectively. Finally,

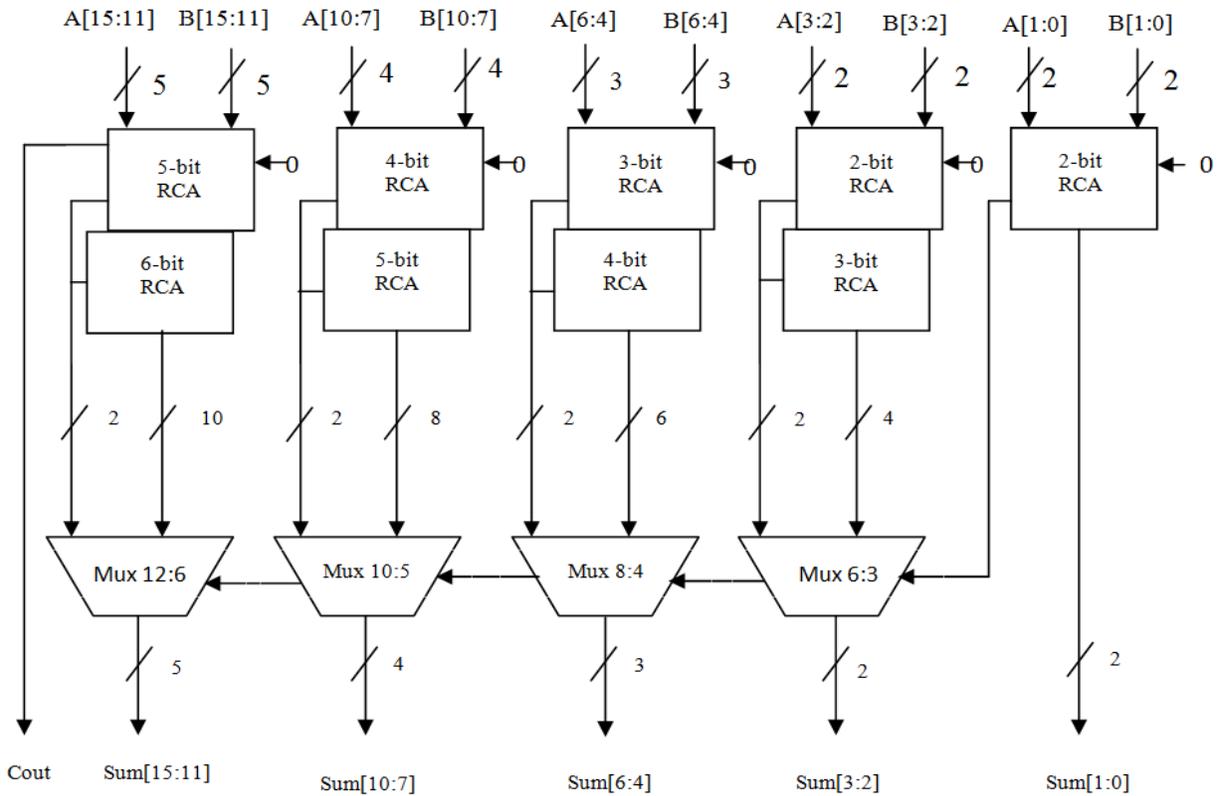


Fig. 2: Architecture of 16-bit dual RCA based CSLA

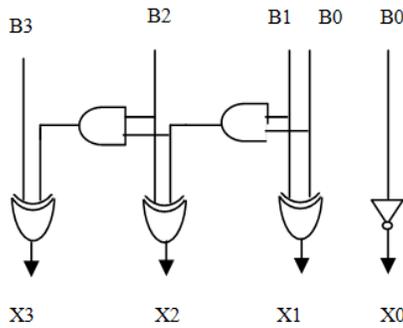


Fig. 3: Architecture of 4-bit Binary to Excess 1 Conversion (BEC) circuits

multiplexer circuits are used to estimate the final sum and carry of 16-bit addition.

16-bit RCA circuit has CPD delay in each stage. But, 16-bit dual RCA based CSLA has only 4 times of RCA CPD delay. However, due to final stage of multiplexer circuits, it is possible to increase the hardware complexity of CSLA circuit. But, it can be identified same logic functions have been used in all groups. Hence, resources have been shared for performing function of each and every group.

Due to sharing same utilization, hardware complexity of dual RCA based CSLA has been reduced significantly. Also power consumption has been

reduced due to reducing the complexity of computational path. However, dual set of RCA circuits didn't give more advantage when integrating into digital signal processing applications like multiplication and filtering structures. Hence, Binary to Excess 1 Converter (BEC) based Sqrt CSLA circuits have been introduced in the past.

BEC based carry select adder: Binary to Excess 1 Converter (BEC) is the conversion circuit in which binary codes are converted into Excess 1 codes. The circuit for 4-bit Binary to Excess 1 (BEC) is illustrated in Fig. 3. The advantage of BEC circuit is that it acts as both conversion circuit and Ripple Carry Addition circuit. When $C_{in} = 1$, hence, RCA when $C_{in} = 1$ circuit of dual RCA based Sqrt CSLA is replaced by BEC based Sqrt CSLA circuit. Like dual RCA based Sqrt CSLA circuit, BEC based Sqrt CSLA circuit has \sqrt{N} groups and each group can execute in a parallel manner.

Architecture of 16-bit BEC based Sqrt CSLA is illustrated in Fig. 4. As the name itself, BEC circuits are involved in the second part of RCA circuits. Each group structure can run concurrently when input data are available. The performance analysis of BEC based Sqrt CSLA has been briefly analyzed in Mohanty and Patel (2014). Group-2 and Group-3 structures of 16-bit BEC based Sqrt CSLA are illustrated in Fig. 5.

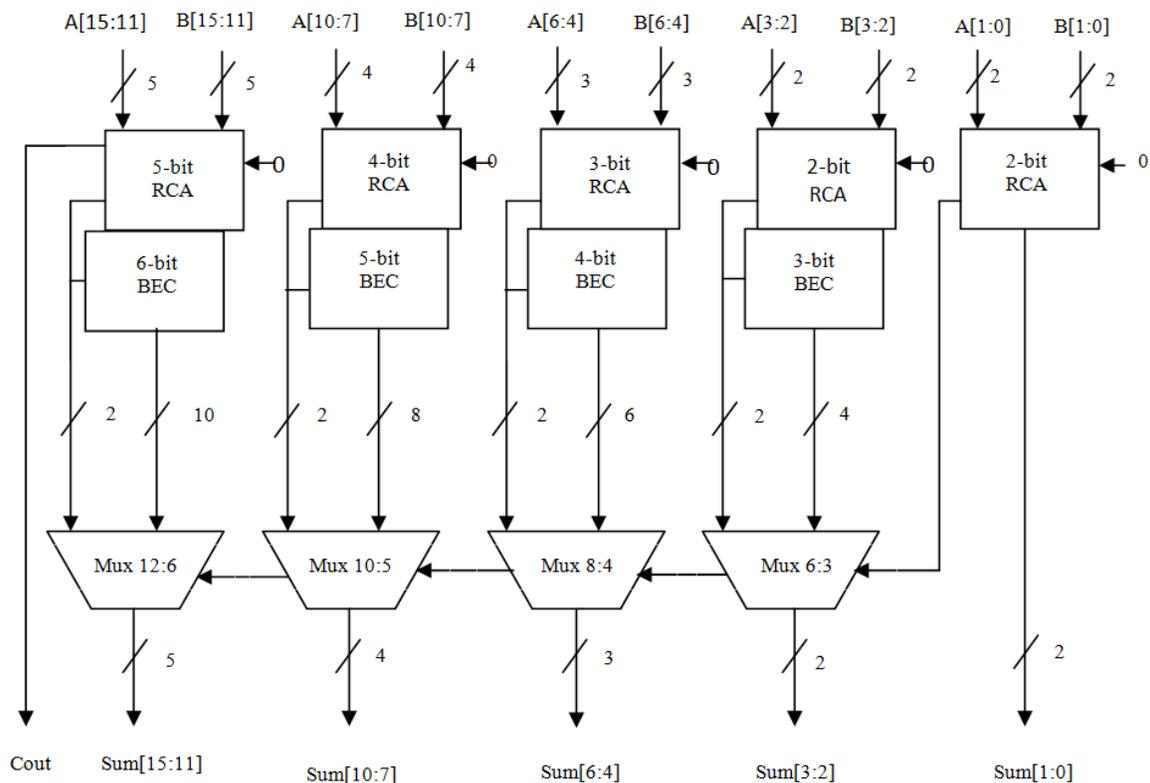


Fig. 4: Architecture of 16-bit BEC based Sqrt CSLA

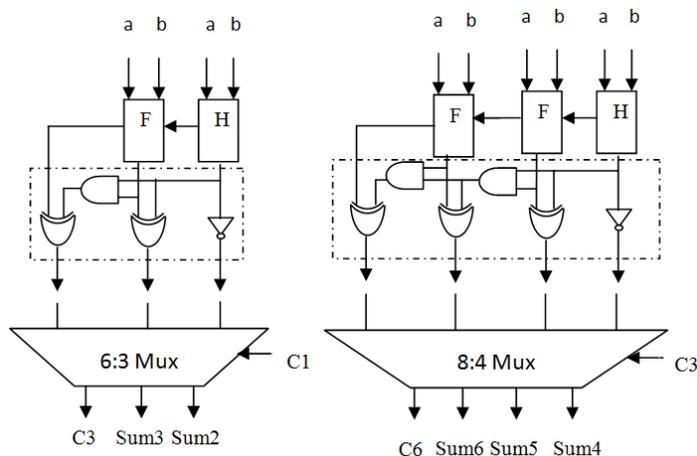


Fig. 5: Group-2 and Group-3 Structures of BEC based Sqrt CSLA

In first stage of group structure, combination of half adders and full adders are involved to perform RCA functions. In second stage, BEC circuits are used instead of using another RCA for $C_{in} = 1$. Finally multiplexer circuits are used to find the final sum carry output. A lot of research works have been suggested the BEC based Sqrt CSLA circuit for 'n' bit addition process. However, to further enhance the BEC circuits, D-latch circuits is used in more research works. When compared to BEC based Sqrt CSLA, D-Latch based Sqrt CSLA circuit utilize less hardware. However, D-

Latch based Sqrt CSLA circuit consumes more delay to perform 'n' bit addition operation. Hence, BEC based Sqrt CSLA circuit gives the best performance in terms of VLSI main concern up to mark.

PROPOSED MODIFIED SQUARE ROOT CARRY SELECT ADDER

In this study, Reduced Half Adder (RHA) and Reduced Full Adder (RFA) is designed to improve the performances of BEC based Sqrt CSLA circuit. Half

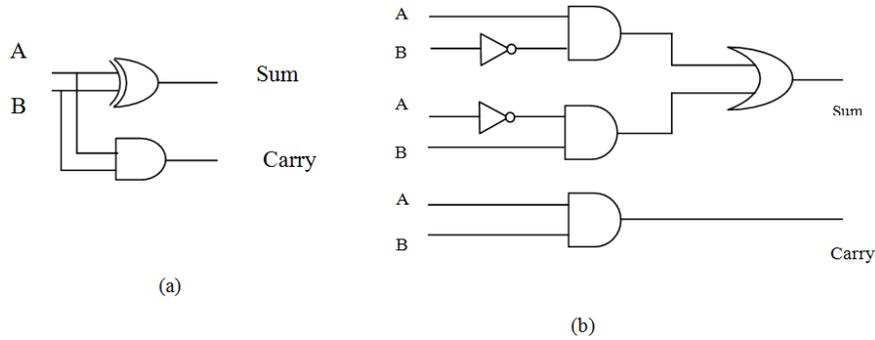


Fig. 6: (a): Half adder circuit; (b): Half adder using basic gates

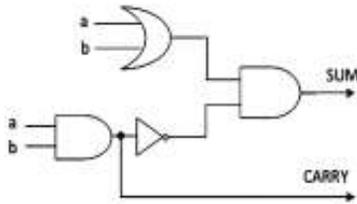


Fig. 7: Reduced half adder

Basic blocks of CSLA	Gate count
XOR	5
2:1 Multiplexer	4
Half adder	6
Full adder	13

Adder and Full Adder are the main blocks of BEC based SQRT CSLA circuit. The proposed RHA and RFA design methodologies have been briefly illustrated in this section.

Design procedure of Reduced Half Adder (RHA): The generalized circuits for Half Adder (HA) are illustrated in Fig. 6a and b.

From Fig. 6, it is clear that, 6 gates are required to design Half Adder (HA) circuit. This generalized circuit for HA is realized in this study. Unwanted redundant operations are identified and eliminated to reduce the hardware complexity. The function of Sum and Carry of HA circuit is demonstrated as follows:

$$Sum = A \oplus B \quad (1)$$

$$Sum = \overline{A}B + A\overline{B} \quad (2)$$

The Sum also represented as follows:

$$\begin{aligned} Sum &= \overline{A}B + \overline{A}B + \overline{A}A + B\overline{B} \\ Sum &= \overline{A}A + \overline{A}B + B\overline{B} + A\overline{B} \\ Sum &= \overline{A}(A+B) + \overline{B}(A+B) \\ Sum &= (A+B)(\overline{A} + \overline{B}) \end{aligned} \quad (3)$$

By using De-Morgan's Theorem, $\overline{A} + \overline{B}$ can also be written as \overline{AB} . Hence, Eq. (3) become as:

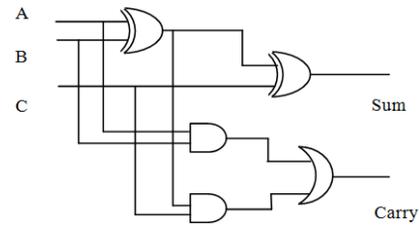


Fig. 8: Full adder circuit

$$Sum = (A + B)(\overline{AB}) \quad (4)$$

$$Carry = AB \quad (5)$$

Modified or Reduced Half Adder (RHA) circuit is illustrated in Fig. 7 by using Eq. (4) and Eq. (5). When compared to Fig. 6b, reduced half adder uses only 4 gates to implement the half adder function. Gate count for traditional hardware elements like HA, FA and Multiplexer circuits is illustrated in Table 1.

Gate Count of conventional HA (Fig. 6b) Circuit is determined as follows:

$$\begin{aligned} \text{Gate Count of conventional HA} &= \text{Gate Count} \\ &= [(3*\text{AND}) + (2*\text{NOT}) + (1*\text{OR})] \\ \text{Gate Count of conventional HA} &= [(3*1) + (2*1) + (1*1)] = 3+2+1 = 6 \end{aligned}$$

Similarly, gate count of proposed reduced HA (Fig. 7) Circuit is determined as follows:

$$\begin{aligned} \text{Gate Count of Proposed RHA} &= \text{Gate Count} \\ &= [(2*\text{AND}) + (1*\text{OR}) + (1*\text{NOT})] \\ \text{Gate Count of Proposed RHA} &= [(2*1) + (1*1) + (1*1)] = 4 \end{aligned}$$

Design procedure of Reduced Full Adder (RFA): Like HA circuit, Full Adder circuit also has been realized and redundant functions are eliminated to further improve the architectural performances. The generalized Full Adder circuit block is illustrated in Fig. 8. FA circuit consists of two HA circuit and a single OR gate to perform the 3-bit addition operation.

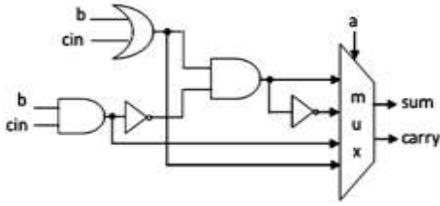


Fig. 9: Reduced full adder

RHA performs HA functions with the help of only 4 gates. Hence with the help of RHA circuit, Reduced Full Adder (RFA) circuit has been designed by using minimal number of logic gates. Also Multiplexer (MUX) based RFA circuit has been designed in this study to further alleviates the performances of digital adder circuits.

Gate Count of conventional FA (Fig. 8) Circuit is determined as follows:

$$\begin{aligned} \text{Gate Count of conventional FA} &= \text{Gate Count} \\ &[(2*\text{XOR}) + (2*\text{AND}) + (1*\text{OR})] \\ \text{Gate Count of conventional FA} &= [(2*5) + (2*1) + \\ &(1*1)] = 10+2+1 = 13. \end{aligned}$$

$$\begin{aligned} \text{Gate Count of Proposed RFA} &= \text{Gate Count} \\ &[(2*\text{RHA}) + (1*\text{OR})] \\ \text{Gate Count of Proposed RFA} &= [(2*4) + (1*1)] = \\ &8+1 = 9. \end{aligned}$$

The structure of Reduced Full Adder (RFA) is illustrated in Fig. 9.

The Sum and Carry of RFA has been denoted as follows:

$$\text{Sum} = \sum_{A=0}^1 [X \cdot \bar{A} + \bar{X} A] \quad (6)$$

where,

$$\begin{aligned} X &= (B + C) \cdot \bar{B}\bar{C} \\ &= \bar{B}\bar{C} + C\bar{B} \\ &= B \oplus C \\ \bar{X} &= \overline{(B + C) \cdot \bar{B}\bar{C}} \\ &= \overline{\bar{B}\bar{C} + C\bar{B}} \\ &= BC + \bar{B}\bar{C} \\ &= B \oplus C \end{aligned}$$

Table 2: Theoretical Gate Count (GC) calculation for both conventional BEC based SQR T CSLA and proposed MSQR TCSLA

Conventional BEC based SQR T CSLA	Proposed MSQR TCSLA
<p>Group-2</p> <p>GC = GC [RCA + BEC + MUX] GC[RCA]=GC[(1*HA)+(1*FA)] GC [RCA] = (1*6) + (1*13) GC [RCA] = 19. GC[BEC]=GC[(2*XOR)+(1*AND)+ (1*NOT)] GC [BEC] = (2*5) + (1*1) + (1*1) GC [BEC] = 12. GC [MUX] = (2*4) = 8. GC = 19+12+8 = 39.</p>	<p>Group-2</p> <p>GC = GC [RCA + BEC + MUX] GC[RCA]=GC[(1*RHA)+(1*RFA)] GC [RCA] = (1*4) + (1*9) GC [RCA] = 13. GC[BEC]=GC[(2*MXOR)+(1*AND)+ (1*NOT)] GC [BEC] = (2*4) + (1*1) + (1*1) GC [BEC] = 10. GC [MUX] = (2*4) = 8. GC = 13+10+8 = 31.</p>
<p>Group-3</p> <p>GC = GC [RCA + BEC + MUX] GC[RCA]=GC[(1*HA)+(2*FA)] GC [RCA] = (1*6) + (2*13) GC [RCA] = 32. GC[BEC]=GC[(3*XOR)+(2*AND)+ (1*NOT)] GC [BEC] = (3*5) + (2*1) + (1*1) GC [BEC] = 18. GC [MUX] = (2*4) = 8. GC = 32+18+8 = 58.</p>	<p>Group-3</p> <p>GC = GC [RCA + BEC + MUX] GC[RCA]=GC[(1*RHA)+(2*RFA)] GC [RCA] = (1*4) + (2*9) GC [RCA] = 22. GC[BEC]=GC[(3*MXOR)+(2*AND)+ (1*NOT)] GC [BEC] = (3*4) + (2*1) + (1*1) GC [BEC] = 15. GC [MUX] = (2*4) = 8. GC = 22+15+8 = 45.</p>
<p>Group-4</p> <p>GC = GC [RCA + BEC + MUX] GC[RCA]=GC[(1*HA)+(3*FA)] GC [RCA] = (1*6) + (3*13) GC [RCA] = 45. GC[BEC]=GC[(4*XOR)+(3*AND)+ (1*NOT)] GC [BEC] = (4*5) + (3*1) + (1*1) GC [BEC] = 24. GC [MUX] = (2*4) = 8. GC = 45+24+8 = 77.</p>	<p>Group-4</p> <p>GC = GC [RCA + BEC + MUX] GC[RCA]=GC[(1*RHA)+(3*RFA)] GC [RCA] = (1*4) + (3*9) GC [RCA] = 31. GC[BEC]=GC[(4*MXOR)+(3*AND)+ (1*NOT)] GC [BEC] = (4*4) + (3*1) + (1*1) GC [BEC] = 20. GC [MUX] = (2*4) = 8. GC = 31+20+8 = 59.</p>
<p>Group-5</p> <p>GC = GC [RCA + BEC + MUX] GC[RCA]=GC[(1*HA)+(4*FA)] GC [RCA] = (1*6) + (4*13) GC [RCA] = 58. GC[BEC]=GC[(5*XOR)+(4*AND)+ (1*NOT)] GC [BEC] = (5*5) + (4*1) + (1*1) GC [BEC] = 30. GC [MUX] = (2*4) = 8. GC = 58+30+8 = 96.</p>	<p>Group-5</p> <p>GC = GC [RCA + BEC + MUX] GC[RCA]=GC[(1*RHA)+(4*RFA)] GC [RCA] = (1*4) + (4*9) GC [RCA] = 40. GC[BEC]=GC[(5*MXOR)+(4*AND)+ (1*NOT)] GC [BEC] = (5*4) + (4*1) + (1*1) GC [BEC] = 25. GC [MUX] = (2*4) = 8. GC = 40+25+8 = 73.</p>
<p>Total</p> <p>GC = 39+58+77+96 = 270</p>	<p>Total</p> <p>GC = 31+45+59+73 = 208</p>

Table 3: Percentage reduction of gate count values in proposed MSQRTCSLA

Conventional BEC based Sqrt CSLA	Proposed MSQRTCSLA	Percentage reduction
Group-2	Group-2	20.51%
Group-3	Group-3	22.41%
Group-4	Group-4	23.37%
Group-5	Group-5	23.95%
Total	Total	22.96%

$$Carry = \sum_{A=0}^1 [BC\bar{A} + (B+C)A] \quad (7)$$

In Proposed Modified Sqrt CSLA circuit, design of both RHA and RFA circuits are integrated into group structures of BEC based Sqrt CSLA circuit.

Theoretical evaluation of gate count for conventional BEC based Sqrt CSLA and Proposed MSQRTCSLA: In 16-bit BEC based Sqrt CSLA circuit, 4 groups are used to perform the addition operation. Each group has both RCA and BEC circuits. Similarly, 16-bit MSQRTCSLA circuit has also 4 groups to perform the addition operation.

MSQRTCSLA circuit uses both RHA and RFA circuits effectively. The gate count calculation for each and every group structures of both conventional BEC based Sqrt CSLA and proposed MSQRTCSLA circuits are analyzed theoretically in Table 2. Table 3 illustrates the percentage reduction of gate count in Proposed MSQRTCSLA circuit.

SYNTHESIS RESULTS AND DISCUSSION

Design of Reduced Half Adder (RHA) and Reduced Full Adder (RFA) has been done through Verilog HDL. Proposed RHA and RFA circuits are to be integrated in 16-bit conventional BEC based Sqrt CSLA circuits to alleviate the performances of Sqrt CSLA circuit. Hence, this circuit named as “Modified Sqrt CSLA”. Simulation Results have been validated by using ModelSim 6.3C tool. The Simulation results of VLSI based Proposed 16-bit MSQRTCSLA is illustrated in Fig. 10. Register Transfer Level (RTL) view for Proposed MSQRTCSLA circuit is illustrated in Fig. 11. Detailed RTL view for each every group structure of Proposed MSQRTCSLA circuit is illustrated in Fig. 12.

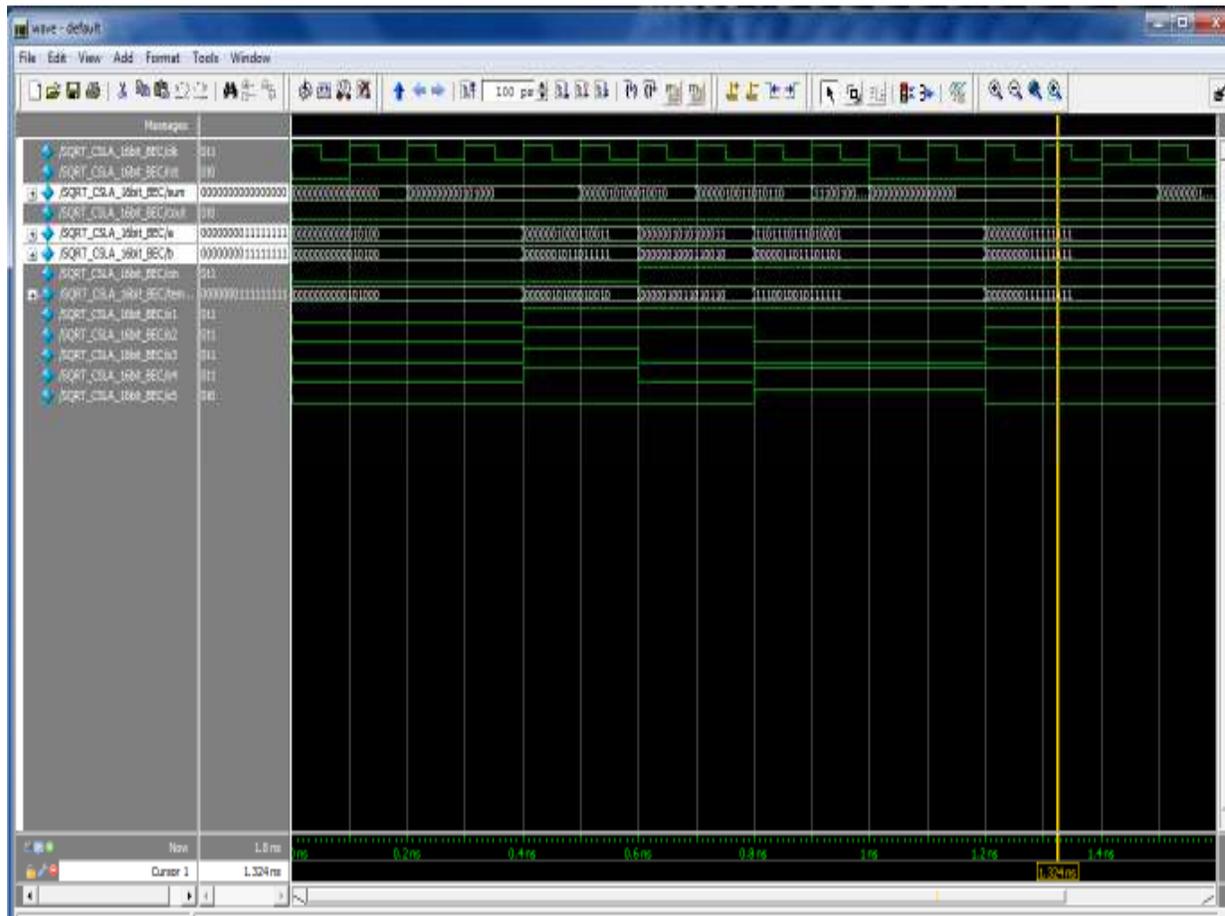


Fig. 10: Simulation result of VLSI based proposed 16-bit MSQRTCSLA adder circuit

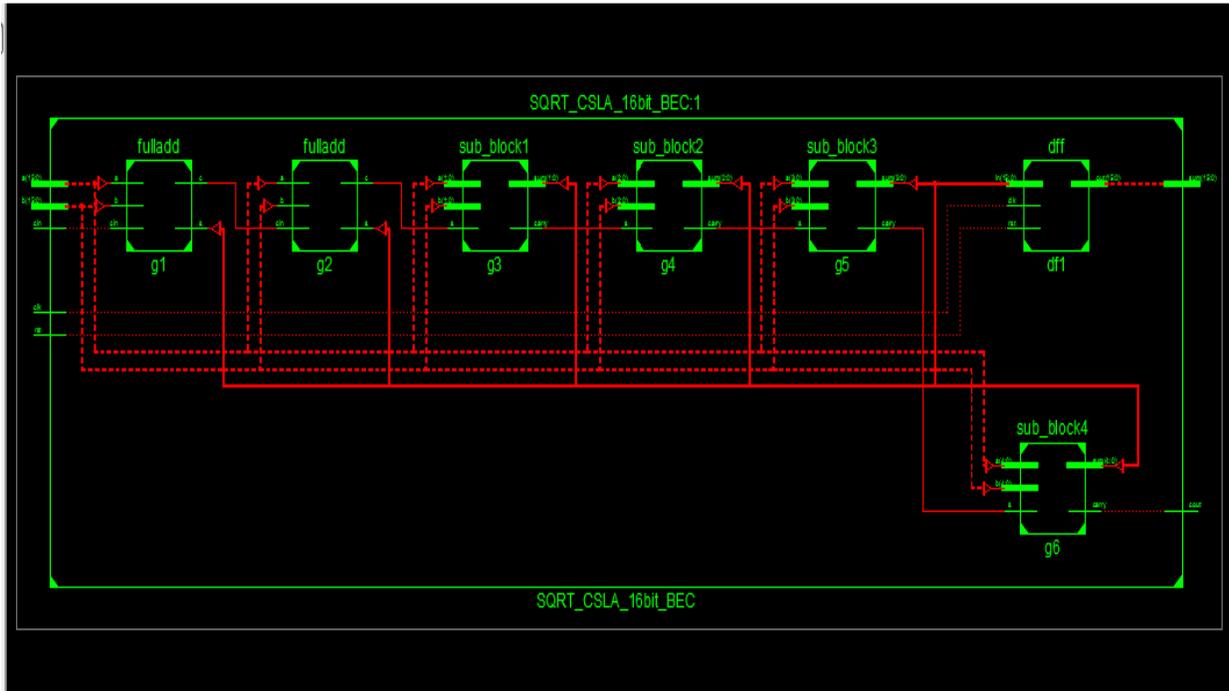


Fig. 11: RTL view for proposed 16-bit MSQRTCSLA adder circuit

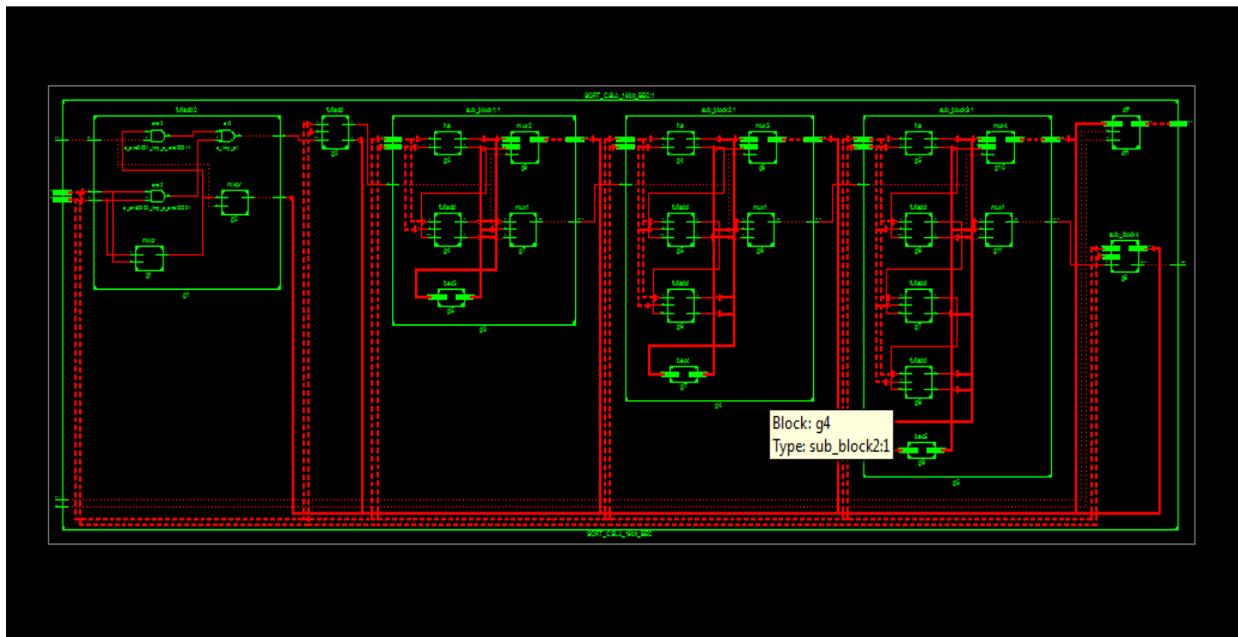


Fig. 12: Detailed RTL view for proposed 16-bit MSQRTCSLA adder circuit

Table 4: Comparison of synthesis performances for both conventional 16-bit BEC based SQRT CSLA and proposed 16-bit MSQRTCSLA

Parameters	Conventional 16-bit BEC based SQRT CSLA	Proposed 16-bit MSQRTCSLA	Percentage reduction
Number of occupied slices	28	26	7.14%
Total number of LUT's	47	46	2.12%
Maximum of inputs arrival time before clock (ns)	15.971	12.319	22.86%
Maximum output required time after clock (ns)	6.216	6.216	~
Maximum combinational delay path	22.421	18.916	15.63%
Frequency (MHz)	62.613	81.175	22.86%
Power (mW)	338	308	8.87%

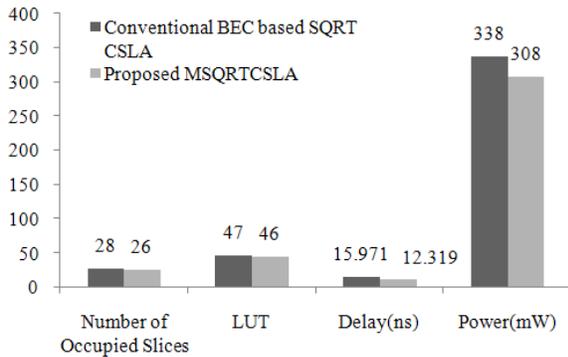


Fig. 13: Performance evaluations for both conventional BEC based Sqrt CSLA and proposed MSQRTCSLA

Synthesis results have been evaluated by using appropriate tools for measuring the utilization of hardware, delay and power of Proposed MSQRTCSLA circuit. Synthesis Results of both conventional 16-bit BEC based Sqrt CSLA and proposed 16-bit MSQRTCSLA circuit is analyzed and compared in Table 4. The performance evaluations are graphically illustrated in Fig. 13.

When compared to results of Tyagi (1993) and Anna *et al.* (2015), Proposed MSQRTCSLA circuit offers 50.72 and 43.53% reduction in delay consumption respectively. Similarly, when compared to the results of Mary and Renji (2014) and Mohanty and Patel (2014), Proposed circuit offer 34.36% reduction in delay consumption. Hence, from above consecution, it is clear that, Proposed MSQRTCSLA circuit gives high speed operation than all other best existing methods.

CONCLUSION

Reduced Half Adder (RHA) and Reduced Full Adder (RFA) are proposed in this study to improve the speed and power consumption of BEC based Sqrt CSLA adder circuit. The reduced number of gates of this study provides the great advantage in the reduction of delay and power consumption. Proposed Modified Sqrt CSLA adder circuit offers 7.14% reduction of Slices, 2.12% reduction of LUTs, 22.86% reduction of maximum input arrival times, 15.63% reduction of maximum combinational path delays and 8.87% reduction of power consumption than conventional BEC based Sqrt CSLA circuit. The Area-Delay Product (ADP) and Power-Delay Product (PDP) of proposed MSQRTCSLA design shows great advantage than conventional BEC based Sqrt CSLA. The proposed MSQRTCSLA architecture is therefore, high speed, low area, low power, simple and an efficient for

VLSI hardware implementation. In future, proposed MSQRTCSLA adder circuit will be integrated in different types of MAC units to alleviate the performances of MAC in terms of VLSI main concerns. Also Proposed MSQRTCSLA adder structure will be absolutely suitable for specific digital signal processing applications like Filtering, Frequency transformation techniques and Wireless digital communication for performing digital addition process.

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