Research Journal of Applied Sciences, Engineering and Technology 8(7): 900-906, 2014 DOI:10.19026/rjaset.8.1051 ISSN: 2040-7459; e-ISSN: 2040-7467 © 2014 Maxwell Scientific Publication Corp.

Submitted: June 20, 2014

Accepted: July 19, 2014

Published: August 20, 2014

Research Article Design of a Novel Optimized MAC Unit using Modified Fault Tolerant Vedic Multiplier

¹R. Deepa and ²A. Shanmugam

¹Department of E&I, Bannari Amman Institute of Technology, Sathyamangalam, Chennai, India ²Department of ECE, SNS College of Technology, Coimbatore, India

Abstract: In this study, the design of optimized Multiplication and Accumulation (MAC) unit with modified Vedic multiplier is presented. To design a MAC unit, efficient multiplier is used to increase speed and to reduce area and power. Conventional MAC is designed using without fault tolerant Vedic multiplier. But it consumes more area and power. And also less delay. So MAC unit is changed to design the efficient Vedic multiplier. Conventional MAC unit with regular Vedic multiplier is not working for some of the inputs condition. To overcome this fault, novel Vedic multiplier is proposed and designed using less half adder and Full Adder. Simulation is carried out using Modelsim 6.3c. Synthesis and Implementation is carried out using Xilinx and FPGA Spartan 3.

Keywords: Fault tolerant multiplier, FPGA spartan 3, MAC, vedic multiplier

INTRODUCTION

MAC unit is used in ALU block. As all of us know that the Computation unit is main unit of any technology (Cieplucha, 2013), which performs different arithmetic operations like as addition, subtraction and multiplication etc., also in some places it performs logical operations also like as AND, OR, INVERT, X-OR etc. which is dominant feature in the digital domain based applications (Deepak and Kailath, 2012). ALU is the execution unit which does not only perform Arithmetic operations but also logical operations. And that's why ALU is called as the heart of Microprocessor, Microcontrollers and CPUs. No technology can exist, without those operations which are performed by ALU (Shams et al., 1998). Every technology uses works upon those operations either fully or partially which are performed by ALU.

The DSP functions extensively make use of the Multiply Accumulate operation, for high performance Digital signal processing system (Itawadiya *et al.*, 2013). A basic MAC architecture consist of a Multiplier and an accumulate adder organized as in Fig. 1. MAC unit compute the product of two numbers and adds the product to an accumulator register (Jaina *et al.*, 2011). The output of register is fed back to one input of the adder as shown in Fig. 1 (Shanthala *et al.*, 2009).

DESIGN OF MAC UNIT USING CONVENTIONAL VEDIC MULTIPLIER

Vedic multiplier can propose using different algorithm. In this study Urdhava-Tiryakbhyam

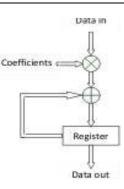


Fig. 1: Architecture of MAC unit

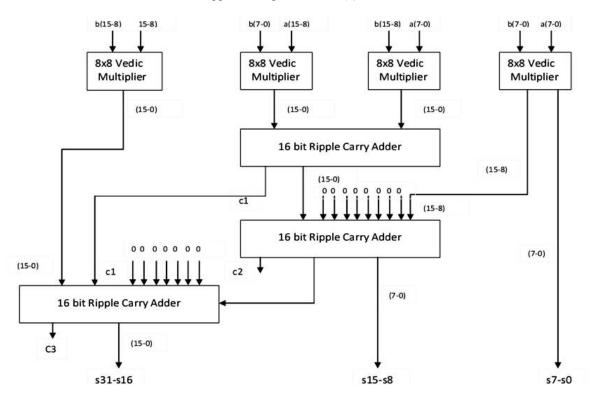
algorithm is used to design the Vedic multiplier (Bansal *et al.*, 2014). Urdhava-Tiryakbhyam is the common formula applicable to all cases of multiplication and also in the division of a huge number by another huge number. It means perpendicularly and diagonally (Huddar *et al.*, 2013) (Fig. 2).

Conventional Vedic multiplier is constructed using Ripple Carry Adder (RCA). RCA consist of number of full adders and half adders. Conventional Vedic multiplier is not working properly, when the carry input has more than one number of ones. So it will be generate fault output, when the carry input consist of more number of one's (Kunchigi *et al.*, 2012).

Proposed MAC unit using modified vedic multiplier: In this research study, Modified Vedic multiplier is proposed to reduce the total number of half adder and full adder in order to rectify the fault, when the carry is 1. From the conventional Vedic multiplier,

Corresponding Author: R. Deepa, Department of E&I, Bannari Amman Institute of Technology, Sathyamangalam, Chennai, India

This work is licensed under a Creative Commons Attribution 4.0 International License (URL: http://creativecommons.org/licenses/by/4.0/).



Res. J. App. Sci. Eng. Technol., 8(7): 900-906, 2014

Fig. 2: Block diagram of conventional vedic multiplier for existing MAC unit

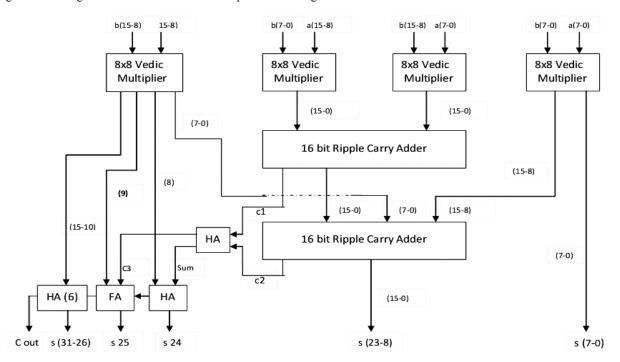
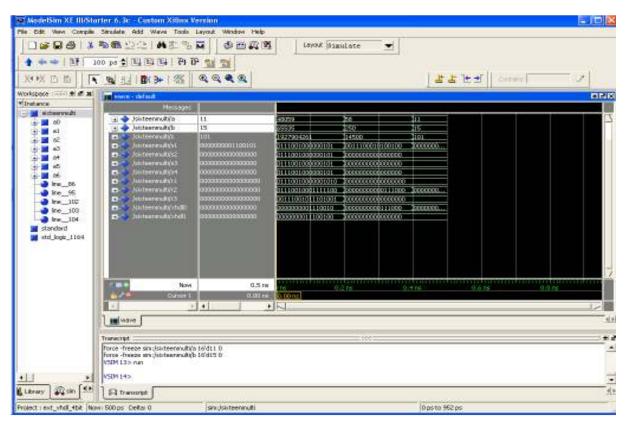


Fig. 3: Block diagram of modified vedic multiplier for proposed MAC unit

2nd and 3rd Ripple Carry Adder (RCA) block is changed in order to reduce the number of half adders and full adders. Modified Vedic multiplier is applied into the proposed MAC unit (Fig. 3).

MAC design with modified Vedic multiplier offers low area, delay and power compared to conventional MAC design with regular Vedic multiplier. Simulation results are illustrated as shown in the Fig. 4 and 5. Synthesis is performed to analyze the area, delay and power. Power can be evaluated using X-power analyzer. Synthesis results are given in the Fig. 6 to 8.



Res. J. App. Sci. Eng. Technol., 8(7): 900-906, 2014

Fig. 4: Simulation result of conventional vedic multiplier with fault during carry = 1

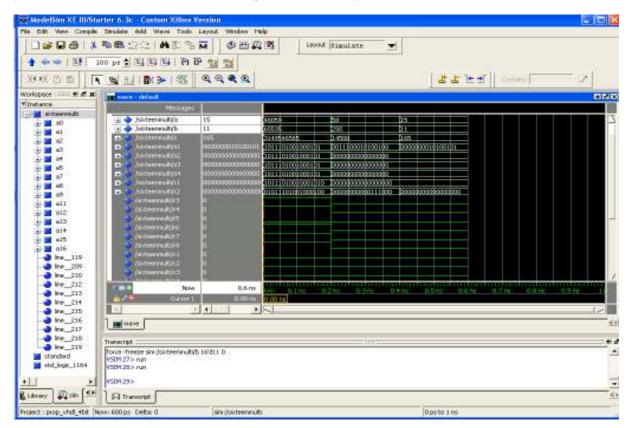


Fig. 5: Simulation result of proposed vedic multiplier without fault during carry = 1

13 18 EU / 15	YBBY BY BALLY DOL	XXXXX A SEDD	A NO M delay	
	taan oo	AAPS ABOUT	- AF DU 46 long	
ourcei 🗶	TIRING REPORT			
ources for: Implement v				
vedic_existing_with sc3r504pq200 in v_p_mac_add1t		RS ARE ONLY A SYNTHESIS ESTIMAT 5 INFORMATION FLEASE REFER TO T ACE-and-ROUTE.		
ili 😧 isideen Vieg1 (reg.v)	Clock Information:			
	Clock Signal	Clock buffer (FF ne		
	cik	I BUFGP	1 64 1	
45 OF ST DU				
hocesses for mac_ad A	Asynchronous Control Sig	nals Information:		
Add Existing	No asynchronous control :	signals found in this design		
12 Vew Design	Timing Summary:			
# 😼 Decign Utiliti	****			
H 😼 User Consh/	Speed Grade: -5			
E COOSyntheside			22753) V	
Wen Sp		ne (Naximum Frequency: 194.4458	DK=)	
CD Vern R1		time before clock: 43.404ns ed time after clock: 6.280ns		
View Te		path delay: No path found		
() () German	Timing Detail:			
6 Complement D				
11 R3 Parents Ph	All values displayed in a	(ent shands inch		

(a) Delay of conventional MAC unit with regular vedic multiplier

		PXXPB ABBORIP	X7 (A) (A) (A)	w (M 1 V
Sources or implement.≪ Sources for implement.≪ © vedic_proposed_w ≡ ○ vedic_proposed		RS ARE ONLY A SYNTHESIS ESTIMATE. G INFORMATION PLEASE REFER TO THE ACE-and-ROUTE.	TRACE REPORT	¢
	Timing Summery Speed Grade: -5 Minimum period: 5.143 Minimum input arrival Maximum output requir		1 54 1	
Check 5 B C General C General C Constant 0 C Processes	Timing Detail: All values displayed in C T Design Summary			

(b) Delay of proposed MAC unit using modified vedic multiplier

Fig. 6: Synthesis result of conventional and modified MAC unit for delay utilization

1 6 2 8 E	are xoox are 2 pp	XX#B	38800 / ¥ ¥ I	M) 🚜 dela		0		
iources 🛪	🐒 FPGA Design Summary 🔥	eign Summary A vedic_existing_with_mac_16_bit Project Status (05/24/2014 - 14:03:29)						
ources for Implement	3 Design Overview	Project File:	vedic_exiting_with_mac_16_bit ine	Current S	State:	Placed and Route	d	
ii 🖸 vc3c50-5pg208	- Summary - Si 108 Properties	Module Nome:	mac_edd16	•6	monia:	No Errora		
B Wingmac, add15 B Module Level Utilization	Target Device:	Target Device: xc3r50 5pg208 + Warnings:		10 Warnings				
B Will - zieteen	Timing Constraints	Product Version:	ISE 10.1 - WW6PACK	• B	outing Results:	All Sizzala Complet	Inly Route	
ieg1 (reg v)	Pinoul Report	Design Goat	Balanced	• T	ming Constraints:	All Constitients Met	6	
	Enter and Warnings	Design Strategy:	Xins Default (unlocked)	• Fi	nal Timing Score	Olimma Report	1	
Constant for mag. add16	Place and Route Messages	eges Route Messages						
Add Existing Sol	Bilger Meriages			und	Available	Utilization	Notefa	
Deate New Sou	All Current Messages	Number of Silce Fip F	Tops	64	1.536	43		
Constant sheet Sold	= Dalalad Ranoth	Number of 4 input UU	Ta	773	1.536	50%	-	
T View Design Su	Project Properties D Enable Enhanced Design Summary	Logic Distribution		2201	11521			
T View Design Su Design Utilities		Number of occupied	Gener	421	768	54%		
 View Design Su Design Utilities User Constraints 	Enable Message Filtering	number of occupied				1003		
View Design Su Design Utilities User Constraints OSynthesize -XS	Enable Message Filtering Display Incremental Messages		onlaining only related logic	421	421	1000		
Vew Design Su Design Utilities User Constraints Office Synthesize - XS Office Synthesize - XS	Enable Message Filtering	Number of Silces of	a la la companya da l	421	421	01	-	
Vew Design Su Design Utilities Union Constraints Constraints Synthesiae - XS Instrument Design Generate Progra	Enable Message Filtering Display Incomental Messages Enhanced Design Summary Contents Show Parktion Data Show Enors	Number of Silces of	onlaining only related logic onlaining unrelated logic		5.050			
View Design Su Design Utilities User Construints Orgentieside - 1/5 Orgentieside - 1/5 Orgentieside Props	Enable Message Filtering Display Incomental Messages Enhanced Design Summary Contents Show Partition Data	Number of Silces o Number of Silces o	onlaming only related logic onlaming unrelated logic input LUTs	0	421	01		

Res. J. App. Sci. Eng. Technol., 8(7): 900-906, 2014

(a) Area of conventional MAC unit with regular vedic multiplier

	KARX SO DIPP KRAA OO	XX#2	N SECTO	17 M M	delay 🛛	9		
iesces 🗶	😰 FPGA Design Summary 👩	vedic_proposed_with_mac_unit_16_bit Project Status (05/24/2014 - 12:52:45)						
iources for Implement.	E Design Overview	Project File:	vedic_proposed_with_mac_unit,	16 bille D	unent State	Placed and Rou	led	
Vedic_proposed_w	Summary 108 Properties	Module Name:	ebac_add/16		+ Enors:	No Enors	1	
Vinnuc, add1 Module Level Dilization	Target Device:	sc3x50-5pq208		+ Warrings;	S.Wanings			
restar 1 V #	If interest Taning Constraints Interest Prove Report Interest Interest	Product Version	ISE 10.1 - WIEPACK		+ flouting flesults:	All Signals Comp Bouted	detaik.	
ind ted ∧		Design Goal:	Balanced		Timing Constraints:	ALConstructs N	ed -	
CS Dr msi Du		Design Steategy:	Xilina Default (unlocked)		Final Timing Score:	0 (Timing Report	đ	
Receiver for not, ad A A Existing A Contract of the second Power Address	vedic_proposed_with_mac_unit_16_bit Partition Summary No partition information was found.							
Create New	All Current Messages		Device UI	kzation Summ	ing			
Y Vew Design	Poject Properties	Logic Utilization		Used	Available	Utilization	Note(s	
E 🎾 Design UBM	Enable Enhanced Design Summary	Number of Silce Fig Flops		6	4 1,536	4%		
Context	Enable Message Filtering	Number of 4 input LUTs		71	7 1,536	463;	-	
Wen Sy	Citplay Incremental Message: Enhanced Design Summary Contents	Logic Distributio	n					
Vev Rt	Show Pattion Data	Number of occupier	d Silces	39	7 768	51%		
View Ht	ShowEnon	Number of Silces	containing only related logic	39	7 397	100%		
Q Deck1	Show Warrings	Number of Silces containing unrelated logic			0 397	674	-	
# C2 General	Show Faling Conchaints	Total Number of	4 input LUTs	71	7 1,536	45%		
Complement D	and all the second stages.	Number of bonded	1081	6	6 124	53%		
A REAL PROPERTY OF A READ PROPERTY OF A REAL PROPER		Number of BUFGM	1000		1 8	12%		

(b) Area of proposed MAC unit using modified vedic multiplier

Fig. 7: Synthesis result of conventional and modified MAC unit for area utilization

RESULTS AND DISCUSSION

Conventional Vedic multiplier, show the result in wrong, when 15×11 , it give 105 instead of 165 due to carry output 1 is not processed. To overcome this fault, modified Vedic multiplier is proposed.

Simulation is done using Modelsim 6.3c. Simulation result of conventional Vedic multiplier is shown in below Fig. 4 and 5. Conventional MAC with

File Tools Help					
Report Navigator	× Name	Power (W)	Used	Total Available	Utilization (%)
View	Clocks	0.078	1		-
E Seport Views	Logic	0.022	773	1536	50.3
E Summary	Signals	0.068	804		-
Themal Information	10:	15.506	66	124	53.2
Settings	Total Quiescent Powe	0.845			
By Tvoltage Source	Total Dynamic Power	15.813			
Clec Information	Total Power	15.858			
Logic Signals 10s By Hierarchy					

Res. J. App. Sci. Eng. Technol., 8(7): 900-906, 2014

(a) Power utilization of existing MAC unit using regular vedic multiplier

File Tools Help					
👌 🔒 σ 🖬 🗎					
Report Navigator	× Name	Power (w)	Used	Total Available	Unlication (%)
View	Clocks	0.096	1	-	-
C C Report Views	Logic.	0.023	717	1536	45.7
B Summary	Signals	0.114	764	-	
Themal Information	10:	15.250	66	124	532
Voltage Source Information	Total Quiescent Power	0.045		1	
Settings	Total Dynamic Power	and the local design of th			
B By Type	the second se	15.649			
- Clocks - Logic					
Signals					
-10s					
By Hierarchy					

(b) Power utilization of proposed MAC unit using modified vedic multiplier

Fig. 8: Synthesis result of conventional and modified MAC unit for power consumption

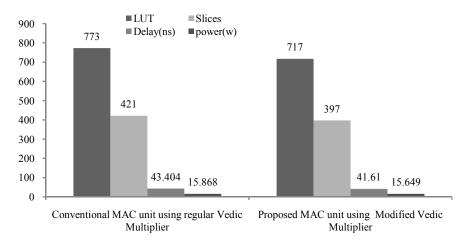


Fig. 9: Performance analysis of proposed modified MAC unit over existing MAC unit

Table 1. Campaniana of	S J: ff-mant MAC it in a		l ann dùn man ltim li ann
Table F. Comparison of	f different MAC unit using	тершаг апа тоатпес	i veaic muniphers
ruote r. companioon or	anne abine	, regular and mounted	i veare manuphers

Туре	LUT	Slices	Delay (ns)	Power (w)
Conventional MAC unit using regular vedic multiplier	773	421	43.404	15.858
Proposed MAC unit using modified vedic multiplier	717	397	41.610	15.649

regular Vedic multiplier consists of 773 LUTs and proposed MAC with modified Vedic multiplier consists of 717 LUTs. Conventional MAC with regular Vedic multiplier consumes 15.858 w of power and proposed MAC with modified Vedic multiplier consumes 15.649 w of power. The number of occupied slices of existing MAC unit is 421 and of proposed MAC unit is 397 (Fig. 9).

Modified Vedic multiplier is shown in Fig. 3. It is used give the exact result, when the carry output is 1. Instead of 16 bit ripple carry adder (32 half adder), 8 half adder and one full adder is used in modified Vedic multiplier to reduce the area and delay than the conventional Vedic multiplier. So 22 half adder is reduced in the modified full adder and also when 15×11 , it gives 165. This fault also rectifies using half adders (Table 1).

CONCLUSION

An efficient multiplier called modified Vedic multiplier has been proposed for MAC unit. The proposed multiplier provides low area and less delay by use of less number of full adder and half adder instead of ripple carry adder. In this study, hardware design and implementation of Field Programmable Gate Array based Multiplication and Accumulation (MAC) unit with modified Vedic multipliers is presented. The design was implemented on Xilinx Spartan 3 XC3S50 FPGA device. Comparative study of an efficient MAC unit with regular Vedic multiplier and modified Vedic multiplier was done. The Modified Vedic multiplier as compared to regular Vedic shows much more reduction in device Utilization. The proposed method offers 10% area, 10% delay and 5% power reduction than the existing architecture. Hence it is concluded that, modified Vedic multiplier based MAC unit provides an efficient method for reducing the power dissipation, delay and area. In future, the proposed MAC unit can be used in the digital FIR filter.

REFERENCES

Bansal, Y., C. Madhu and P. Kaur, 2014. High speed Vedic multiplier designs-A review. Proceeding of 2014 Recent Advances in Engineering and Computational Sciences (RAECS), pp: 1-6.

- Cieplucha, M., 2013. High performance FPGA-based implementation of a parallel multiplieraccumulator. Proceeding of 20th International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES), pp: 485-489.
- Deepak, S. and B.J. Kailath, 2012. Optimized MAC unit design. Proceeding of IEEE International Conference on Electron Devices and Solid State Circuit (EDSSC, 2012), pp: 1-4.
- Huddar, S.R., S.R. Rupanagudi, M. Kalpana and S. Mohan, 2013. Novel high speed Vedic mathematics multiplier using compressors. Proceeding of International on Multi-Conference Automation, Computing, Communication, Control and Compressed Sensing (iMac4s), pp: 465-469.
- Itawadiya, A.K., R. Mahle, V. Patel and D. Kumar, 2013. Design a DSP operations using Vedic mathematics. Proceeding of International Conference on Communications and Signal Processing (ICCSP, 2013), pp: 897-902.
- Jaina, D., K. Sethi and R. Panda, 2011. Vedic mathematics based multiply accumulate unit. Proceeding of International Conference on Computational Intelligence and Communication Networks (CICN, 2011), pp: 754-757.
- Kunchigi, V., L. Kulkarni and S. Kulkarni, 2012. High speed and area efficient Vedic multiplier. Proceeding of International Conference on Devices, Circuits and Systems (ICDCS, 2012), pp: 360-364.
- Shams, A.M., W.M. Badawy and M.A. Bayoumi, 1998. An enhanced low-power computational kernel for a pipelined multiplier-accumulator unit. Proceeding of the 10th International Conference on Microelectronics (ICM '98), pp: 33-36.
- Shanthala, S., C.P. Raj and S.Y. Kulkarni, 2009. Design and VLSI implementation of pipelined multiply accumulate unit. Proceeding of 2nd International Conference on Emerging Trends in Engineering and Technology (ICETET, 2009), pp: 381-386.