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Harmonic Reduction in Five Level Inverter Based Dynamic Voltage Restorer

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Abstract: This study deals with harmonic reduction in the five level inverter based Dynamic Voltage Restorer(DVR). The control of DVR that injects a voltage in series with a distribution feeder is presented. DVR is a power electronic controller that can protect sensitive loads from disturbances in supply system. DVR can regulate the voltage at the load. The simulation results of five level inverter based DVR are presented. The spectrum for the output voltage is also presented.

Key words: DVR, five level inverter, MATLAB, simulink, series compensation

INTRODUCTION

The Fig. 1 shows the series connection of a Dynamic Voltage Restorer (DVR) between the utility source and loads, through a coupling transformer. During normal operating conditions, the DVR can be switched offline (Li *et al*., 2002) or controlled to compensate for any injected harmonic voltages in the utility grid (Newman *et al*., 2003). Upon the occurrence of a voltage sag (decrease in v_{PCC}), the DVR is commanded to inject a voltage v_o such that the magnitude of v_L (= v_{PCC} + v_o) remains essentially constant throughout the sag period. However, the phase of v_L can either be shifted or remain unchanged, depending on the compensation techniques adopted.

Conventionally, the series voltage v_o is injected through a coupling transformer, whose main functions are to provide voltage boosting (v_o/v_o' > 1) and electrical isolation between the phases. Usage of a transformer, however, has the disadvantage of making the DVR bulky and costly, the other disadvantages, as summarized in (Li *et al*., 2002). To overcome these disadvantages, (Li *et al*., 2002) has proposed the series/parallel connection of semiconductor switches, or H-bridges, to develop high voltage DVR (HVDVR), which can be connected directly to the utility grid without a coupling transformer.

This study begins by analyzing different topological possibilities for implementing the HVDVR with the main aim of designing a reliable custom power conditioner. The next letter next presents an open-loop control scheme with Posicast compensator (Hung, 2003) incorporated for damping transient voltage oscillations at the instant of voltage injection (an issue which has not been actively investigated for DVR).

The Posicast-based open-loop control is subsequently improved by adding a parallel multifeedback-loop control path to give two-degrees-of-freedom in control tuning. This feedback path uses the P+resonant compensator (Zmood *et al*., 2001) to force the steady-state voltage error to zero, hence, enhancing the DVR load voltage regulation performance. All principles presented have been verified in Matlab/Simulink simulation using a cascaded five-level and a binary seven-level inverter. The Cascaded multilevel H-bridge inverter utilizing capacitor voltage sources is given (Corzine *et al*., 2003). Active Harmonic elimination for Multilevel Inverters is given (Du *et al*., 2006). A survey of topologies, controls and applications of multilevel inverters is given (Lai *et al*., 2002). Reduced common mode modulation Strategies for cascaded multilevel inverters is given (Loh *et al*., 2003). The objective of this study is to reduce the harmonics using five level inverter.

CASCADED H-BRIDGE MULTI-LEVEL BOOST INVERTER WITHOUT INDUCTORS

The five level inverter is shown in Fig. 2. To see how the system works, a simplified single phase topology is shown in Fig. 3. The output voltage v_1 of this leg of the bottom inverter (with respect to the ground) is either $+V_{dc}/2$ (S_5 closed) or $-V_{dc}/2$ (S_6 closed). This leg is connected in series with a full H-bridge, which, in turn, is supplied by a capacitor voltage. If the capacitor is kept charged to $V_{dc}/2$, then the output voltage of the H-bridge can take on the values $+V_{dc}/2$ (S_1 and S_4 closed), 0 (S_1 and S_2 closed or S_3 and S_4 closed), or $-V_{dc}/2$ (S_2 and S_3 closed). An example output waveform from this topology is shown in Fig. 4a. When the output voltage $v = v_1 + v_2$ is required to be zero, one can either set $v_1 = +V_{dc}/2$ and $v_2 = -V_{dc}/2$ or $v_1 = -V_{dc}/2$ and $v_2 = +V_{dc}/2$.

Additional capacitor's voltage regulation control detail is shown in Fig. 4. To explain how the capacitor is kept charged, consider the interval $\theta \leq \theta \leq \Pi$, the output

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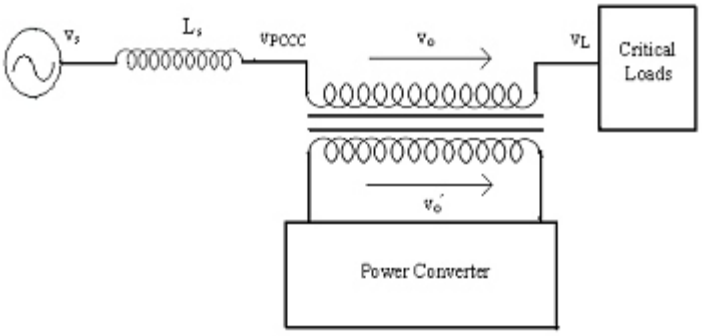

Fig. 1: System configuration with dynamic voltage restoration

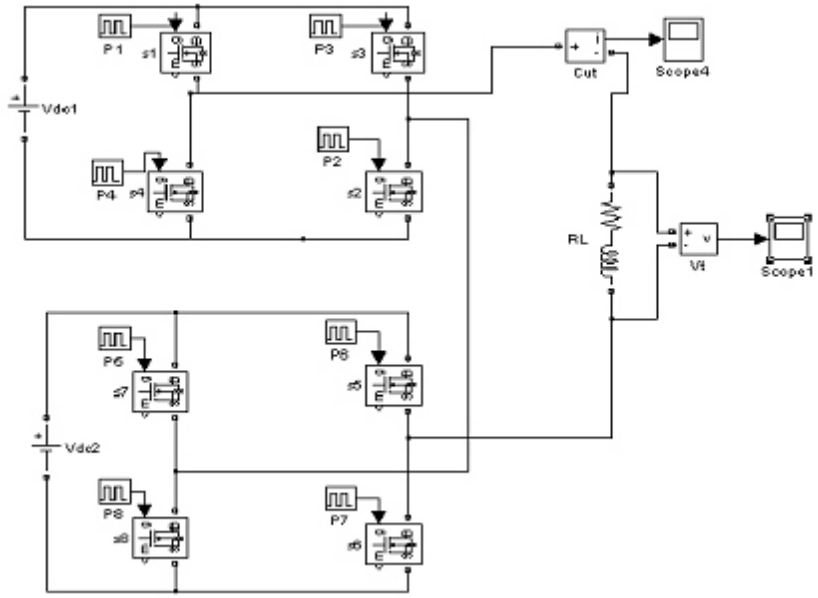

Fig. 2: Five level inverter

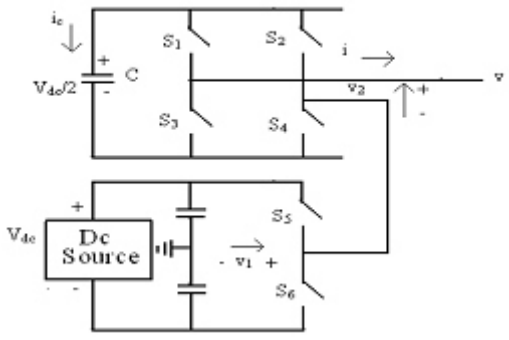

Fig. 3: Single phase of the proposed dc-ac cascaded H-bridge multilevel boost inverter

voltage in Fig. 4a is zero, and t.he current $i > 0$. If S_1 and S_4 are closed (so that $v_2 = +V_{dc}/2$) and S_6 is closed (so that $v_1 = -V_{dc}/2$), then the capacitor is discharging [$i_c = -i < 0$; Fig. 4b], and $v = v_1 + v_2 = 0$. On the other hand, if S_2 and

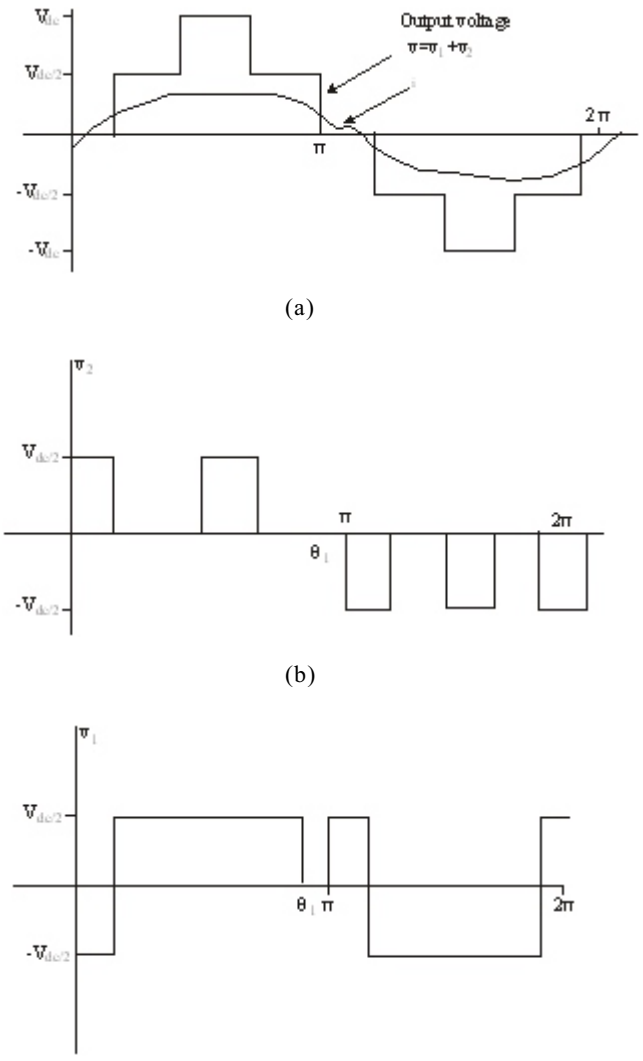

Fig. 4: Capacitor voltage regulation with capacitor charging and discharging (a) Overall output voltage and load current (b) Output of Inverter 1 and (c) Output of Inverter 2

S_3 are closed (so that $v_2 = -V_{dc}/2$) and S_5 is also closed (so that $v_1 = +V_{dc}/2$), then the capacitor is charging [$i_c = i > 0$; Fig. 4c], and $v = v_1 + v_2 = 0$. The case $i < 0$ is accomplished by simply reversing the switch positions of the $i > 0$ case for charging and discharging of the capacitor. Consequently, the method consists of monitoring the output current and the capacitor voltage, so that during periods of zero voltage output, either the switches S_1, S_4 and S_6 are closed or the switches S_2, S_3 and S_5 are closed, depending on whether it is necessary to charge or discharge the capacitor. It is this flexibility in choosing how to make the output voltage zero is exploited to regulate the capacitor voltage.

The goal of using fundamental frequency switching modulation control is to output a five-level voltage waveform, with a sinusoidal load current waveform, as shown in Fig. 4a. If the capacitor's voltage is higher than $V_{dc}/2$, switches S_5 and S_6 are used to control the output voltage waveform, v_1, and the switches S_1, S_2, S_3 and S_4 are used to control the output voltage waveform v_2, shown in Fig. 4b. The highlighted part of the waveform in Fig. 4b is the capacitor discharging period, during which the inverter's output voltage is 0V.

If the capacitor's voltage is lower than $V_{dc}/2$, the switches S_5 and S_6 are controlled to obtain output voltage waveform v_1, and switches S_1, S_2, S_3 and S_4 are controlled to obtain output voltage waveform v_2. Therefore, the capacitors' voltage can be regulated by alternating the capacitor's charging and discharging control, when the inverter output is 0V.

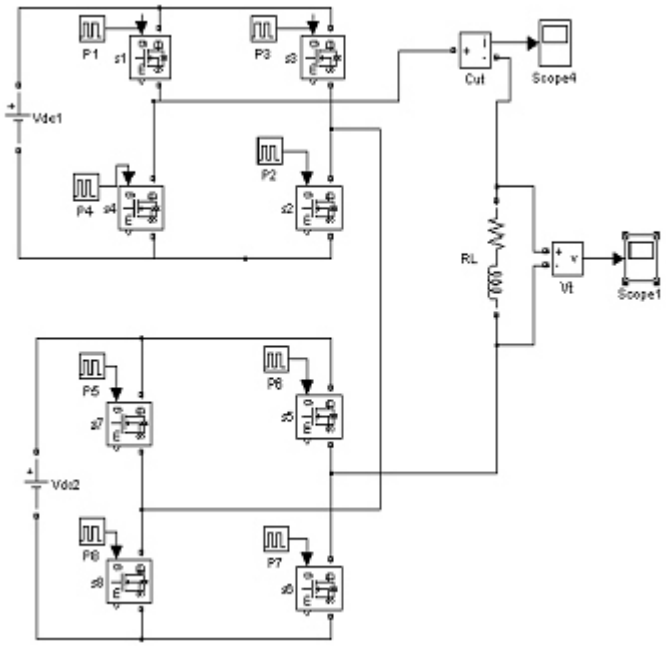

Fig. 5a: Five level inverter with RL load

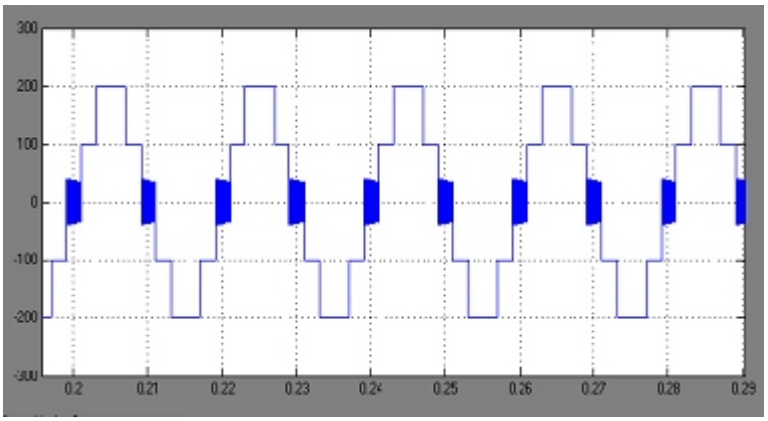

Fig. 5b: Output voltage of five level inverter

This method of regulating the capacitor voltage depends on the voltage and current not being in phase. That is, one needs positive (or negative) current when the voltage is passing through zero in order to charge or discharge the capacitor. Consequently, the amount of capacitor voltage the scheme can regulate depends on the phase angle difference of output voltage and current. In other words, the highest output Ac voltage of the inverter depends on the displacement power factor of the load. The above literature does not deal with five level inverter based DVR. This study presents the concept of five level inverter based DVR.

SIMULATION RESULTS

Digital simulation is done using the blocks of Matlab simulink and the results are presented here. Five level inverter system with RL load is shown in Fig. 5a. The transmission system is modelled by using series impedance model. The shunt capacitance is neglected. The five level inverter output voltage is shown in Fig. 5b.The five level inverter output current is shown in Fig. 5c. DVR using five level inverter is shown in Fig. 6a. The voltage across external, load-1 and load-2 are shown in Fig. 6b. The RMS voltage is shown in Fig. 6c.The RMS

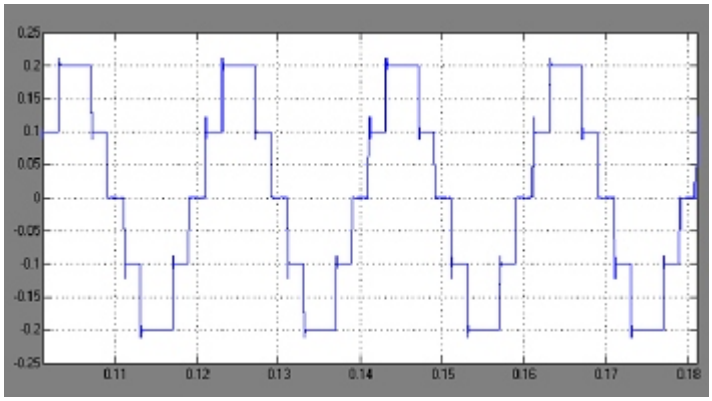

Fig. 5c: Output current of five level inverter

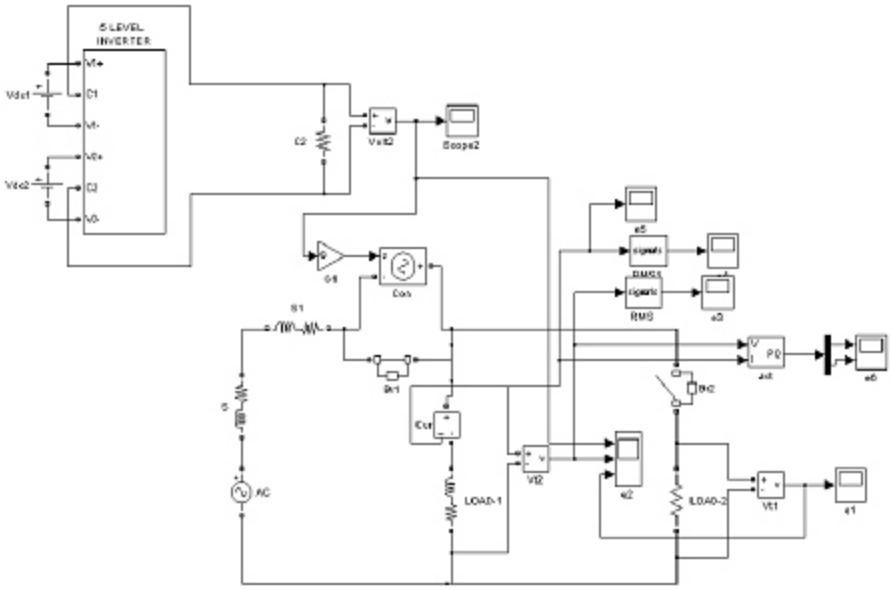

Fig. 6a: DVR without LC filter

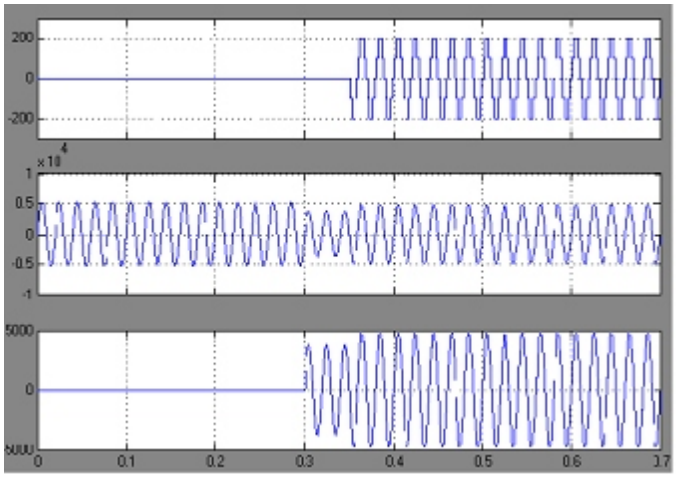

Fig. 6b: Voltage across external,load-1and load-2

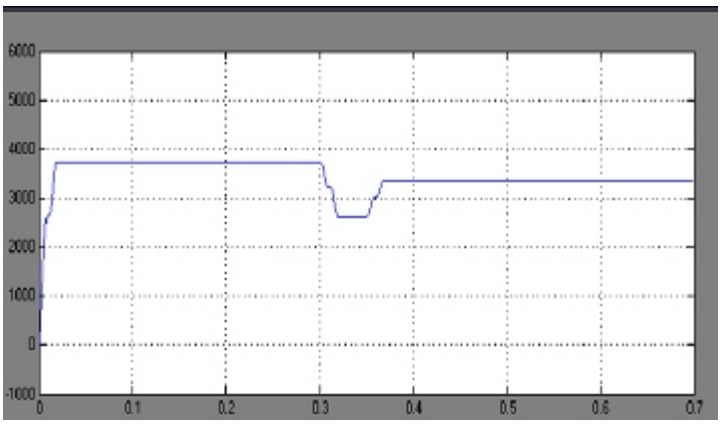

Fig. 6c: RMS voltage

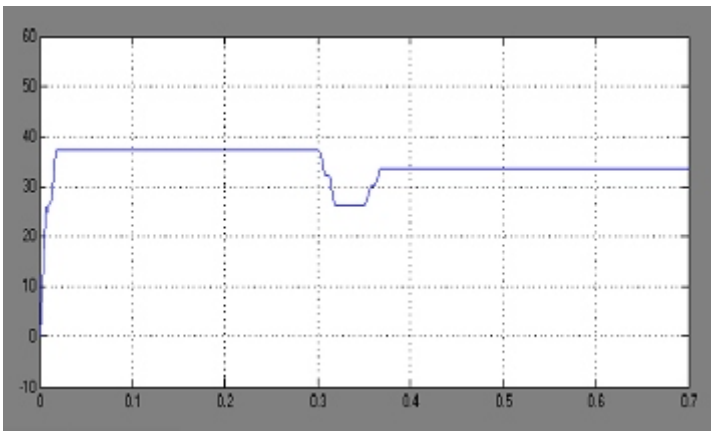

Fig. 6d: RMS load current

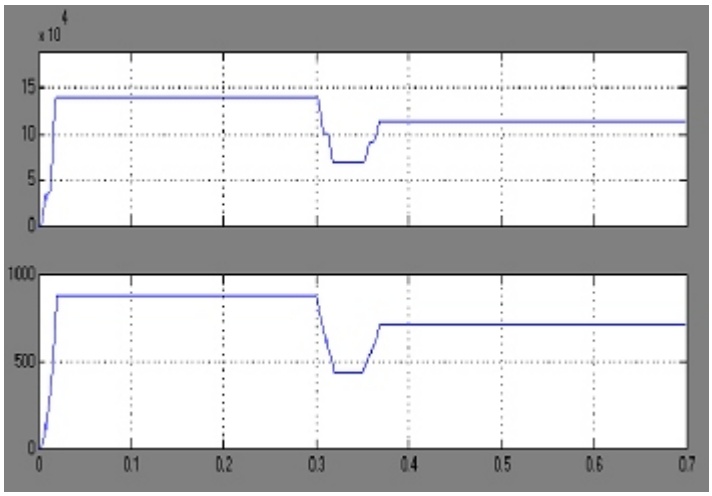

Fig. 6e: Real and reactive powers

load current is shown in Fig. 6d. The real and reactive powers are shown in Fig. 6e. FFT analysis for the output voltage is shown in Fig. 6f. The THD value is 3.65%.

DVR system with LC filter is shown in Fig. 7a. The voltage across external, load-1 and load-2 are shown in Fig. 7b. The RMS voltage is shown in Fig. 7c.The RMS

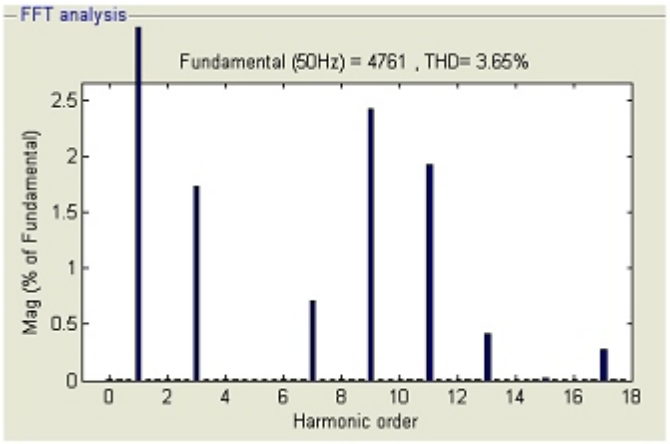

Fig. 6f: FFT analysis for voltage

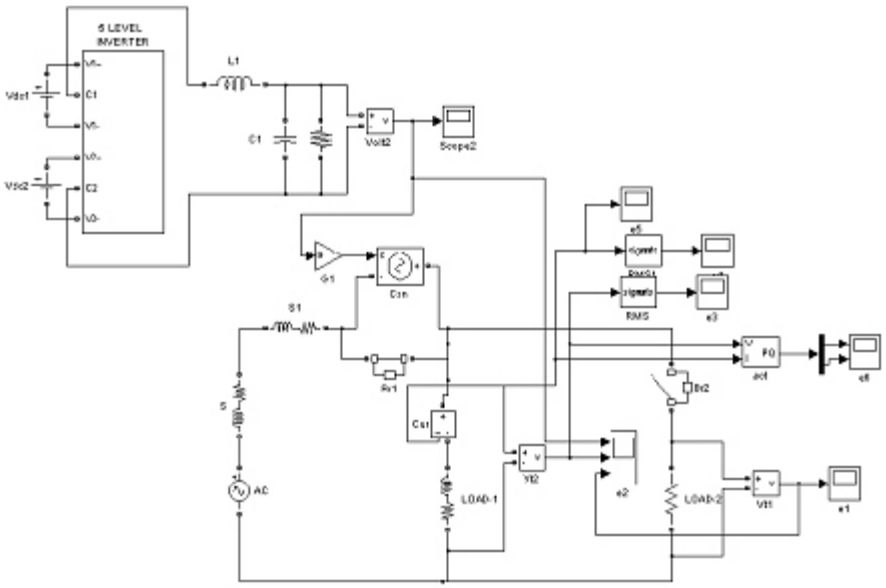

Fig. 7a: DVR with LC filter

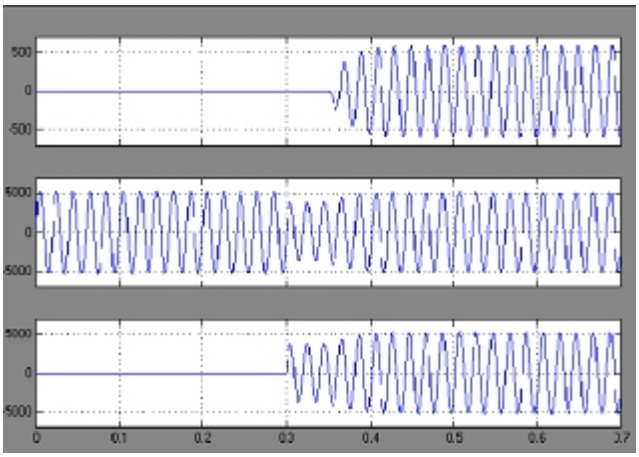

Fig. 7b: Voltage across external,load-1 and load-2

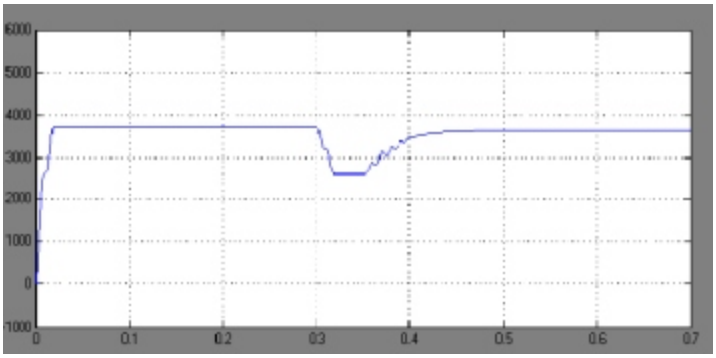

Fig. 7c: RMS voltage

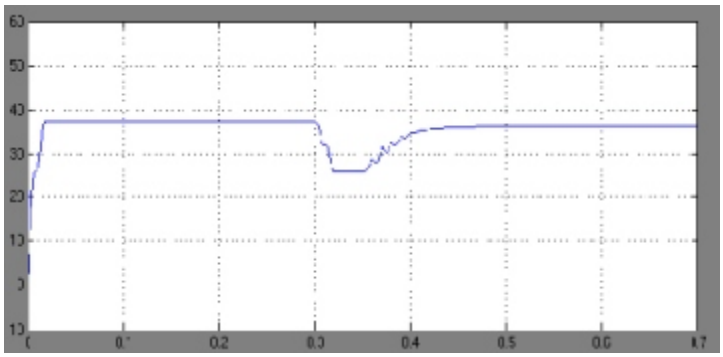

Fig. 7d: RMS load current

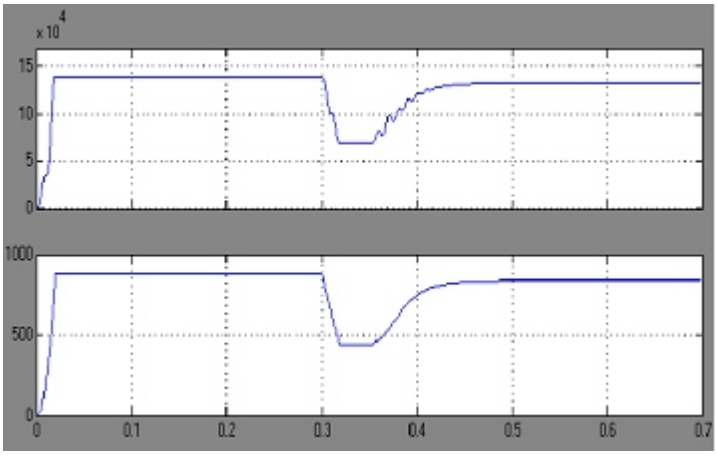

Fig. 7e: Real and reactive powers

load current is shown in Fig. 7d. The real and reactive powers are shown in Fig. 7e. FFT analysis for the output voltage is shown in Fig. 7f. The THD reduces to 0.72%. Thus the harmonics are reduced from 3.65 to 0.72%. The harmonic reduction indicates that the simulation results are in line with the predictions.

CONCLUSION

This study presents circuit modelling and simulation of DVR using cascaded five level inverter. This study demonstrates the capability of DVR to improve the voltage quality. DVR structure is studied and the

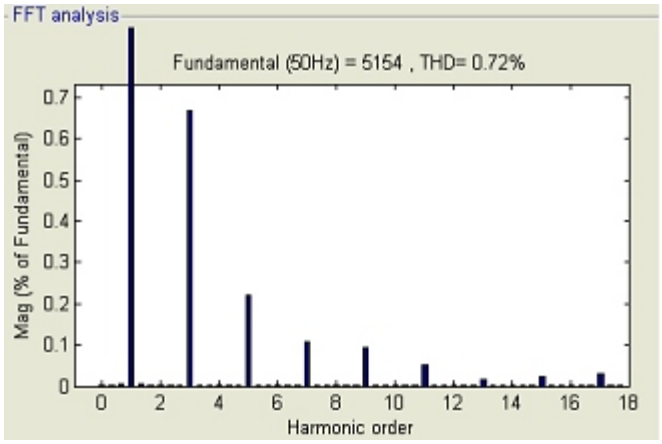

Fig. 7f: FFT analysis for inverter output

corresponding results are presented. The heating is reduced since the harmonics in the output of cascaded inverter are less. The simulation is based on the assumption of balanced load and single phase circuit model. The simulation results are in line with the predictions. Five level inverter is a viable alternative since it has reduced harmonics.

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