

Simulation and Experimental Results of 7-Level Inverter System

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Abstract: This study deals with the simulation and experimentation of 7-level inverter. This study presents 7-level inverter with harmonics reduction along with the reduction in number of switches. The percentage (%) total harmonic distortion is calculated for 7-level inverter. The harmonic reduction is achieved by selecting appropriate switching angles. The functionality verification of the 7-level inverter is done using MATLAB. The result of simulation is verified by experimentation.

Key words: Cascaded multilevel inverter, 7-level inverter

INTRODUCTION

The multi level inverter was first introduced in 1975. The 3-level converters was the first multilevel inverter introduced. A multilevel converter is a power electronic system that synthesizes a desired output voltage from several levels of dc voltages as inputs. With an increasing number of dc voltage sources, the converter output voltage waveform approaches a nearly sinusoidal waveform while using a fundamental frequency-switching scheme. The primary advantage of multilevel inverter is their small output voltage, results in higher output quality, lower harmonic component, better electro magnetic computability, and lower switching losses (Chiasson *et al.*, 2004; Rodriguez *et al.*, 2002).

Multilevel inverter consists of an array of power semiconductor switches, capacitor voltage sources and clamping diodes. The multilevel inverter produces the stepped voltage waveforms with less distortion, less switching frequency, higher efficiency, lower voltage devices and better electromagnetic compatibility (Agelidis and Calais, 1998; Nabae *et al.*, 1981; Ziogas, 1980). The commutation (process of turn-off) of the switches permits the addition of the capacitor voltages, which reach high voltages at the output (in the output terminal of multilevel inverter) (Patel and Hoft, 1974).

METHODOLOGY

H-bridge inverter: Another characteristic is that the “H” topology has many redundant combinations of switches’ positions to produce the same voltage levels. As an example, the level “zero” can be generated with switches in position $S_{(1)}$ and $S_{(2)}$, or $S_{(3)}$ and $S_{(4)}$, or $S_{(5)}$ and $S_{(6)}$, and so on (Babaei *et al.*, 2007; Manjrekar *et al.*, 2000; Du *et al.*, 2006). Another characteristic of “H” converters is that

they only produce an odd number of levels, which ensures the existence of the “0V” level at the load. For example, a 51-level inverter using an “H” configuration with transistor-clamped topology requires 52 transistors, but only 25 power supplies instead of the 50 required when using a single leg (Manjrekar *et al.*, 2000). Therefore, the problem related to increasing the number of levels and reducing the size and complexity has been partially solved, since power supplies have been reduced to 50%.

Figure 1 shows the single-phase H-bridge of cascaded inverter. The ac terminal voltages of each bridge are connected in series. Unlike the diode clamp or flying capacitors inverter, the cascaded inverter does not require any voltage-clamping diodes or voltage balancing capacitors. This configuration is useful for constant frequency applications such as active front-end rectifiers, active power filters, and reactive power compensation.

In this case, the power supply could also be voltage regulated dc capacitor. The circuit diagram consists of two cascade bridges. The load is connected in such a way that the sum of output of these bridges will appear across it. The ratio of the power supplies between the auxiliary bridge and the main bridge is 1:2. One important characteristic of multilevel converters using voltage escalation is that electric power distribution and switching frequency present advantages for the implementation of these topologies (Du *et al.*, 2006).

Using H-bridge inverter the harmonics was reduced in 3 and 7-level output voltages. The inverter generates a high quality output voltage waveform. It reduces dv/dt stress imposed on power switching devices and also harmonic components of output voltage and load current quite well.

The phase output voltage is synthesized by the sum of two inverter outputs. Each inverter bridge is capable of generating three different levels of voltage outputs. The main bridge can generate $+2V_{dc}$, 0 , $-2V_{dc}$ and the auxiliary

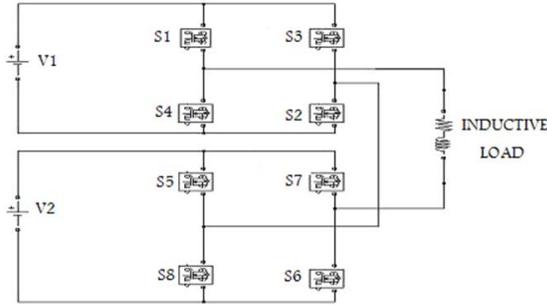


Fig. 1: H-bridge inverter

Table 1: Switching sequence of H-bridge inverter

Voltage level	S ₁	S ₂	S ₃	S ₄	S ₅	S ₆	S ₇	S ₈
-3V _{dc}	0	0	1	1	0	0	1	1
-2V _{dc}	0	0	1	1	1	1	0	0
-1V _{dc}	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	0
+1V _{dc}	0	0	0	0	1	1	0	0
+2V _{dc}	1	1	0	0	0	0	1	1
+3V _{dc}	1	1	0	0	1	1	0	0

bridge can generate +V_{dc}, 0, -V_{dc}. By using appropriate combinations of switching devices many voltage levels are obtained. When the positive group switches are turned on the voltage across that particular bridge is positive. When the negative group switches are turned on the voltage across that particular bridge is negative. When S₅, S₆ are turned on the voltage across the main bridge is +2V_{dc}.

When S₇, S₈ are turned on the voltage across the main bridge is -2V_{dc}. When S₁, S₂ are turned on the voltage across the auxiliary bridge is +V_{dc}. When S₃, S₄ are turned on the voltage across the auxiliary bridge is -V_{dc}. To obtain +2V_{dc} the switch combinations S₁, S₂, S₇ and S₈ are turned on. To obtain +3V_{dc} the switch combinations S₁, S₂, S₅ and S₆ are turned on. To obtain -2V_{dc} the switch combinations S₃, S₄, S₅ and S₆ are turned on. To obtain -3V_{dc} the switch combinations S₃, S₄, S₇ and S₈ are turned on. The Table 1 shows the switching strategy of transistors at each level. The status of the switch is ‘0’, that switch is in OFF condition. The status of the switch is ‘1’, that switch is in ON condition.

Harmonic reduction: To eliminate 5th, 7th and 9th order harmonics, the firing angles for each level is found by solving the following equations:

$$\begin{aligned} \cos 5a_1 + \cos 5a_2 + \cos 5a_3 + \cos 5a_4 &= 0 \\ \cos 7a_1 + \cos 7a_2 + \cos 7a_3 + \cos 7a_4 &= 0 \\ \cos 9a_1 + \cos 9a_2 + \cos 9a_3 + \cos 9a_4 &= 0 \end{aligned}$$

Using Math CAD, the values of the “a” is obtained as follows:

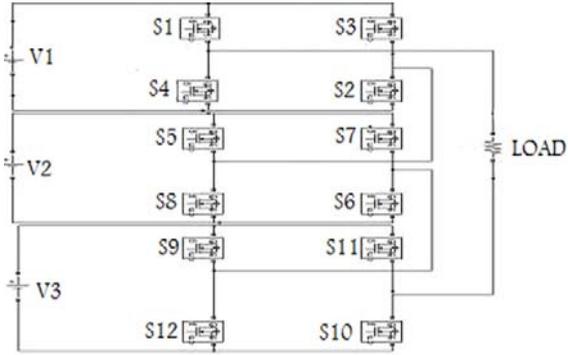


Fig. 2: H-bridge 7-level conventional inverter

Table 2: Switching sequence and output voltage levels

On switches	Node A voltage (V _A)	Node B voltage (V _B)	Output voltages (V _{AB})
Q ₃ , Q ₄	0	0	0
Q ₁ , Q ₄ , Q ₅	V _d	0	V _d
Q ₁ , Q ₄ , Q ₇	2V _d	0	2V _d
Q ₁ , Q ₄ , Q ₅ , Q ₇	3V _d	0	3V _d
Q ₁ , Q ₄ , Q ₇	2V _d	0	2V _d
Q ₁ , Q ₄ , Q ₅	V _d	0	V _d
Q ₁ , Q ₂	0	0	0
Q ₂ , Q ₃ , Q ₅	0	V _d	-V _d
Q ₂ , Q ₃ , Q ₇	0	2V _d	-2V _d
Q ₂ , Q ₃ , Q ₅ , Q ₇	0	3V _d	-3V _d
Q ₂ , Q ₃ , Q ₇	0	2V _d	-2V _d
Q ₂ , Q ₃ , Q ₅	0	V _d	-V _d

$$\begin{aligned} a_1 &= 12.834 \\ a_2 &= 29.908 \\ a_3 &= 50.993 \\ a_4 &= 64.229 \end{aligned}$$

where, a₁, a₂, a₃, a₄ are the firing angles in degrees. The switching instants are obtained by carrying out the above calculations.

The H-bridge 7-level conventional inverter is shown in the Fig. 2. The conventional 7-level inverter has some disadvantages they are requires 2(m-1) switching devices; increase the cost; large in size; controlling is complex. In order to over come the above draw backs the following model has been proposed.

The Fig. 3 shows the proposed 7-level inverter. The proposed inverter generates a high quality output voltage waveform. It reduces dv/dt stress imposed on power switching devices. The Table 2 shows the switching strategy of proposed H-bridge 7-level inverter at each level.

Simulation results of H-bridge Inverter: H-bridge 3-level inverter simulink circuit shown in Fig. 4a. The output of the H-bridge inverter is connected with inductive load. The H-bridge inverter converts the DC voltage into AC voltage in various steps. The switching strategy of the circuit is explained in the previous section.

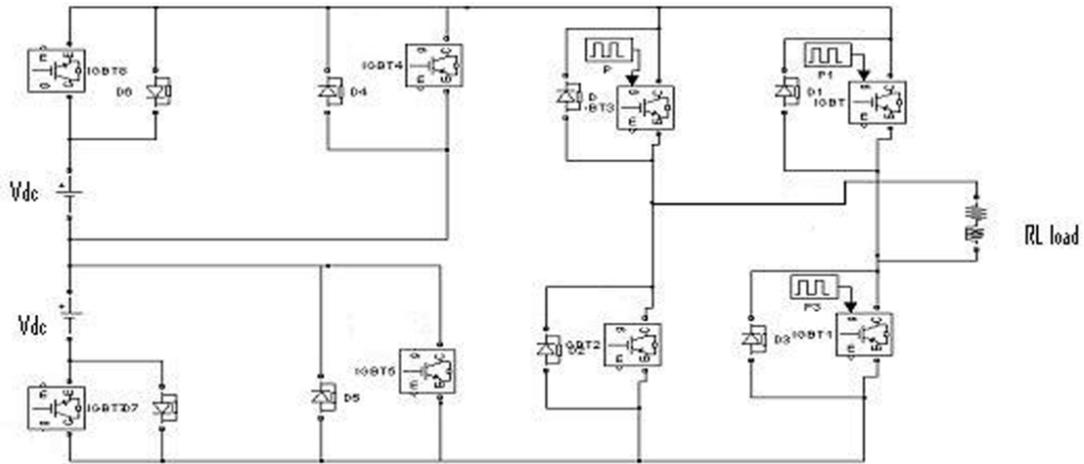


Fig. 3: Proposed H-bridge 7-level inverter

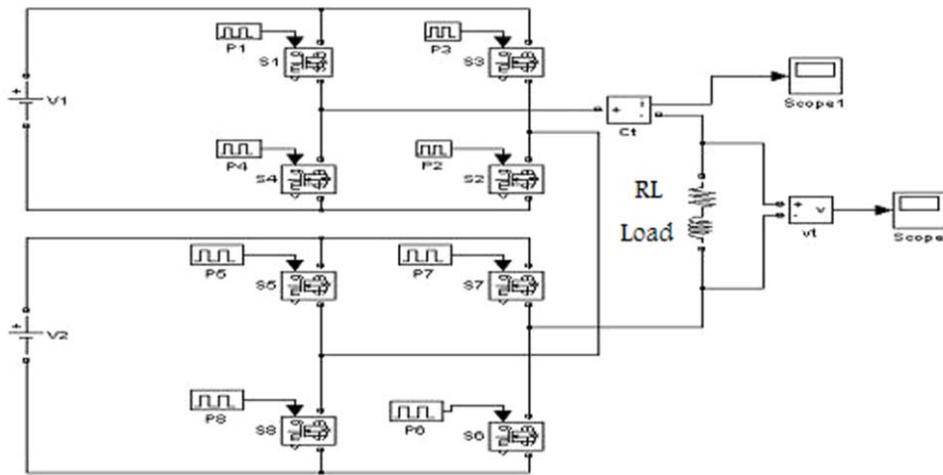


Fig. 4a: Simulink circuit for H-bridge 3-level inverter

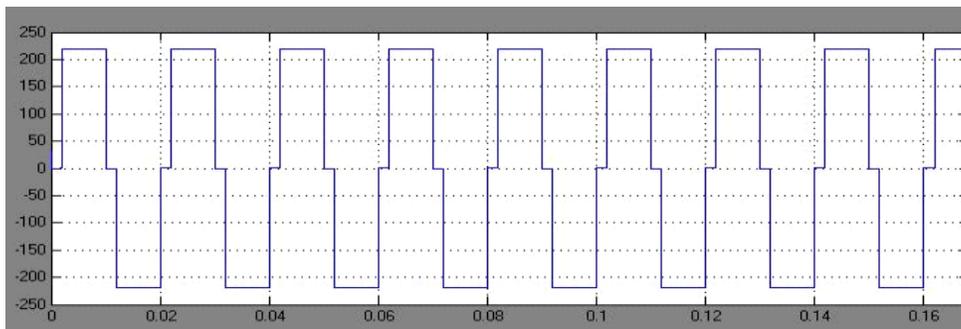


Fig. 4b: H-bridge 3-level inverter output voltage

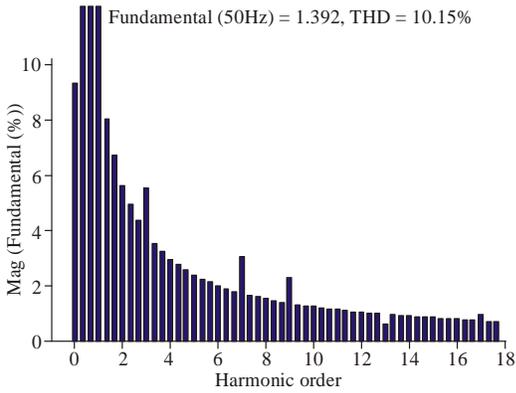


Fig. 4c: H-bridge 3-level inverter FFT analysis

This circuit is simulated in MATLAB and the harmonics are obtained using FFT analysis. The output waveform is shown in the Fig. 4b. Figure 4c shows the harmonics represent in the output. The THD value is 10.15%.

Conventional H-bridge 3-level inverter simulink circuit shown in Fig. 5a. The Conventional H-bridge inverter converts the DC voltage into AC voltage in various steps. The switching strategy of the circuit is explained in the previous section. This circuit is simulated in MATLAB and the harmonics are obtained by using FFT analysis. The output waveform is shown in the Fig. 5b. Figure 5c shows the harmonics present in the output THD value 8.73%.

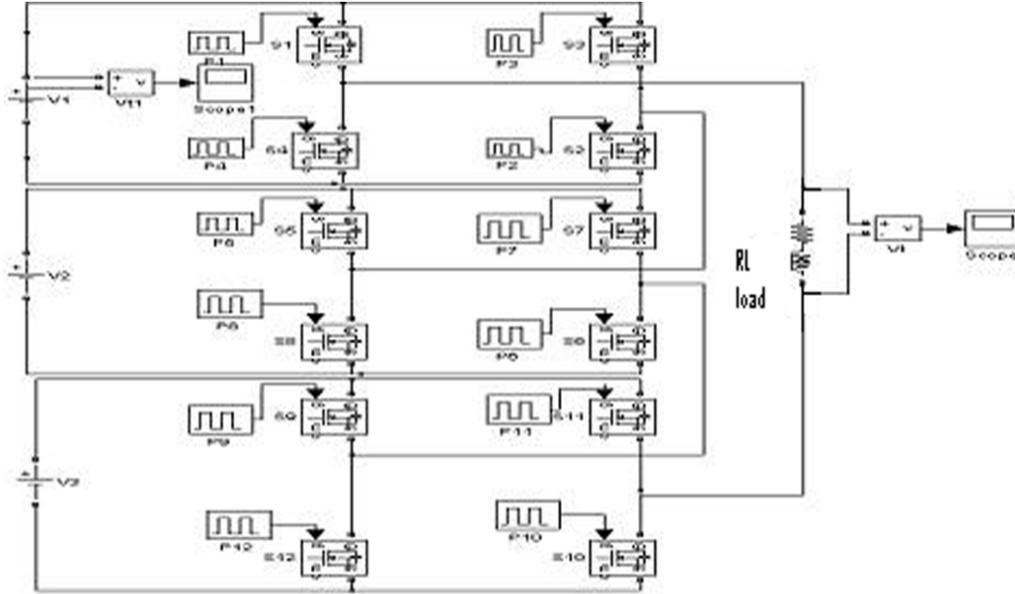


Fig. 5a: H-bridge 7-level conventional inverter

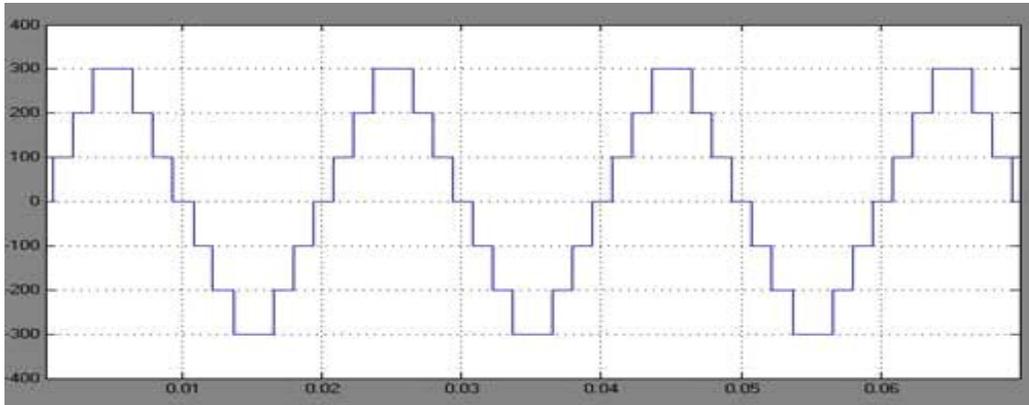


Fig. 5b: H-bridge 7-level conventional inverter output voltage

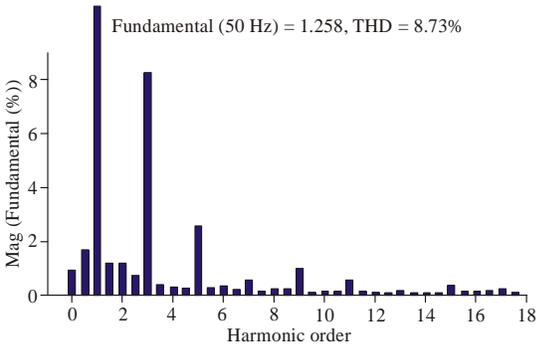


Fig. 5c: H-bridge 7-level conventional inverter FFT analysis

Proposed H-bridge 3-level inverter simulink circuit shown in Fig. 6a. The output of the proposed H-bridge inverter is considered with inductive load. The proposed H-bridge inverter converts the DC voltage into AC voltage in various steps. The switching strategy of the circuit is explained in the previous section. This circuit is simulated in MATLAB and the harmonics are obtained by using FFT analysis. The output waveform is shown in the Fig. 6b. Figure 6c shows the harmonics represent in the output. The THD value is 5.79%.

EXPERIMENTAL RESULTS

The hardware is fabricated and tested in the laboratory. Top view of the proposed 7-level inverter

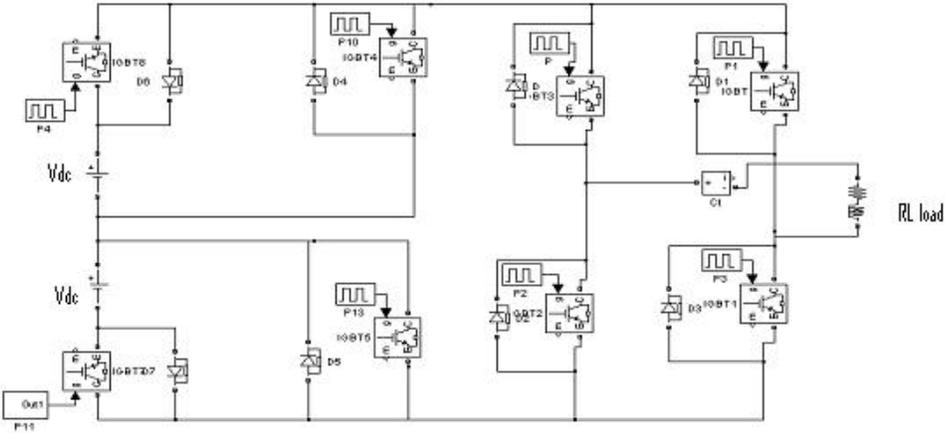


Fig. 6a: Simulink circuit for proposed H-bridge 7-level inverter

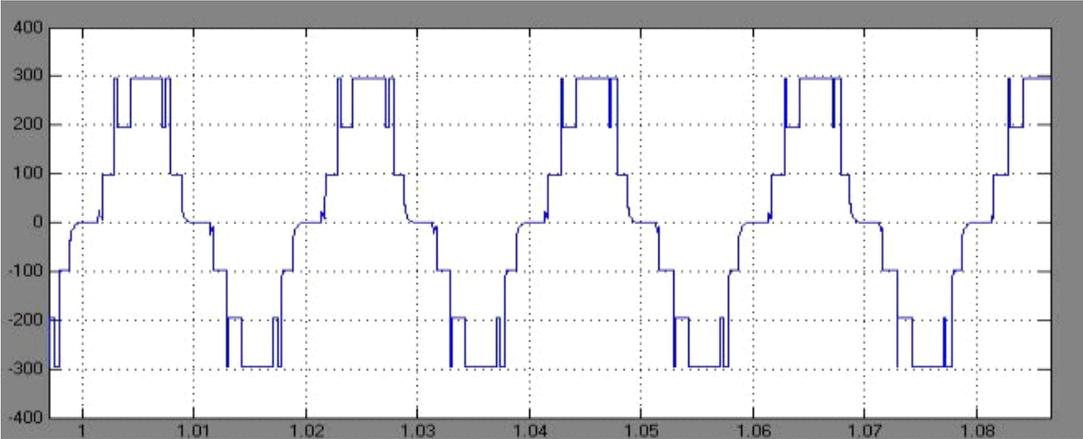


Fig. 6b: Proposed H-bridge 7-level inverter output voltage

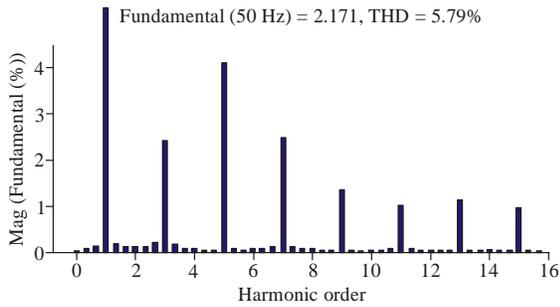


Fig. 6c: Proposed H-bridge 7-level inverter FFT analysis

Table 3: Comparison of harmonics in multilevel inverter

S.No.	Type of inverter	THD harmonics (%)
1	H-bridge 3-level inverter	10.15
2	H-bridge 7-level inverter	8.73
3	H-bridge proposed 7-level inverter	5.79

hardware is shown in Fig. 7a. The control circuit and power circuit of proposed 7-level inverter is shown in Fig. 7b and c, respectively. The hardware implementation and hardware output voltage of proposed 7-level inverter shown in Fig. 7d and e, respectively. The control circuits are used to generate the pulses for ON and OFF the switches. The microcontroller 89C2051 generates the

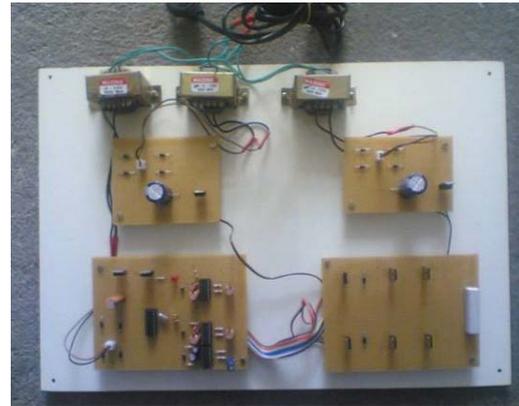


Fig. 7a: Proposed 7-level inverter hardware

pulses to ON the switches. The pulses are amplified by using the driver circuit.

It can be seen from the Table 3 that with the use of H-bridge 3-level inverter, there is a decrease in the %THD level to 10.15%. Further with the use of H-bridge 7 and 9-level inverter, the %THD are 8.73 and 7.30%, respectively. While using the proposed model the % THD level is reduced to 5.79%. This shows an improved performance of the H-bridge inverter.

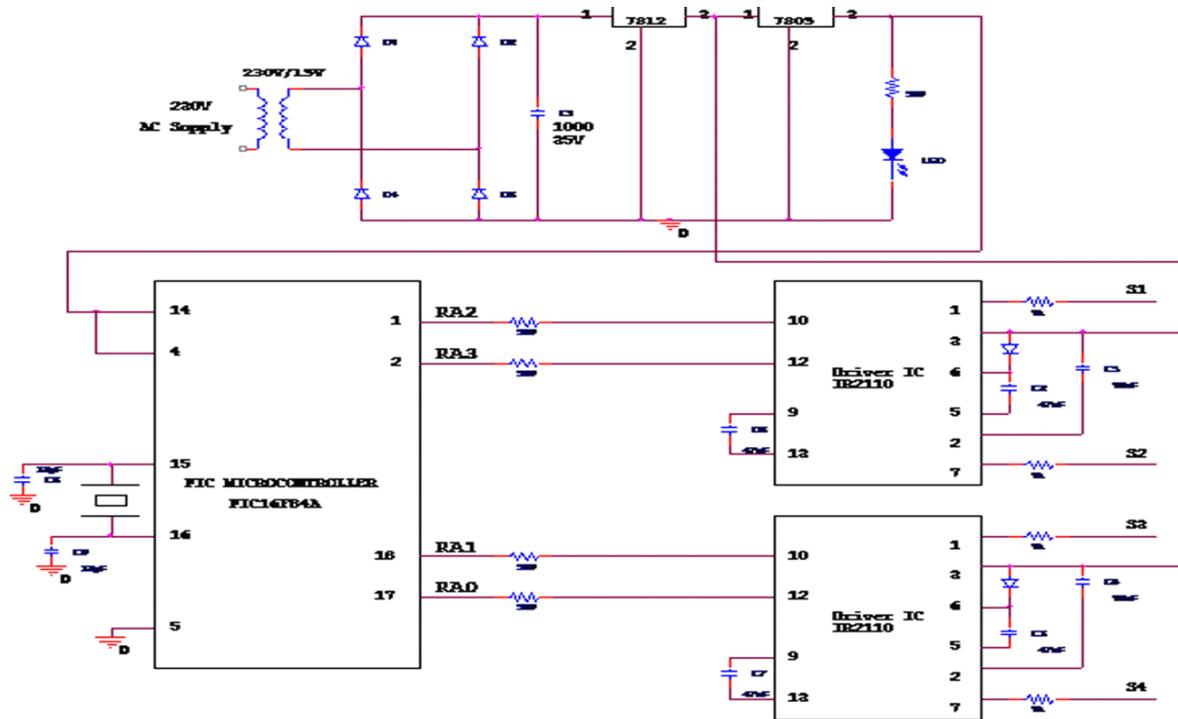


Fig. 7b: Control circuit of proposed 7-level inverter

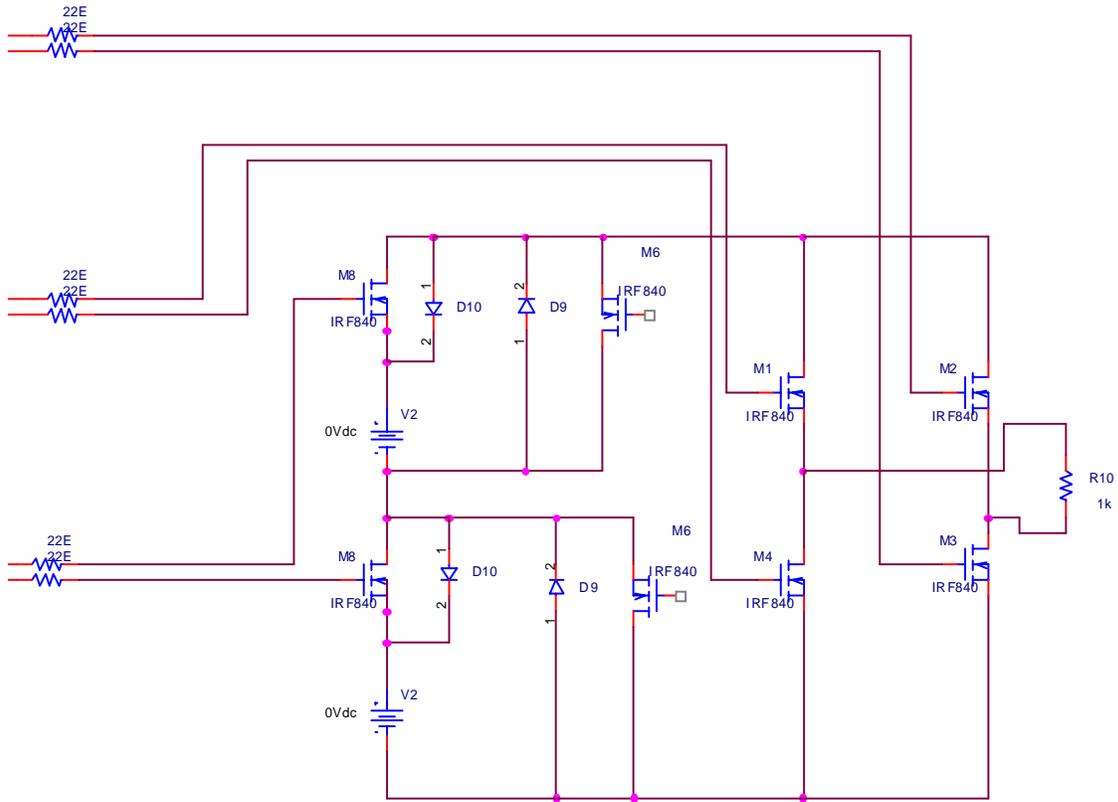


Fig: 7c: Power circuit of proposed 7-level inverter

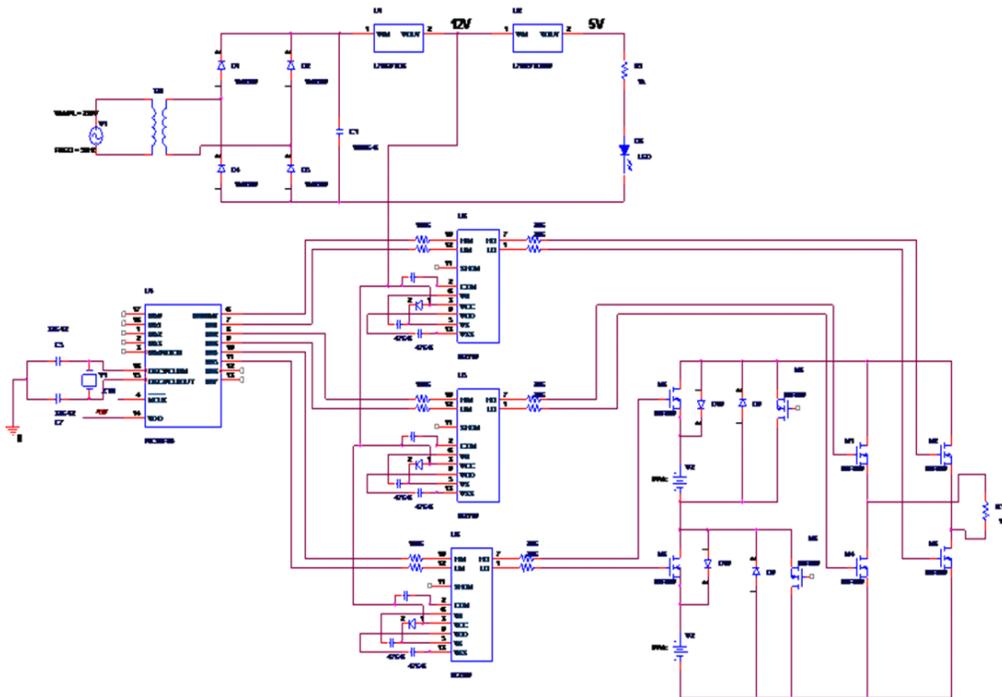


Fig: 7d: Hardware implementation of proposed 7-level inverter

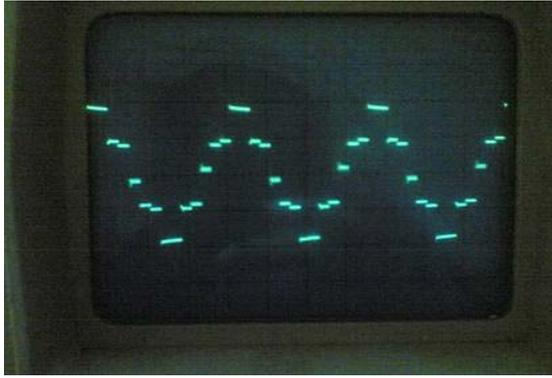


Fig: 7e: Hardware output of proposed 7-level inverter

CONCLUSION

H - bridge inverter has been simulated with reduced harmonics and implemented. Finally the harmonics in multilevel inverter at different stages are compared. From that comparison, it is seen that the 7-level inverter has least value of THD. The simulation results are in line with the prediction. The experimental results closely agree with the simulation results.

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