

Optimized Nanometric Fault Tolerant Reversible BCD Adder

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Abstract: In this study a novel nanometric fault tolerant quantum and reversible binary coded decimal adder is proposed. Reversible logic has found emerging attentions in optical information processing, quantum computing, nanotechnology and low power design. BCD Adder is a combinational circuit that can be used for the addition of two numbers in BCD arithmetic's. The proposed reversible BCD adder has also parity preserving property. It is better than all the existing counterparts. The proposed circuit is optimized. It is compared with the existing circuits in terms of number of constant inputs, number of garbage outputs, quantum cost and hardware complexity. All of the parameters are improved dramatically. It is to be noted that all the circuits have nanometric scales.

Key words: Binary coded decimal adder, fault tolerant, nanotechnology based systems, nanometric circuits, quantum computing, quantum circuits, quantum gates, reversible logic

INTRODUCTION

One of the important factors in the VLSI system design is power dissipation. Landauer (Landauer, 1961) proved that irreversible logic results in energy dissipation. It is due to loss of information. For every bit of information that is lost during a computation, these circuits dissipate energy in an order of $KTLn2$ Joules where $K=1.3806505 \times 10^{-23} \text{ m}^2/\text{kg}^{-2}\text{K}$ (Joules/Kelvin) is the Boltzmann's constant and T is the absolute temperature at which operation is performed (Bennett, 1973). Reversible logic circuits are those circuits that do not lose information because they allow the reproduction of inputs from the observed outputs. Reversible circuits have found promising attention in nanotechnology, quantum computing, low power CMOS circuit design and optical computing. Bennet showed that zero energy dissipation would be possible if and only if the circuit made of reversible gates. A circuit or a gate is reversible if and only if for each input vector there is a unique output vector. The input vector can be uniquely recovered from the output vector. That is, there is a one-to-one mapping between its input and output vectors. Such circuits allow the reproduction of the inputs from observed outputs and we can determine the inputs from the outputs (Haghparast *et al.*, 2009; Perkowski *et al.*, 2001; Perkowski and Kerntopf, 2001; Haghparast and Navi, 2011; Kerntopf *et al.*, 2004; Mohammadi *et al.*, 2009). Neither feedback nor fanout are allowed in reversible logic circuits. Thus

the synthesis of reversible logic circuits differs from the irreversible one (Gupta *et al.*, 2006). In the past decade some reversible logic circuit synthesis methods are proposed (Gupta *et al.*, 2006; Maslov *et al.*, 2003; Haghparast, 2011). In reversible logic for each input vector there should be a unique output vector. There are some important factors in designing reversible logic circuits such as the number of garbage outputs, the number of constant inputs, hardware complexity and the Quantum Cost (QC). We try to minimize them (Haghparast *et al.*, 2009; Mohammadi *et al.*, 2009; Gupta *et al.*, 2006; Maslov *et al.*, 2005; Haghparast and Navi, 2007; Haghparast and Navi, 2008; Haghparast and Navi, 2008b; Haghparast and Navi, 2008c).

Constant inputs are those inputs that are either set to zero (0) or one (1) and are constant. Garbage outputs refer to the outputs that are not used as primary outputs or as inputs to other gates. Hardware complexity refers to the number of gates (NOT, AND and EXOR gate) used to synthesize the function of the circuit. The quantum cost (QC) of a reversible circuit is defined as the number of 1×1 or 2×2 reversible or quantum logic gates that are needed to realize the circuit (Gupta *et al.*, 2006). For instance, the QC of Toffoli gate and F2G gate are 5 and 2, respectively.

In addition the design of fault tolerant reversible circuits are much more difficult than the design of conventional irreversible logic circuits (Haghparast and Navi, 2008b; Haghparast and Navi, 2008c).

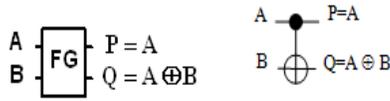


Fig. 1: Two symbols of feynman gate

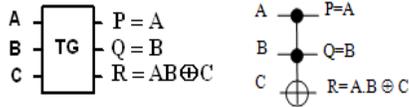


Fig. 2: Two symbols of Toffoli gate

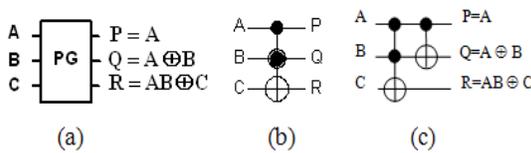


Fig. 3: Peres gate: (a) symbol and functionality, (b) The symbol used in this paper (c) equivalent circuit

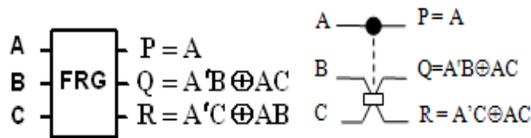


Fig. 4: Two symbols of parity preserving reversible fredkin gate

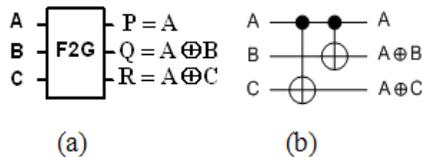


Fig. 5: Parity preserving reversible F2G gate (a) symbol and functionality, (b) its quantum equivalent

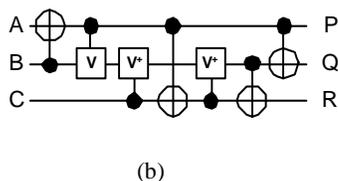
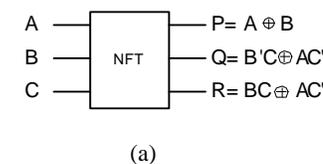


Fig. 6: Parity-preserving reversible NFT gate (a) symbol and functionality, (b) its quantum equivalent

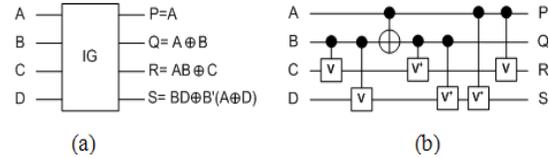


Fig. 7: Parity-preserving reversible IG gate (a) symbol and functionality, (b) its quantum equivalent (Haghparast and Navi, 2011)

If a system is made up of fault tolerant components, then it will be able to continue its operation properly when the failure occurs in some of its components (Haghparast and Navi, 2011). The detection and correction of faults in such fault tolerant systems are much easier. We can achieve fault tolerance in many systems by using parity bits. Thus, parity preserving reversible circuit design will be very important for development of fault tolerant reversible systems in nanotechnology which is an emerging technology (Haghparast and Navi, 2011; Islam and Begum, 2008; Haghparast, 2011).

In this study we propose an optimized nanometric fault tolerant reversible BCD adder. All the scales are in the nanometric area. This design is better than the all existing counterparts in the sense of above mentioned complexity factors.

Background: In this section we explain the basic concepts which are used in the paper. it includes some background information about reversible logic gates and circuits, fault tolerant reversible gates, existing fault tolerant reversible BCD adders and necessary blocks to construct our proposed design.

Reversible gates: We say that a gate or a circuit is reversible if and only if there is a one-to-one mapping between its inputs and outputs (Haghparast and Navi, 2007; Haghparast and Navi, 2008; Haghparast and Navi, 2008b; Haghparast and Navi, 2008c; Islam and Begum, 2008). Reversible logic gates can be implemented in various technologies such as CMOS logic, optical logic, quantum and nanotechnology..

There are many reversible logic gates such as Feynman gate (Feynman, 1985), Toffoli gate (Toffoli, 1980), Peres gate (Peres, 1985), etc. Feynman (Feynman, 1985) gate is a 2*2 reversible gate which is shown in Fig. 1. Its QC is 1. Reversible 3*3 Toffoli (Toffoli, 1980) gate which is depicted in Fig. 2 is universal, i.e. any logical reversible circuit can be implemented sing this gates. Its QC is only 5.

Peres (Peres, 1985) gate, also known as New Toffoli gate (NTG), is also a 3*3 reversible gate which can be

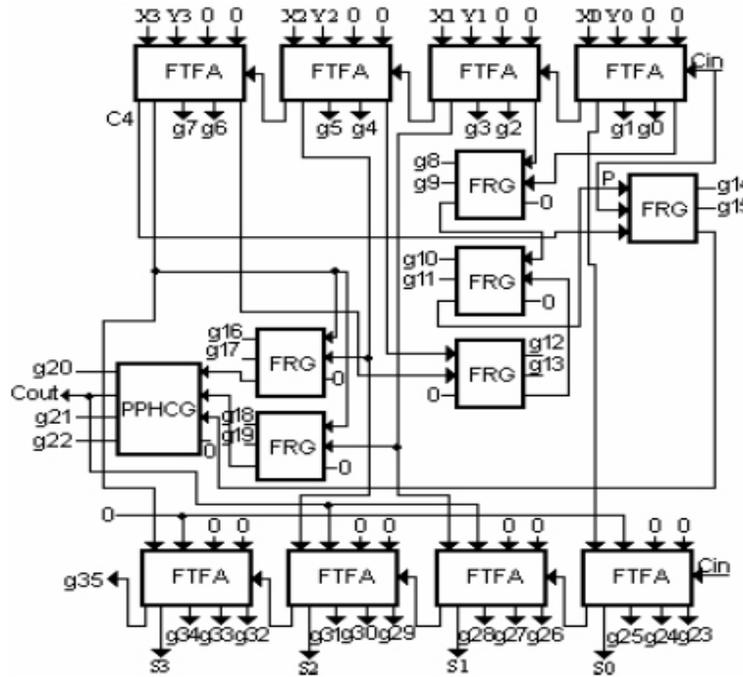


Fig. 8: Existing fault tolerant reversible BCD adder in (Islam and Begum, 2008)

constructed by one Toffoli and one Feynman gate. The Peres gate is shown in Fig. 3. Its QC is only 4.

Parity preserving reversible gates and circuits: Those reversible logic gates (or circuits) which have the equal input parity and output parity are called “parity preserving”. It means that the input parity and the corresponding output parity are the same. Most of arithmetic and other processing functions do not preserve the parity of the data. Parity checking is one of the most widely used methods for error detection in digital logic systems (Haghparast and Navi, 2011; Haghparast and Navi, 2008b; Haghparast and Navi, 2008c). Therefore it is important to construct parity preserving reversible gates and circuits.

There exist a few parity-preserving reversible gates such as Fredkin gate (FRG) (Fredkin and Toffoli, 1982) which is depicted in Fig. 4, Feynman double gate (F2G) (Parhami, 2006) which is depicted in Fig. 5, New Fault Tolerant Gate (NFT) (Haghparast and Navi, 2008b) which is depicted in Fig. 6. The above mentioned parity preserving reversible gates are 3*3 reversible gates. These gates are parity preserving gates because their input parity $A\bar{A}B\bar{A}C$ is the same as their output parity $PQ\bar{A}R$.

Fredkin (Fredkin and Toffoli, 1982) gate is a 3×3 reversible gate. It is a universal gate, i.e., any logical reversible circuit can be implemented using this gate. The Fredkin gate acts as a controlled cross switch. If the

control input of a Fredkin gate (A input) is set to ‘0’, then its target outputs, P and Q, are the same as the corresponding inputs, B and C, respectively. If the control input is set to ‘1’, then the target outputs are swapped values of their corresponding inputs. The QC of fredkin gate is 5.

Feynman double gate (F2G) is also a 3*3 fault tolerant reversible gate. The QC of F2G is only 2. It acts as a copying circuit. If the second and third input is set to ‘0’, then we have three copies of the first input in the output. NFT gate is another useful 3*3 fault tolerant reversible gate which is universal. Its QC is only 5. The quantum representation of the NFT is depicted in Fig. 6.a. The IG gate is a 4*4 parity preserving reversible gate. The IG gate is depicted in Fig. 7. The quantum cost of the IG gate is 7 (Haghparast and Navi, 2011).

Existing fault tolerant reversible BCD adder: There are only two existing fault tolerant reversible BCD adders in (Islam and Begum, 2008; Haghparast, 2011). In this section we describe the functionality of both existing designs in detail.

First existing fault tolerant reversible BCD adder: To the best of our knowledge the first existing fault tolerant reversible BCD adder is suggested in (Islam and Begum, 2008). It is depicted in Fig. 8. It includes two four-bit fault tolerant reversible full adder blocks, six Fredkin

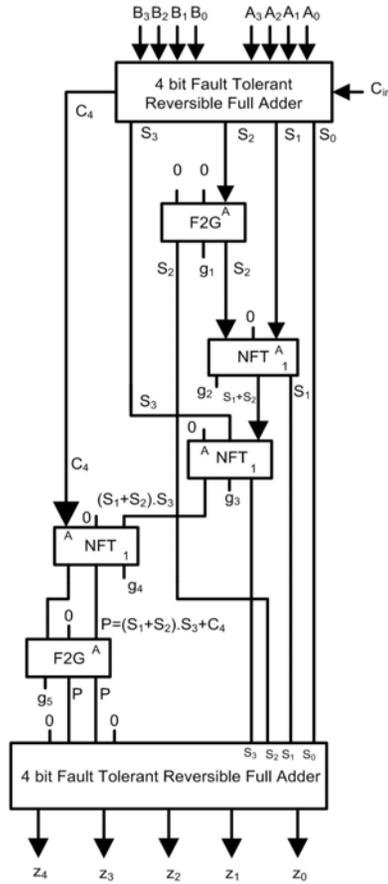
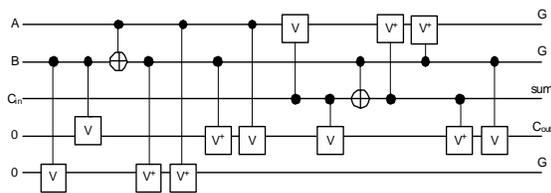
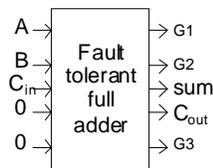


Fig. 9: Existing fault tolerant reversible BCD adder in (Haghparast, 2011)



(a)



(b)

Fig. 10: Fault tolerant reversible full adder in (Dastan and Haghparast, 2011); (a) Quantum representation, (b) Block diagram

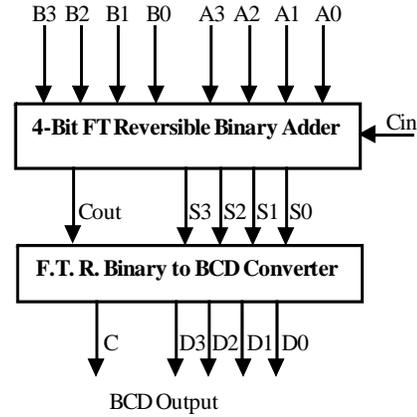


Fig. 11: A new block diagram of a BCD-FA used in the third approach

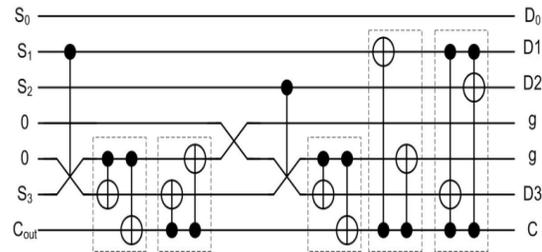


Fig. 12: Our proposed fault tolerant reversible binary to BCD converter

gates and a PPHCG gate. The QC of PPHCG is only 6 (Haghparast and Navi, 2011). This design produces 40 garbage outputs. It also requires 24 constant inputs. The quantum cost of this circuit is 148. To compute the hardware complexity of the proposed design, Let:

- α = A two input EX-OR gate calculation
- β = A two input AND gate calculation
- δ = A NOT calculation
- T = Total Logical Calculation

Thus the hardware complexity of the existing design in (Haghparast, 2011) is $T = 84\alpha + 72\beta + 28\delta$.

Second existing fault tolerant reversible BCD adder: Another existing parity preserving reversible BCD adder which is much better than the first design is suggested in (Haghparast, 2011). It is depicted in Fig. 9. It includes two 4-bit fault tolerant reversible full adder blocks, three NFTA gates and two F2G gates. The QC of the circuit is 131. This design produces 29 garbage outputs. It also requires 24 constant inputs. To compute the hardware complexity of the proposed design, Let:

Table 1: Specifications of the proposed fault tolerant reversible BCD adders in this work and the existing counterparts

Design	No. Gin	No. Gout	QC	Hardware complexity
This work	10	14	84	$46\alpha+34\beta+12\delta$
Existing (Islam and Begum, 2008)	24	40	148	$84\alpha+72\beta+28\delta$
Existing (Haghparast, 2011)	24	29	131	$80\alpha+57\beta+22\delta$
Improvement	58.33%	65~51.72%	43.24~35.87%	-

- α = A two input EX-OR gate calculation
- β = A two input AND gate calculation
- δ = A NOT calculation
- T = Total logical calculation

Thus the hardware complexity of the existing design in (Haghparast, 2011) is $T=80\alpha+57\beta+22\delta$.

In this structure the existing fault tolerant reversible full adder in (Dastan and Haghparast, 2011) is used to construct a four bit fault tolerant reversible full adder which is depicted in Fig. 10. The existing fault tolerant reversible full adder has a QC of only 14. It has two constant inputs and produces only three garbage outputs.

Our proposed fault tolerant reversible BCD adder: In this section we use a different structure to design a fault tolerant reversible BCD adder (Mohammadi *et al.*, 2009). It is depicted in Fig. 11. In this structure instead of designing a detection unit and a correction unit, we design a converter that its input is the output of fault tolerant binary adder, and its output is a fault tolerant BCD digit. This structure requires four fault tolerant reversible full adders. We use the structure of Fig. 10 which is introduced in (Dastan and Haghparast, 2011) as the fault tolerant reversible full adder block. Its quantum cost is only 14.

Our proposed parity preserving reversible BCD adder requires to design a fault tolerant reversible Binary to BCD Converter. The proposed fault tolerant reversible Binary to BCD Converter is depicted in Fig. 12. It includes four F2G gates, two TG gates and two FRG gates. The QC of the proposed circuit is only 28. This design produces only 2 garbage outputs. It also requires only 2 constant inputs. To compute the hardware complexity of the proposed fault tolerant reversible Binary to BCD Converter design, Let:

- α = A two input EX-OR gate calculation
- β = A two input AND gate calculation
- δ = A NOT calculation
- T = Total logical calculation

Thus the hardware complexity of the proposed fault tolerant reversible Binary to BCD Converter circuit is $T = 14\alpha+10\beta+4\delta$.

Evaluation of the proposed fault tolerant reversible BCD adder: Our proposed parity preserving reversible BCD adder performs better than the existing circuits presented in (Islam and Begum, 2008; Haghparast, 2011).

An experimental result will comprehend it clearly. Table 1 compares the proposed reversible circuit with the existing counterparts. Our proposed circuit is better than (Islam and Begum, 2008; Haghparast, 2011) in term of complexity:

For (Islam and Begum, 2008): $T = 84\alpha+72\beta+28\delta$

For (Haghparast, 2011): $T = 80\alpha+57\beta+22\delta$

For our proposed circuit: $T = 46\alpha+34\beta+12\delta$

Thus, the propounded parity-preserving reversible circuit requires less logical calculations than (Islam and Begum, 2008; Haghparast, 2011). One of the other major constraints in reversible logic is to minimize the quantum cost of the circuits. The Quantum Cost (QC) of the proposed design is only 84. The QC of the existing design in (Islam and Begum, 2008) is 148. The QC of the existing design in (Haghparast, 2011) is 131. Thus we can state that the proposed circuit is better than (Islam and Begum, 2008; Haghparast, 2011) in term of quantum cost. Another significant criterion in designing a reversible circuit is to lessen number of constant inputs. A heavy price is paid for every constant input bit. The proposed reversible circuit has only 10 constant inputs. The design in (Islam and Begum, 2008) has 24 constant inputs. The design in (Haghparast, 2011) has 24 constant inputs. Thus, we can state that our design is better than (Islam and Begum, 2008; Haghparast, 2011) in term of number of constant inputs. Another significant criterion in designing a reversible circuit is to lessen number of garbage outputs. The proposed reversible circuit produces only 14 garbage outputs. The design in (Islam and Begum, 2008) produces 40 garbage outputs. The design in (Haghparast, 2011) produces 29 garbage outputs. Thus, we can state that our design is better than (Islam and Begum, 2008; Haghparast, 2011) in term of number of garbage outputs.

CONCLUSION

In this study an optimized nanometric fault tolerant reversible BCD adder is suggested. It is much better than the existing counterparts. The proposed circuit is compared with the existing circuits in terms of the number of constant inputs, number of garbage outputs, hardware complexity and Quantum Cost (QC). Table 1 compares the proposed circuit with the existing circuits. We see that

all the parameters are improved dramatically. At least 35 percent improvement in all the terms is reported. All the scales are in the nanometric area. The proposed circuit can be used in the design of fault tolerant quantum computers.

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