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An Innovative Test Data Compression Method Using Scan Chain Compaction

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Abstract: Test data compression method is a key issue for reducing test data volume and test application time. Various techniques have been developed with great success on dealing with data compression. The previous schemes of compression techniques have been developed to reduce test data volume but the application time is not sufficiently reduced. Additional fault simulation and test generation are necessary to advice high fault coverage. The proposed Odd-Even Scan Network (OESN) provides the high compression ratio and the fast testing time. The compatible scan cell group is planned to implement and it will be integrated with the existing scan chain compaction. The experimental results on ISCAS-89 show that the proposed approach achieves high compression ratio.

Key words: ATE, fault coverage, graph coloring, scan chain, test vector

INTRODUCTION

In recent trends complexity of designing a circuit has increased, when it goes for VLSI circuits it increases twice further, in which testing plays the key role. If the size of test data increases then test cost will also increase which creates new types of defects in the large size of design manufacturing process. For this type of circuit the ATE (Automatic Test Equipment) has to store complex test data and transfer it into the chip. Various test data compression schemes have been developed for reducing test data volumes for simple CUT (Circuit under Test). Methods for dealing with complex test data can be classified into two categories: Code based schemes and structural schemes. The code based approach (Chandra and Chakrabarty, 2001; Nourani and Tehranipour, 2005) has been proposed to reduce only the test data volume and the application time is not taken into account. Dictionary-based compression with fixed length indices method needs the data to be stored in memory or large size hardware circuit. The structural compression (Hsu *et al.*, 2001; Pandey and Patel, 2002) method provides both the reduction of test data volume and testing time. However it does not achieve high fault coverage.

Scan based reconfiguration technique for test data compression in the existing system deals with the XOR-based methodologies. In which the scan chain network is formed using compatible scan cell groups. These groups are formed from the conflict graph, which is related to minimum number of conflict lines for each node. Though it reduces the test data volume, the process is very lengthy. So the application time is high and reduction of scan depth is restricted to a particular level.

To overcome the above drawbacks a new test data compression method using scan chain compaction is proposed. In scan chain compaction reduction of test data is achieved by finding the compatible scan cell groups directly from the conflict graph with less process which minimizes the application time and gives high compression ratio, further while using dictionary based compression scheme (Lei and Chakrabartynk, 2003) it achieves twice the compression.

Scan chain compaction constructs an Odd-Even Scan Network which has minimum number of scan depth or scan cell. As a result of this scan chain compaction it reduces total data volume and the test application time. It delivers high compression ratio and fast application test while retaining the original faults coverage without any additional fault simulation and test generation. The OESN is tested on ISCAS-89 benchmark circuit's experimental result shows that this approach is efficient to reduce the test data volume and test application time.

METHODOLOGY

Existing system:

Scan chain: Compaction means reducing the size of test data in order to reduce the space and transmission time. Scan chain compaction method is one among those which is used to reduce the size of the test data. This method involves constructing conflict graph (Taejin *et al.*, 2010; Miyase and Kajihara, 2003). Conflict graph is constructed by considering the scan cells as the vertices.

The scan cell chain generated by the above approach is given below. Even though it reduces the test data volume it has a limitation of forming individual group only with odd number of vertices. Here whenever number of vertices is even in the group, the last vertex is removed

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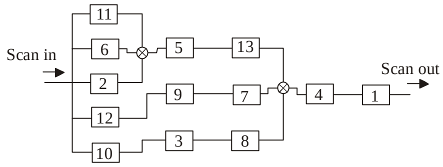

Fig. 1: Existing scan Chain network

TV1	0	0	0	0	1
TV2	0	0	1	1	1
TV3	1	1	0	1	1
TV4	1	1	1	1	1
TV5	0	1	1	0	0

Fig. 2: Test vectors

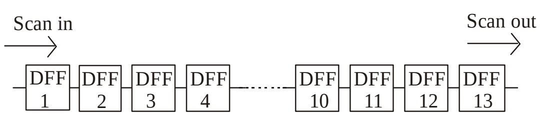

Fig. 3: Sample patterns of single scan Chain

from the particular group and then added to next group, so the scan depth and complexity of process gets increased, which showed in Fig. 1 and 2.

This limitation is overcome by the OESN. For the same example the problem is solved in projected method, in which 13 scan depths is reduced to 4 following the reconfigured scan chain network. In this, while forming the compatible groups there is no constraint that number of scan cell in a group is odd, both odd or even number of scan cell is relevant.

Proposed system:

Scan chain reconfiguration: The proposed method aims to construct an Odd-Even Scan Network with reduced scan depth which results in high compression ratio. Compactable scan cell groups are formed directly from the conflicts graph, without considering the minimum number of edges and by using graph coloring algorithm (Garey and Johnson, 1979). The Groups are formed in such a way that each group should not have any adjacent vertex. While forming group the number of vertices in

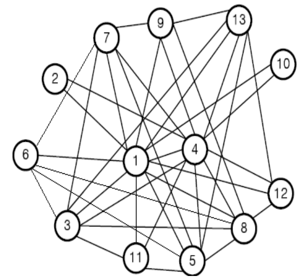

Fig. 5: Conflict graph

each group is taken both odd and even number of vertex. After forming the group they are ordered in descending order. This is used to reduce the area. XOR gates are used for the reason that when odd number of inputs receives the same value it produces the same output as that of the input. This will avoid constant value generation of XOR-gates. If the fan-in of XOR gates is increased then there will be delay in the circuit. To avoid this, minimum numbers of inputs are given to XOR gates and then more XOR gates are used to combine the temporary results.

The problem is given in Fig. 3 and 4. It has 13 flip flops and these flip flops are considered as scan cells. Numbers of scan cells are called as scan depth. Input to these scan cells are generated through ATPG tool. The memory size to store the test data for scan chain is computed as the scan depth times the number of test vectors, for this example it is 13*5 = 65 bits.

There are about 13 scan cells so as per the above system we do have 13 vertices in the conflict graph constructed. Now the adjacency is checked, if there is a vertex that is not adjacent to another vertex, that vertex is added to the group. So groups are formed accordingly.

Conflict graph for the above scan chain is shown in Fig. 5. This will give five set of non-adjacent vertices. Let G1, G2, G3… Gn is the groups of vertices formed by the CUT during the process of scan chain. For the above example groups formed are G1 = {1}, G2 = {2, 3, 5, 9, 10, 12}, G3 = {4, 6}, G4 = {7, 8, 11, 13}.

Now a network is formed from all these groups, here the scan depth is reduced to four. So the application time is reduced from 13 to 4 clock cycles. Apart from this performance enhancement, memory size to store test vectors is also reduced due to the reduction of test data

	DFF1	DFF2	DFF3	DFF4	DFF5	DFF6	DFF7	DFF8	DFF9	DFF10	DFF11	DFF12	DFF13
TV-1	1	X	0	0	0	0	0	0	0	X	X	X	0
TV-2	1	0	0	1	0	X	1	1	0	0	1	0	1
TV-3	1	1	1	1	1	X	0	0	1	1	X	X	0
TV-4	1	X	X	1	1	1	X	1	1	X	X	1	1
TV-5	0	X	1	0	1	0	1	1	X	X	1	X	X

Fig. 4: Test vectors

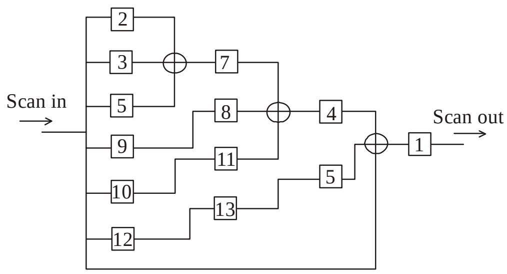

Fig. 6: Odd-even scan network

TV1	0	0	0	1
TV2	0	1	1	1
TV3	1	0	1	1
TV4	1	1	1	1
TV5	1	1	0	0

Fig. 7: Compressed test vectors for OESN

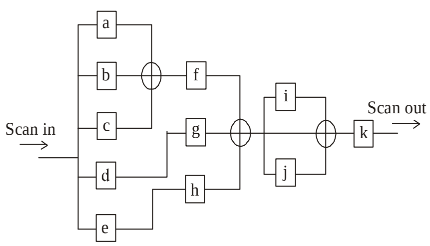

Fig. 8: Sample odd-even scan network

size. Odd-Even Scan Network performance enhancement is illustrated in Fig. 6 and 7.

As shown in Fig. 6, the entire network is divided into four stages. If an XOR gate has even number of inputs, one extra input is given from anyone of the appropriate previous stage. Two examples are shown in Fig. 6 and 8. The major purpose of this third input is to make the number of inputs from even to odd, to the third XOR gate in those circuits.

Table 1: Compression ratio of odd-even scan network

Circuit	Original bits	Compressed bits	Compression ratio of OESN	Compression ratio of existing (Taejin *et al*., 2010)
s13207	70818	10395	85.32	60.95
s15850	59808	18818	68.53	51.17
s35932	28208	8992	68.12	53.24
s38417	164736	26037	84.19	82.47
s38584	199104	78880	60.38	39.97

Table 2: Comparison of compression ratio for scan depth

	Compression ratio in percentage scan depth	
Circuit	Existing	OESN
s13207	59.87	78.84
s15850	43.82	63.67
s35932	53.47	68.12
s38417	49.26	84.19
s38584	40.39	60.38

During the compression process, if the inverse compatible occurs then, insert inverters on the scan path to drive the same test data.

EXPERIMENTAL RESULTS

Experimental results are carried out on ISCAS-89 benchmark circuits and the results are tabulated. The test data are generated through the Mintest. Table 1 shows the Compression ratio of Odd-Even Scan Network. When efficient test data compression is achieved and so is the compression ratio. Table 2 shows Comparison of compression ratio for scan depth. From that we conclude that the proposed system is far better than the existing system. In proposed system the processing time is less and gives high compression ratio. Figure 9 shows the Simulation result for Odd-Even Scan Network. Figure 10 shows the pictorial representation of compression ratio of existing and OESN. Figure 11 shows the graphical representation of compression ratio of existing and OESN for scan depth.

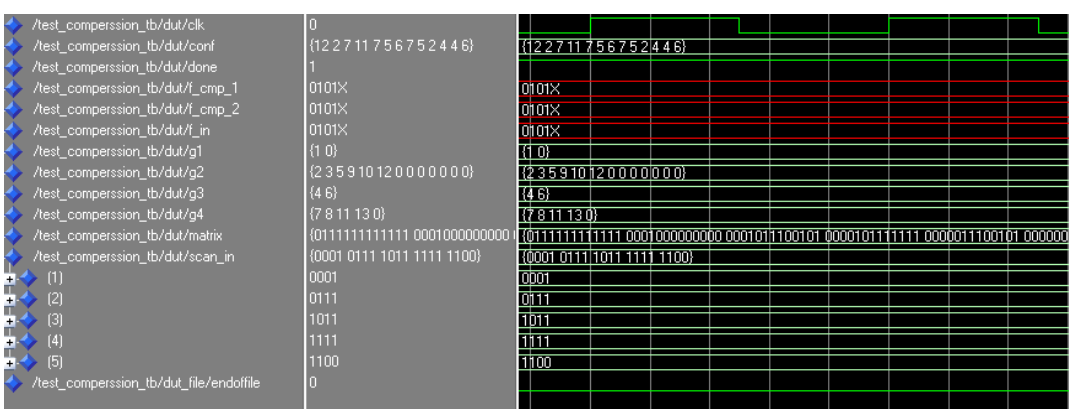

Fig. 9: Simulation result for odd-even scan network

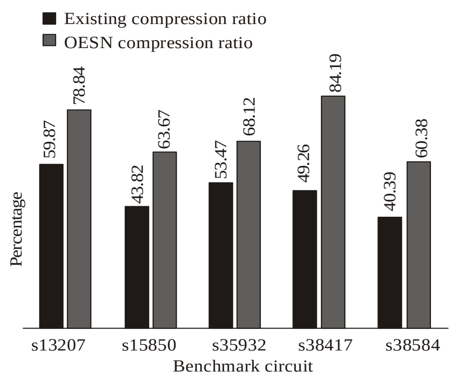

Fig. 10: Compression ratio of existing and OESN

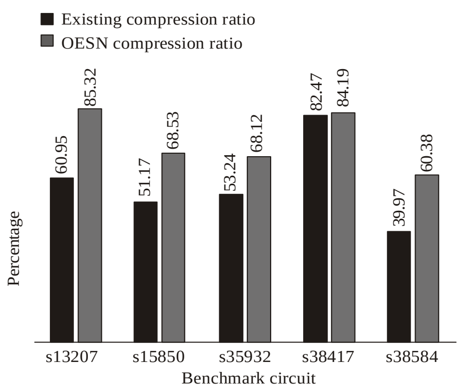

Fig. 11: Compression ratio of existing and OESN for scan depth

Formula for calculating scan depth ratio:

Scan depth compression ratio = (Original Scan Depth – Compressed Scan Depth) / (Original Scan Depth)

CONCLUSION

The experimental result proves that the proposed system has more performance enhancement in terms of speed and area and is more suitable for VLSI chips. Due to decreased scan depth (Fig. 2 and 7), results can be made available within a few clock cycles. Due to increasing of compression ratio (Fig. 10) the memory area to save test vector is reduced. Hence this compression technique is far better than the other existing procedures. Here 3 input XOR gates are used for better fan in and fan out. Future enhancements may involve finding optimum number of fan in and fan out XOR gates. If such gates are identified and used, the test data compression may be increased.

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