

A Novel Approach for X-filling and Reordering Test Vectors for Power Reduction

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Abstract: Optimization of testing power is a significant task to be carried out in digital circuit design. During testing, the power dissipation will be high due to very high number of toggles between test vectors. Hence power minimization is significant during testing. X bits in the test vectors are identified and then X bits are replaced with their appropriate values. The filled vector set is next reordered. In this study, Kruskal based approach is proposed for reordering the vector to minimize the number of toggles and hence power consumption. It is experimented with ISCAS89 benchmark circuits, generated from MINTEST to validate our study.

Key words: Peak power, reordering, switching activity, TSP, X-filling, X-identification

INTRODUCTION

Power is an important aspect in today's environment. System level power reduction and RTL level power reduction are some important power reduction schemes used nowadays. Peak power and average power are two different powers that are to be reduced.

Reordering of test vectors reduces the peak power and hence the average power. Since the test vectors can be represented as a complete graph this problem is similar to solving TSP with a slight modification. The technique used in the existing system includes finding the X identification and fill according to their appropriate values by x-filling. Thus X-filled values are reordered in order to reduce the size. In order to improve the efficiency of the reordering function, a new approach has been proposed which is Kruskal's based spanning tree method. It ensures the least power consumption. Compare to other brute-force techniques, this technique is faster and compare to genetic based approaches like PSO (Wang *et al.*, 2003), ACO etc. and neural based approaches this will give least power.

EXISTING SYSTEM

X identification idea has been proposed in the test relaxation technique for combinational and full-scan sequential circuits (El-Maleh and Al-Suwaiyan, 2002). Brute-force technique (Kajihara and Miyase, 2004) tests each and every bit, and if there occur any change in its value then the fault coverage may reduce. Each bit is checked so it requires large time. So this cannot be applicable for larger circuits. Use of fault simulation is

another way, but here it is similar to implications and justification of the ATPG algorithm and will produce the same fault as the previous method (Girard, 2002). In this X identification technique fault propagation path is more concentrated than the activation path. Dynamic power reduction is not taken into account.

Using line identification, it will identifier the fault activation and fault propagation to the primary output. The values that are identified by these lines are retained and the other lines are changed to X. Fault activation path is also taken into account in addition with fault propagation path without giving up the fault coverage. During this process of X identification and X filling both the dynamic and the leakage powers are reduced. After filling it is reordered further to reduce the power further more. As an effect of reordering, size is reduced, device density increases, so the power is reduced and the demand of chip may also increase.

Power dissipation is high during the testing of a circuit which is produced due to the switching activities. There are two types of power dissipation, static and dynamic. Dynamic power is more concentrated, switching activity is the main cause for most power dissipation. Static power cannot be neglected, so to estimate average leakage power efficiency parallel fault simulation (Lee and Ha, 1992) methodology is used. Dynamic power estimated is considered. A simulator is developed which is used to find the capacitance at the gate output which will help in finding the dynamic power.

For the other transition that will occur during test when compared to the normal function is to reorder the test set, which will modify the sequence of testing. Reordering is mapped with travelling sales man problem (Krishna Kumar *et al.*, 2010), to find the Hamiltonian path

of the minimum cost to form a complete graph is a NP-hard procedure. So different heuristic techniques are used to find the solution of the problems. For lowering the transition density, switching activity is to be reduced. Test vector generated by the ATPG are examined for X identification. X can be replaced as zero or one or greedy method (Kedarnath and Nur, 2007) and these are considered as test vectors.

A branch and bound may be a used to get the best solution. But it is not practical due to its time performance. In order to increase the time performance and maintain the advantage of getting the best solution, we are going for the proposed method. While considering Particle swarm optimization which is randomly taken for the iteration process and more over it won't check till end of the process. This is major disadvantage of the PSO method. Though genetic based approaches like PSO have great time performance optimal solution cannot be obtained by using PSO (Wang *et al.*, 2003).

PROPOSED SYSTEM

In this section the proposed method shows how to reduce the transition between the rows using kruskal based algorithm. Algorithm is explained below.

Algorithm:

- Step 1:** Each vertex represents a unique test vector.
- Step 2:** Form a complete graph. That is each and every vertex is connected to the rest of the vertices.
- Step 3:** Assign edge weights. The edge weight represents number of toggles between vertices.
- Step 4:** Sort the edges in monotonically increasing order.
- Step 5:** Make the vertices into separate sets before starting the iteration.
- Step 6:** Choose the first edge from the beginning of the sorted list.
- Step 7:** After choosing the edge the end points are checked. If they belong to same set then the edge is rejected. If not go to step 9.
- Step 8:** Choose the immediate next edge. Go to step 7.
- Step 9:** The end points of the edge are merged in to a single set and the degrees of both vertices are incremented by one.
- Step10:** Check the degree of any vertex has more than 2 and check in the merged set at least two vertices are having degree 1. If both conditions are satisfied go to step 12.
- Step11:** If at least a condition is not satisfied, then reject the edge. Go to step 8.
- Step12:** Check in a single set all vertices are available. If yes, go to step 14.
- Step13:** Go to step 8.
- Step14:** Terminate the algorithm.

The re-ordered test pattern starts from either single degree vertex and proceed to go to the next vertex (test

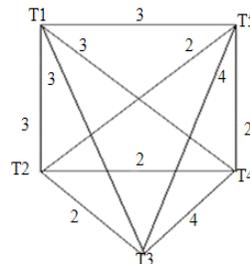


Fig. 1: Complete graph

degree vertex and proceed to go to the next vertex (test pattern) till it meets the last vertex which is also having single degree.

Example: Objective: Re-order the following 5 test vectors such that least toggle occurs.

T1:11010T2:10001T3:01001
T4:10100T5:10111

Figure 1 shows the complete graph for above test vectors. Figure 2 shows the reordered path for this example.

Track 1:

- (T1, T2) = 3 (T1, T3) = 3
- (T1, T4) = 3 (T1, T5) = 3
- (T2, T3) = 2 (T2, T4) = 2
- (T2, T5) = 2 (T3, T4) = 4
- (T3, T5) = 4 (T4, T5) = 2

Track 2:

- (T2, T3)
- (T2, T4)
- (T2, T5)
- (T4, T5)
- (T1, T2)
- (T1, T3)
- (T1, T4)
- (T1, T5)
- (T3, T4)
- (T3, T5)

Track 3:

- {T1} {T2} {T3} {T4} {T5}
- {T2, T3} {T1} {T4} {T5}
- {T2, T3, T4} {T1} {T5}
- {T2, T3, T4, T5} {T1}
- {T2, T3, T4, T5, T1}

Track 4:

- (T2, T3) (T2, T4) (T4, T5) (T1, T3)

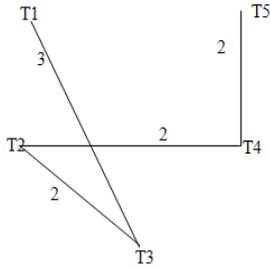


Fig. 2: Least toggle path

Track 5:

- T1, T3, T2, T4, T5
- T5, T4, T2, T3, T1

Track 6: As shown in Fig. 2.

EXPERIMENTAL RESULTS

This section describes the number of toggles occurred using proposed reordering technique. The kruskal based algorithm is implemented using C language and tested with the ISCAS89 bench mark circuits. Here the test patterns are obtained from Mintest dynamic compaction algorithm (Hamzaoglu and Patel, 1998) with 100% fault coverage.

In the ISCAS89 bench mark circuits the test vectors which contain don't care bits are replaced by zero's in the zero fill. Similarly the don't care bits are replaced by one's in the one fill.

Greedy fill algorithm identifies the minterms from the test vectors. The test vectors with don't cares are replaced by that minterm which has maximum number of occurrences (Kedarnath and Nur, 2007). Finding all minterms will be very high in our case, 2^{214} is the minimum! So, a modified method is proposed. Each column is verified whether zero or one has maximum occurrence. Don't cares in that column are filled with that bit.

Table 1 represents the proposed technique for its various comparison methods and its switching activities. Whereas Table 2 describes the compression ratio between PSO and kruskal based algorithm. Here the proposed method compression ratios are better compare to PSO. Greedy fill has the trade-off between maximum compression ratio percentage and time as well as power consumption due to extra comparisons in columns.

Figure 3 shows the proposed kruskal based algorithm for the various techniques and its switching activities. Figure 4 shows the compression ratio for both the proposed and existing systems.

Table 1: Comparison of various techniques and its toggles for proposed technique

Circuits	Zero fill	One fill	Greedy fill
S5378	2559	2485	2175
S9234	4197	3770	3670
S35932	6453	5237	4843
S38584	19791	18972	17004
S38417	18912	17586	12216

Table 2: Compression ratio in percentage

Circuits	PSO	Zero fill	One fill	Greedy fill
S5378	49.33	71.66	72.47	75.91
S9234	40.46	75.32	77.83	78.42
S35932	9.65	44.71	55.13	58.51
S38584	56.55	72.48	73.62	76.36
S38417	39.10	53.26	56.54	69.81

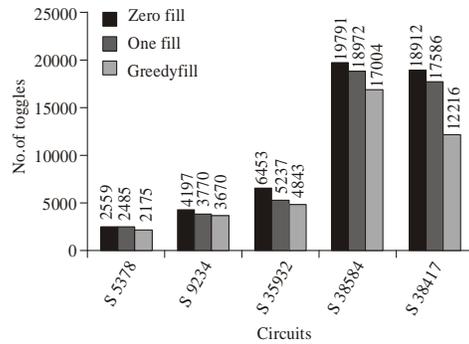


Fig. 3: Comparison of various proposed techniques

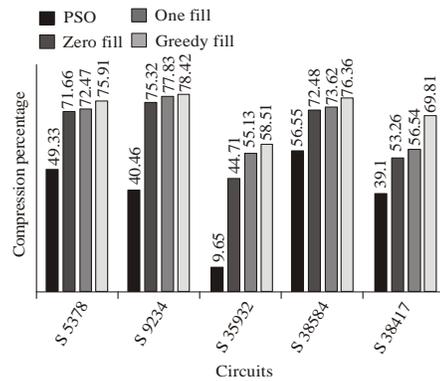


Fig. 4: Compression ratio in percentage

CONCLUSION

This study, a test patterns are obtained from mintest and which is used to find the number of toggles. Kruskal based approach technique to attain minimum transition ratio, which is based on zero fill, one fill and greedy fill algorithm techniques. Experimental results for the ISCAS89 benchmark circuits proved that maximum compression ratio is significantly achieved. And moreover greedy fill algorithm achieves the maximum compression compare to zero fill and one fill. Compare to the particle swarm optimization this method verifies till the end

process and finds out the shortest path where the test vectors are not taken as randomly.

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