Efficient Mathematical Model on VLSI Circuit Partitioning

R. Manikandan, Jaladhanki Sindura, M.D.L. SriRavali and P. Swaminathan
Department of ICT, School of Computing, SASTRA University, Thanjavur-613401, India

Abstract: With the advancement of technology, there is need to develop alternative approaches to classical problems. After powerful mathematical modeling of new approach to classical problems, it is necessary to verify and validate the modeling by well formed experiments. One such area of interest is VLSI Design issue, in particular, Circuit Partitioning. In this study, we address the problem partitioning in VLSI design and layout. After reviewing earlier methods, we present an alternative mathematical model on VLSI circuit partitioning. This is our new direction and with this aim two or more number of research articles contributed by us which in comparison with other algorithms lead to research survey article.

Key words: Circuit partitioning, graph theoretical algorithms, partitioning and mathematical model

INTRODUCTION

Partitioning is a technique to divide a circuit or system into a collection of smaller parts (components). It is on the one hand a design task to break a large system into pieces to be implemented on separate interacting components and on the other hand it serves as an algorithmic method to solve difficult and complex combinatorial optimization problems as in logic or layout synthesis.

Partitioning has been an active area of research for at least a quarter of a century. The main reason that partitioning has become a central and sometimes critical design task today is the enormous increase of system complexity in the past and the expected further advances of microelectronic system design and fabrication.

The size of VLSI designs has increased to systems of hundreds of millions of transistors. The complexity of the circuit has become so high that it is very difficult to design and simulate the whole system without decomposing it into sets of smaller subsystems. This divide and conquer strategy relies on partitioning to manipulate the whole system into hierarchical tree structure. In this study, we unify different techniques and problem specific perspectives so far undertaken by researchers in this field. We wish to add that earlier methods fail to address uncertainty inherent in the problem specification and procedure adopted for solution. Even though there are recently developed mathematical models which do not address completely required precision. Thus, we have developed efficient hypergraph mathematical model to solve such VLSI Design issue.

EXISTING MODELS

The main problem of portioning in VLSI Design and other related domain of study can be placed as getting sub domain of vertices in a given hyper graph. Earliest researchers like Kernighan-Lin (KL) and Fiduccia-Mattheyses (Alpert and Khang, 1996; Alpert *et al.*, 1997; Bui and Jones, 1993) have given algorithms of iterative refinement on the specific nodes of relative importance. Some have placed the problems in searching for Max-Min cut on graphical representation of the design. In a study on hyper graph and co processor design, an approach is made to give a probability algorithm through Markov chain in which additional model for a FPGA layout is suggested using SAT Problem. The reduction in complexity is tackled through SAT Problem. (Thiyagarajan and Manikandan, 2011)

Graph partitioning play an important role in Circuit design and testing. The objective is to divide the circuits into blocks such that the components fall within prescribed sizes. The complexity of the connection between these component is reduced. Controlling of cut size for various types of graph have been studied by (Hendrickson and Leland, 1993; Karypis and Kumar, 1995). Multilevel algorithms compare spectral methods and parallel formulation for such sequential circuit partitioning. Delay minimization of VLSI circuits have been studied through global clustering and connectivity information (Yang and Wong, 1995). Prim's algorithm can complete an optimal solution if node duplication is allowed in circuit design.

(Somasundaram, 2007) has given multilevel sequential circuit partitioning for delay minimization of VLSI circuit using special type of K-Partitioning algorithm and as achieved bench mark circuits. Any given

partitioning problem is to decompose given circuit into K blocks and for given K with balanced area. Circuit delay is a measure as the longest combinatorial for delay from premier input of flip flop output to a premier output or flip of input. Researchers have an objective to perform multilevel partitioning with retiming for minimum delay in reducing cut size as much as possible.

PROPOSED MODEL

Consider a hypergraph G (V, E). Given that function f_o and f_w (weight of each part) exist, and given an integer k >1 and a real-valued balance criterion $0 < \epsilon < 1$, the goal is to find a partition $\Pi = \{P_1 ,\dots , P_K\}$, with corresponding part weights $W_i = f_w(Pi), 1 \le i \le k$ such that:

$W_i < (1 + \epsilon)Wavg$ holds for all $1 \le I \le k$

where

$$\left(Wavg = \sum_{i=1}^{k} w_i / k \right)$$

and $f_o(\Pi, \epsilon))$ is optimized. (Aleksandar, 2006)

Step 1: Input the number of vertices to be considered, N.
Step 2: List the respective adjacent nodes for each vertex to form an adjacency matrix and their weights, W_i
Step 3: Consider a balance factor b, whose value lies between 0 and 1. And, input the number of partitions to be divided, k.
Step 4: Calculate the average weight of all the nodes, Wavg
Step 5: The adjacent nodes are classified into a partition till they satisfy the condition $Wi < (1 + \epsilon)$ Wavg and rest are classified into other partitions based on the same condition.
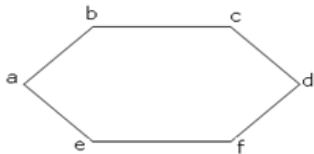
For example, consider the above graph with 6 vertices.
Adjacency matrix for this graph is:

Vertex	Adjacent nodes
A	b, e
B	a, c
C	b, d
D	c, f
E	a, f
F	e, d

Weights of the each vertex are considered as: 2, 1, 3, 2, 3, 1
Then weight average, Wavg is: 2.
Consider the balance factor as: 0.5. Then, condition becomes $W_i < 3$.
When the number of partitions is considered to be 4, then nodes:
a, b come under partition 1,
e comes under partition 2,
c comes under partition 3,
d, f come under partition 4.

CONCLUSION

This model partitions the graph in a simple and easy way. It only considers weights of the nodes based on which the partitioning is done. By adjusting the balance factor we get more optimized results of partitioning. In future, the circuit partitioning may lead strong conjecture in major VLSI Design issue.

REFERENCES

Aleksandar, T., 2006. Parallel algorithms for hypergraph partitioning. Ph.D. Thesis, pp: 34-36.

Alpert, C. and K. Khang, 1996. A Hybrid Multilevel/Genetic Approach for Circuit Partitioning. Fifth ACM/SIGDA Physical Design Workshop, Reston, V.A., pp: 100-105.

Alpert, C.J., J.H. Huang and A.B. Kahng, 1997. Multilevel circuit partitioning. Thirty fourth ACM/IEEE Design Automation Conference Anahein, C.A., pp: 530-533.

Bui, T. and C. Jones, 1993. A heuristic for reducing fill in sparse matrix factorization. *Sixth* SIAM Conf. Parallel Processing Scientific Computing, Norfolk, V.A., pp: 445-452.

Hendrickson, B. and R. Leland, 1993. A Multilevel algorithms for partitioning graphs. Technical report SAND 93-1301.

Karypis, G. and V. Kumar, 1995. Analysis of Multilevel Graph Partitioning. Technical Report TR 95-035, Department of Computer Science, University of Minnesota.

Somasundaram, K., 2007. Multi-level Sequential circuit partitioning for delay minimization of VLSI circuits. J. Inf. Comput. Sci., 2(1): 66-70.

Thiyagarajan, M. and R. Manikandan, 2011. Hypergraph and coprocessor design for VLSI partitioning problems. J. Theoretical Appl. Inf. Technol., 26(2): 107-111.

Yang H. and D.F. Wong, 1995. Circuit clustering for delay minimization under area and Pin constraings. In ED&TC, pp: 65-70.