Research Journal of Applied Sciences, Engineering and Technology 4(14): 2100-2104, 2012
ISSN: 2040-7467
© Maxwell Scientific Organization, 2012
Submitted: January 26, 2012 Accepted: February 16, 2012 Published: July 15, 2012

Test Data Compression Based on Threshold Method for Power Reduction

S. Saravanan and G. Elakkiya
School of Computing (SOC), Sastra University, Thanjavur-613401, India

Abstract: Testing a given circuit is a very important issue in today″s situation due to high test cost. Tester mainly focuses on power dissipation and test data volume. Compression technique is implemented to reduce test power which causes the chip failure and is also used to reduce test data size. This study discusses reduction of test data and scan chain shift-in power. Proposed method on compressing test data is done by threshold method for unspecified test patterns. Appropriate indexing and encoding is done in this method. An analysis of shift in power is carried out for encoded compressed pattern by considering its switching activity. Experimental results prove that the proposed method can produce rapid reduction in test data volume and shift-in power.

Key words: Compression, encode, index, shift-in power, switching activity

INTRODUCTION

An important objective of testing in System-on-Chip (SOC) is test data and power dissipation. It is necessary to reduce them considerably. There is a dynamic growth of scan cells due to increase of chip design technology. This technology accounts for large scale chip design and needs more number of test data and longer scan chains. Power dissipation relates to the switching activity of transitions in the circuit.

Generally power dissipation is considered during scan testing. A circuit or digital system consumes more power in test mode when compared to normal mode (Rosinger *et al.,* 2002) and shift in power of scan chains which is an important contributor to test power. This extra power consumption creates severe hazards in circuit reliability. In some cases, it can even trigger instant circuit damage. Thus, it is of importance to reduce power consumption for SOC test.

EXISTING METHODOLOGY

Number of techniques to reduce power consumption in test mode are presented in (Yoshida and Watati, 2003; Wang, 2002). A drawback of compression schemes based on LFSR reseeding (Lee and Touba, 2007) shows that the unspecified bits are filled with random values, producing large number of transitions during scan-in and hence causing high-power dissipation. In Low Shift and Capture Power Scan Tests (Remersaro *et al*., 2007), take a fully specified test set as input and generate a new test set with reduced shift power and capture power. Through the X-filling procedure, it reduces both shift power and capture power. Fill half of the X-bits to capture power reduction and the other half by shift power reduction.

Controlling scan vector power dissipation and minimized power without additional hardware are specified in static compaction techniques (Sankaralingam *et al.,* 2000). Touba (2006) presents a detailed survey of these techniques. Nine coded compression technique (Nourani *et al.,* 2004) is efficiently adopted for single or multiple-scan chain designs in reducing test application time and pin requirement. In Block Merging technique (El-Maleh, 2008), good compression effect was achieved by encoding runs of fixed-length blocks and only the merged block and number of block merged are recorded. Combining the two methods, run-length based and Huffman coding for scan testing which reduces test data volume, test application time and scan in power.

Selective Huffman encoding scheme (Jas *et al.,* 2003) provides test data compression nearly equal to that of an optimum Huffman code having much less area overhead for the decoder. Some techniques consider a trade-off between compression ratio and test power because test data compression techniques based on coding and test power reduction techniques based on X-filling uses the same X bits in test cubes. Therefore, reducing test power results in compression ratio loss. Run length compression techniques based on encoding runs of 0″s.such as Golomb (Chandra and Chakrabarty, 2001), FDR (Chandra and Chakrabarty, 2003).

In a Selective Scan Slice Encoding Technique (Badereddine *et al.,* 2008) first fill all don″t care bits by X-filling technique, such as 0-filling. Then selective

Corresponding Author: S. Saravanan, School of Computing (SOC), Sastra University, Thanjavur-613401, India

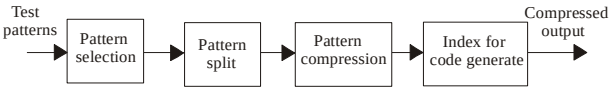

Fig.1: Block Diagram for threshold based test data compression

encoding technique compresses test data. The method results in more test data storage volume compared to Test data compression using selective encoding of scan slices Wang Chakrabarty (2008). But, it is possible to reduce test power with no compression ratio loss. Neither slower scan clock nor blocking logic in the scan cells are required when Golomb coding of test sets which are precomputed is used in order to save peak and average power (Chandra and Chakrabarty, 2001; Chandra and Chakrabarty, 2002). The existing technique (Lin and Chen, 2007) considers on selective pattern compression scheme and is used for reducing size of test data and shift-in power.

This study discusses about various decoders. Four different types of schemes are possible. Fixed to Fixed (F-F) code has both input and output which are fixed. This code is less flexible and not efficient enough to implement compared with Fixed to Variable (F-V) code. Variable to Variable (V-V) code has both input and outputs which are variable. These schemes needs some additional constraints and reduce the complexity to implement compared with Variable to Fixed (V-F) code scheme. Finally Fixed to Variable (F-V) code and Variable to Fixed (V-F) code is chosen to investigate its performance on reduced test pattern and its switching activity. Above two schemes are having different behaviour based on encoding method.

Proposed system: All the test patterns are split into two groups. They are

- More Specified Scan chain (MSS), shift-in pattern which are in non-compressed forms, due to very less number of don″t care.
- More Unspecified Scan chain(MUS), shift-in pattern which are in compressed form, due to very less number of specified bits.

The Fig. 1 shows the block diagram for threshold based test data compression. Test patterns are given as input to pattern selection block. This block divides test pattern into two groups as MSS and MUS. Selected patterns are split into various groups based on input and output dependency. Based on the code generated from the compressed output, index values are allotted.

The compressed output gives the appropriate encoding scheme. This threshold based scheme is used on More Unspecified (MUS) scan chain only. It has more don″t care bit and is easier to implement.

X bit ratio is considered for each and every individual Pattern Length (P_L). X bit ratio is the ratio of PL subtracted with don″t care (X) bits divided by PL. Threshold value is depending on X bit ratio. Threshold values in Eq. (1) are split into MSS and MUS of the test pattern. If X bit ratio in Eq. (2) is more than threshold value, it is called MUS. Otherwise, it is called MSS. Compressed Test Pattern needs a special decoder to decode test patterns:

$$\text{Threshold} = 1 - (\text{X bit ratio}) \quad (1)$$

$$\text{X bit ratio} = P_L - \text{Don't care (X)bits} / P_L \quad (2)$$

This optimization methodology consists on F-V and V-F methods. In this technique, all the test pattern depends on scan chain partition, which split single scan chain into multiple scan chain. The following example describes scan chain partition. Table 1 shows original set test of test pattern, which consist of 7 test patterns each with 19 bit wide.

All the test pattern is to be followed in three stages:

- Pattern selection stage with respect to its corresponding threshold value. Proposed example is considered for 0.2 threshold value.
- Pattern compression stage produces compressed test pattern of More Unspecified Scan chain (MUS).
- Power optimization stage considers switching activity carried out in column by column in MUS. It achieves low shift-in power consumption in encoded patters.

Variable to fixed code and fixed to variable code:

Pattern selection stage: As in the given Table 1 the 7-bit pattern is reduced to 5-bit pattern based on its threshold value. In Table 2 Pattern splitting states for V-F code is generated. Table 4 shows groups each with 5-bit pattern. The corresponding compression stage is given in Table 3. Indexing and encoded compressed output for V-F code is shown in Table 4. This encoding shows variable bit length for proposed index.

For F-V compression, the same procedure is followed as described above. In given Table 5 pattern splitting is observed for 2 groups with 10-bit and 9-bit pattern. Its corresponding compression stage is given in Table 6. Indexing and compressed encoded output is shown in Table 7. To achieve fixed length encoding, the given example is partitioned into 2 groups as shown in Table 5.

Pattern compression stage: The given data is split into several groups according to its TC. Depends up on the TC

Table 1: Original test patterns

More specified bit
X000001011XX10X11010
10010X111XX111X10101
More unspecified bit
10XXX1XX01X101X1110
110XX1XX11X11011XXX
101XXX10X0101XX0111
11XXX01X11XXX011XX0
XXXXXXX1XXXXXXXXXXX

Table 2: Pattern splitting for V-F code

10XXX	1XX01	X101X	1110
110XX	1XX11	X1101	1XXX
101XX	X10X0	101XX	0111
11XXX	01X11	XXX01	1XX0
XXXXX	XX1XX	XXXXX	XXXX

Table 3: Compression for V-F code

101XX	1X101	X101X	1110
110XX	1XX11	X1101	1110
101XX	X10X0	101XX	0111
110XX	01X11	X1101	1110
101XX	1X101	X101X	1110

Table 4: Indexing and encoding for V-F

0	0	0	0	1	11	11	1
1	1	1	0	0	00	00	0
0	2	2	1	1	10	10	0
1	3	1	0	0	01	00	1
0	0	0	0	1	11	11	0

Table 5: Pattern splitting for F-V code

10XXX1XX01	X101X1110
110XX1XX11	X11011XXX
101XXX10X0	111XX1101
11XXX01X11	1010X11XX
XXXXXXX1XX	XXXXXXXXX

Table 6: Compression for F-V code

10XXX1XX01	X101X1110
110XX1XX11	111011101
101XXX10X0	111011101
11XXX01X11	1010X11XX
10XXX1XX01	X101X1110

Table 7: Indexing and encoding for F-V

0	0	11	11
1	1	00	00
2	1	10	00
3	2	01	10
0	0	11	11

value its corresponding encoding is generated. With respect to compressed pattern if the variations found in encoding bit value then it is belongs to V-F category. If the pattern splitting is done according to encoding bit value then it comes under F-V category.

It is described as follows in Table 8. If the Total number of Compression (TC) decoding result is less than or equal to 2, result will be encoded in single bit as per in set 1. Else if the TC is above 2 or less than or equal to 4, result will be encoded as two bits as per in set 2. If the TC is above 4 or less than or equal to 8, then, result will be encoded as three bits as per in set 3. Thus the rest of the combination is take care for encoding. The compression pattern number either is equal or less then original pattern number after the compressing steps.

Table 8: Relationship between TC with encoding

	Conditions	Encoding results
Set 1	$T_c \leq 2$	0
		1
Set 2	$2 \leq T_c \leq 4$	00
		01
		10
		11
Set 3	$4 \leq T_c \leq 8$	000
		001
		.
		.
		110
		111
Set 4	$8 \leq T_c \leq 16$	0000
		0001
		.
		.
		1111
.	.	.
.	.	.
.	.	.
Set N	TNC ≤ M	$M \leq 2^N$

Power optimization stage: This section describes switching activity of proposed method. Power dissipation is applied to any two vectors by counting the number of weighted transitions. This is denoted as by the following Weighted Transitions Metric (WTM) equation:

$$WTM = \Sigma ((L-j). (Tpi, j \text{ XOR } Tpi, j+1)) \quad (3)$$

where TPi,j is the present scan test pattern and TPi,j+1 is the next scan pattern in the design. If more number of scan test pattern is applied then WTM is also considered for Peak power (WTMP) and Average power (WTMA). Peak power is calculated by the maximum value of WTM in „n″ number of scan test pattern. Average power is calculated by summing all test pattern with the average of „n″ test pattern.

Following example illustrates the calculation procedure of WTM. Let the given test pattern set T contains 5 bit in one test pattern. Test vector (T) = 0 1 1 0 1. Its corresponding weighted transition metric WTM value is 7.

In this power optimization stage, low shift-in power is achieved. Proposed low power method is considered for encoded data. Thus switching activity is considered for encoded data transition.

Figure 2, shows proposed stage diagram consider an initial step, where reset signal is high by making ideal stage. In next stage where test patterns are generated from

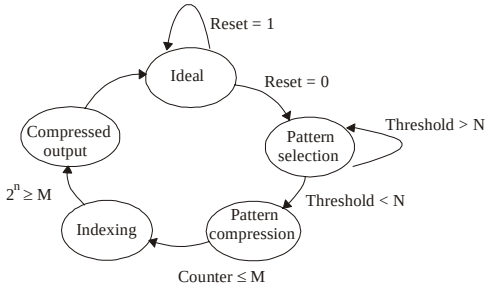

Fig. 2: Proposed state diagram

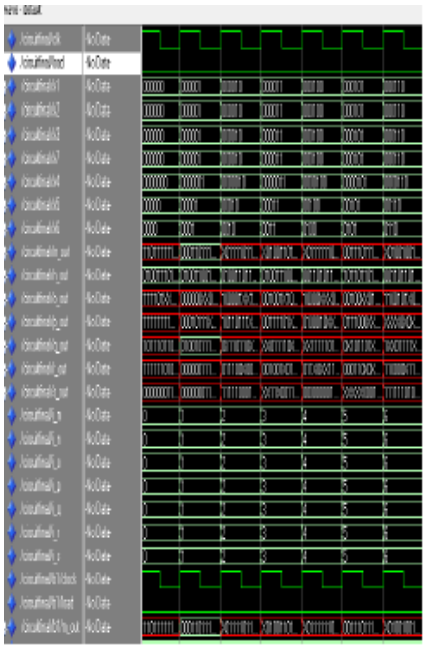

Fig. 3: Proposed simulation result

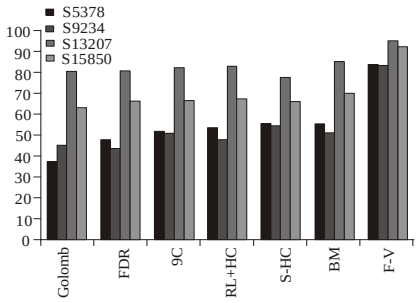

Fig. 4: Analysis for various schemes

the ATPG tool, reset signal is made low. In the pattern selection stage, threshold limit is considered to produce MUS. Compression is considered with row wise pattern and counter is used to count the compressed pattern. At the end, comparing the patterns is limited with group as for adding the counter. It is used to count the next stage of each pattern considering index in compression result in the array memory.

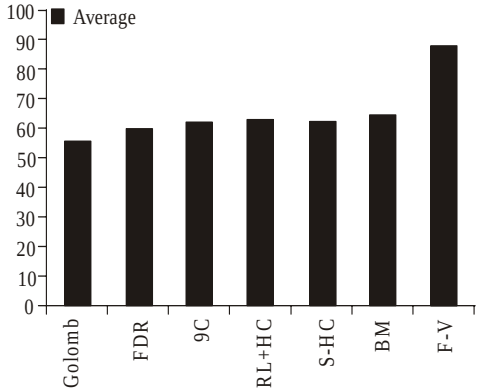

Fig. 5: Analysis average compression for various schemes

Table 9: Experimental result of proposed method

Circuit	Original volume	V-F code %	F-V code %
S5378	23754	81.30	83.17
S9234	39273	80.97	82.99
S13207	165200	82.14	94.85
S15850	76986	81.50	92.14

EXPERIMENTAL RESULTS

This section describes the proposed experimental performance, to evaluate the efficiency of test pattern compression and its switching activity. Proposed method is achieved by proper threshold value and its encoding value. Proposed threshold is taken as 0.2. Implementation is done by using VHDL and tested with full scan version of ISCAS89 benchmark circuit. Mintest dynamic compaction algorithm (Sankaralingam *et al*., 2000) based test pattern is used for experimental work. Simulation results are shown in Fig. 3. Presented waveform outputs are the corresponding outputs produced by the above mentioned block diagram for threshold based test data compression. Figure 4 Shows proposed compression with existing methods. It produces significant reduction in test pattern.

Analysis of average compression is also shown in Fig. 5. Result promises 23 to 30% reduction in average value of compression.

Table 9 shows the experimental results for both V-F code and F-V code. This result shows the advantage of F-V than V-F in compression of test pattern. It is found that F-V code is more efficient than V-F in the order of 1 to 10%. Proposed result is targeted to 0.2 threshold value. Table 10 shows proposed compression method with existing method. It shows significant reduction in average compression. Switching activity is observed in Table 11 as power comparison of encoded test pattern. Total power, Average power and Peak power is calculated as per Eq. (3). It also shows F-V provides less power consumption than V-F code.

Table 10: Experimental result of proposed compression method with other existing method

Circuit	Original volume	Golomb %	FDR %	9C %	RL-HC %	S-HC %	BM %	F-V code %
S5378	23754	37.11	47.98	51.64	53.75	55.10	54.98	83.17
S9234	39273	45.25	43.61	50.91	47.59	54.20	51.19	82.99
S13207	165200	79.74	81.30	82.31	82.51	77.00	84.89	94.85
S15850	76986	62.82	66.21	66.38	67.34	66.00	69.49	92.14
Average	-	56.23	59.77	62.81	62.79	63.07	65.13	88.28

Table 11: Experimental result for power consumption

Circuit	Pattern	Total power	Average power (WTMA)	Peak power(WTMP)
S5378 V-F	111	33836	304.82	591
S5378 F-V	111	28337	255.28	488
S9234 V-F	159	70697	444.63	794
S9234 F-V	159	68405	430.22	770
S13207 V-F	236	452836	1918.79	5475
S13207 F-V	236	168117	712.36	2152
S15850 V-F	126	253146	2009.09	5116
S15850 F-V	126	139015	1103.29	2834

CONCLUSION

Two schemes with related encoding methodology to reduce test power consumption and test data volume are proposed in this study. These schemes achieve better reduction rate of test data volume which are recorded as experimental results. Comparison of Fixed to Variable (F-V) code with previous work shows that the results provide relatively small test data size. Results shows average compression is reduced about 23 to 30% compared with existing systems. In addition, we implement the decoder for F-V code in VDHL and observe its trade-off between volume of test pattern and shift-in power. Switching activity is also reduces significantly. The approach made this project is practical and fit enough to be applied in modern DFT chip designs.

REFERENCES

Badereddine, N., Z. Wang and P. Girard, K. Chakrabarty, A. Virazel, S. Pravossoudovitch and C. Landrault, 2008. A selective scan slice encoding technique for test data volume and test power reduction. J. Electronic Testing: Theory Appl., 24(4): 353-364.

Chandra, A. and K. Chakrabarty, 2001. System-on-a-chip data Compression and decompression architecture based on Golomb codes. IEEE T. Comput. Aided Des, 20(3): 355-368.

Chandra, A. and K. Chakrabarty, 2001. Combining low-power scan testing and test data compression for system-on-a chip. In Proceeding ACM/IEEE Design Automation Conference pp: 166-169.

Chandra, A. and K. Chakrabarty, 2002. Low-power scan testing and test data compression for system-on-a-chip. IEEE T. Comput. Aided Design, 21: 597-604.

Chandra, A. and K. Chakrabarty, 2003. Test data compression and test resource partitioning for system-on-a-chip using Frequency-Directed Run-length (FDR) codes. IEEE T. Comput., 52(8): 1076-1088.

El-Maleh, A.H., 2008. Efficient test compression technique based on block merging. IET Comput. Digit Tech, 2(5): 327-335.

Jas, A., J.G. Dastidar, M.E. Ng and N.A. Touba, 2003. An efficient test vector compression scheme using selective Huffman coding. IEEE T. Computer-Aided Des. Integr. Circuits Syst., 22(6): 797-806.

Lee, J. and N.A. Touba, 2007. LFSR-reseeding scheme achieving low-power dissipation during test, IEEE Trans. Computer-Aided Des. Integr. Circuits Syst., 26(2): 396-401.

Lin, C.Y. and H.M. Chen, 2007. A selective pattern-compression scheme for power and test-data reduction. In Proceeding International Conference Computer-Aided Design, pp: 520-525.

Nourani, M., M. Tehranipour and K. Chakrabarty, 2004. Nine-coded compression technique with application to reduced pin-count testing and flexible on-chip decompression. In Proceeding Design, Automation, Test in Europe, pp: 1284-1289.

Remersaro, S., X. Lin, S.M.. Reddy, I. Pomerany and J. Rajski,, 2007. Low Shift and Capture Power Scan Tests. Proceeding of the 20th International Conference on VLSI Design (VLSI D), pp: 793-798.

Rosinger, P.M., P.T. Gonciari, B.M. Hashimi and N. Nicolici, 2002. Analysing trade-offs in scan power and test data compression for systems-on-a-chip. IEEE Proc. Comput. Digital Tech., 149: 188-196.

Sankaralingam, R., R. Oruganti and N.A. Touba, 2000. Static compaction techniques to control scan vector power dissipation. In Proceeding IEEE VLSI Test Symp., pp: 35-40.

Touba, N.A., 2006. Survey of test vector compression techniques. Design Test Comput., 23(4): 294-303.

Wang, Z. and K. Chakrabarty, 2008. Test data compression using selective encoding of scan slices. IEEE Trans. VLSI Syst., 16(11): 1429-1440.

Wang, S. and S.K. Gupta, 2002. An automatic test pattern generator for minimizing switching activity during scan testing activity. IEEE T. Computer-Aided Design, 21: 954-968.

Yoshida, T. and M. Watati, 2003. A new approach for low-power scan testing. In Proceeding International Test Conference, pp: 480-487.