

Digital Waveform Generator Based on FPGA

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Abstract: Field Programmable Gate Array (FPGA) of the Cyclone II series was as the core processor of frequency meter and the Quartus II was as the development platform. This article had designed the fully digital signal generator. It used all-digital frequency synthesizer technology and FPGA programming implemented the three waveforms: sine wave and square wave and triangle wave. The frequency was adjustable through 10-bit phase accumulator and the analog multiplier achieved amplitude modulation. Using 51 soft nuclear FPGA wrote a C program and realized the input control word. The 4 × 4 matrix keyboard inputted frequency or amplitude value and the LCD1602 displayed them. The test results show that the system has high precision, distortion and low.

Key words: 51 soft nuclear, digital frequency synthesis, field programmable gates away, waveform generator

INTRODUCTION

Waveform generator is an indispensable tool for all kinds of test and experiment and it is also have very extensive application for communication, measuring, radar, control and teaching field. Both in production, scientific research or in the teaching, waveform generator are the best tools for electronic engineers to do the simulation experiment of signal. Along with the development of our country economy and science and technology, the corresponding test equipment and testing method put forward higher request and waveform generator test instrument has become very important, so it has important significance to develop waveform generator (Zhang *et al.*, 2011; Li and Ma, 2010; Feng *et al.*, 2010; Luo, 2011).

The FPGA is programmable IC and it has the highest integration and complexity (Zhang *et al.*, 2011). The FPGA can implement the arithmetic logic unit, the multiplier, the digital filters and the two-dimensional convolution, etc., with the logical design of the logical unit of complex algorithms and signal processing unit and it can repeat programming for infinite times and it also can modify and uninstall the finished design in the same device and a lot of number of basic components on the FPGA, which makes a very complex electronic circuit design into something more than reality (Bao *et al.*, 2008). In recent years, the FPGA technology obtained a rapid development and extensive application of greatly increase of its resource capacity, working frequency and integration and the use of FPGA got attention in realizing some special digital integrated circuit and direct digital

frequency synthesizer based on FPGA has the more advantages (Li and Ma, 2010). The advantages are that it has a flexible interface and the control mode, a relatively short period of time, a wide conversion bandwidth and phase change and continuous frequency resolution is higher. It also provides another method for designers based on integrated realization circuit is the FPGA technology in the realization of the application for DDS system of digital part design. First will meet the problem of transmission across the clock that is very typical in the FPGA design. The output of the single chip microcomputer clock is μs magnitude and FPGA digital system is the ns magnitude, so the transmission speed matching directly affects the stability of the input control word.

This study took FPGA as signal generator. Frequency or amplitude value is input from the keyboard and it will be displayed in the LCD1602. Frequency or amplitude value is converted to frequency or amplitude control word sent to the DDS through the micro controller. Moreover, the direct numerical frequency synthesizer based on FPGA has a lot of benefits, such as flexible joggle and way to control, relatively short transmuting time, relatively broad belt, the succession of change of phase position and high screen resolution, etc.

DDS TECHNOLOGY

The Direct Digital frequency Synthesis technology (DDS) is a new technology of frequency synthesis and way to produce signal (Feng *et al.*, 2010). The traditional digital method of producing sine wave is to make use of

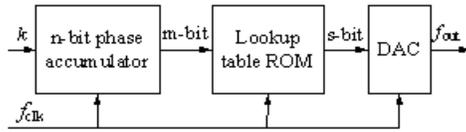


Fig. 1: DDS composite

a piece of ROM, a piece of DAC and the address counter. In order to make output frequency more convenient, it can use phase position accumulator, which makes output frequency proportional to the product of clock frequency and the increment of phase position. It is shown in Fig. 1.

The direct synthetic system which applies the method of phase position accumulator makes the accuracy of the sine wave on the phase is taken as the n -bit, then the resolution ratio amounts to $1/2^n$. It fetches each point on the numerical phase position circle (the number used as address) and reads the sine wave amplitude value of ROM and reconstitutes the sine wave through DAC. The function of phase position in this system is to fetch a number every other k points when reading each point on the numerical phase position circle (k is the frequency control word). In this way, the DAC out put sine wave frequency is formula (1):

$$f_{SIN} = k(f_{clk}/2^n) \quad (1)$$

In the formula, f_{clk} is a clock of DDS; n is usually in between 24 and 32.

The DDS core is phase position accumulator. It is like a common calculator, but it is composed of n -bit adder and n -bit phase position register. When a clock pulse comes, the output of the phase register will add as 2π phase increment value. The adder adds the frequency controlling data and the accumulating phase position data outputted by accumulating register and sends the result to the data input terminal of the accumulating register. The phase position accumulator comes into linearity phase position accumulation, to the extent of producing a counting overflow, whose frequency is the output frequency of DDS. The sine polling list is a programmable PROM. It stores a periodic sine-signal sampling value of encoding with regarding a phase position as its address. It contains information of numerical range of periodic sine wave and each address corresponds to a phase point of the range from 0-360 degree in sine wave. If we add the output of phase register to phase controlling data, we can get a data which can be used as an address to addressing sine polling list. The list maps the inputted address information into sine wave range signal, drives DAC and outputs the analog signal (Liu *et al.*, 2009a).

DDS parameters: For the countcapacity 2^n phase accumulator and sine wave waveform memory of a sampling point phase of m , if the frequency control

character is k , the output signal frequency for f_{SIN} and the reference clock frequency for f_{clk} , then the system output signal frequency is formula (2):

$$f_{SIN} = k f_{clk}/2^n \quad (2)$$

The frequency resolution of the output signal frequency is formula (3):

$$\Delta f_{min} = f_{clk}/2^n \quad (3)$$

From the Nyquist sampling theorem, it is known that the largest frequency of the DDS output is formula (4):

$$f_{max} = f_{clk}/2 \quad (4)$$

The k of frequency control word can be launched by the above formula and it is formula (5):

$$k = f_{SIN} \times 2^n / f_{clk} \quad (5)$$

when the frequency of external reference clock is 50 MHz and the output frequency is 1 MHz, after six times frequency of the system clock, then make f_{clk} into 300 MHz, it can use the above formula calculated control frequency word that the DDS need to set: $k = 248/300$.

DDS composition: DDS. vhd top design principle is shown in Fig. 2. It is compiled in the Quartus II environment. The Quartus is FPGA/CPLD development integration environment that provided by the company Altera and it provides a design environment that has nothing to do with the structure, so designers can design input easily, process rapidly and device programming. Quartus design tools fully support the design process of VHDL and Verilog and it's internal studded with VHDL, Verilog logic synthesis device. Also, Quartus have simulation function, but also support the third party simulation tools. Quartus include modular compiler. The module compiler includes the function of analysis/comprehensive device, adapter, with instruments, timing analyzer, compile data interface, etc (Ma and Wang, 2011).

K8051SOFT-COR E MICROCONTROLLER AND KEIL SOFTWARE

The chip microcomputer 89C51 is a low voltage and CMOS 8-bit microprocessor with 4k bits Flash programmable and erasable read only memory. 89C2051 is a chip microcomputer of FPEROM-Flash Programmable and erasable read only memory with 2k bits. The chip microcomputer of erasable read only memory can be erased 100 times. Its device applies ATMEL and is compatible with industrial standard MCS-51. Because of multifunctional-figure CPU and flash memory composed in a single slug, 89C51 of ATMEL is an efficient microcontroller and 89C2051 is its simplified version (Liu *et al.*, 2009b).

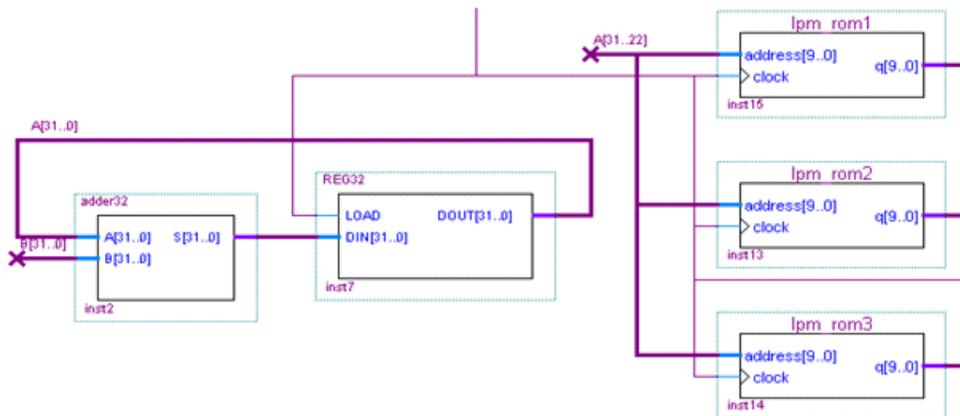


Fig. 2: DDS.vhd top principle diagram

Link the ROM and RAM to 8051soft nuclear, it becomes the complete 8051 single chip microcomputer. The MCS51 microcontroller CPU also belongs to CISC CPU. K8051 microcontroller is VQM by the original code (Verilog Quartus Mapping File) to express, in Quartus II environment it can be with VHDL, Verilog and other hardware description language mixed compile comprehensive and in a single piece of FPGA, it can realize all hardware system and complete the software debugging. K8051 microcontroller nuclear also contains 8-bit complex instructions and its memory uses Harvard structure. K8051 instruction system and 8051/2 and 8031/2 are fully compatible and hardware is also basic same. For example, it may meet 64 kB external storage and also may meet 256 bytes internal data RAM and it includes two 16 timing/counter, full-duplex serial ports, the power consumption of the save work mode and interrupt response structure and so on.

Keil is the 51 SCM development software platforms. The Keil μ Vision2 can be simulation software. To connect 51 SCM into the hardware emulator and load the project program in the emulator, then it can achieve real-time simulation. It can also use μ Vision2 embedded module, the Keil monitor-51, under no additional hardware emulator conditions, connected to the microcontroller hardware system and achieve real-time simulation for the project program.

When the system starts work, first initialize the system and then execute keyboard scan subroutine, buttons for identification. In data processing procedure, the system will be the keyboard input keys of many times for the corresponding frequency conversion or amplitude value and the P1 to mouth. This frequency or amplitude value using the formula method is transformed in to the frequency or amplitude control word sent to the P0 port that is connected to the DDS, so the control word is sent to the DDS. Call LCD display routines and the frequency or magnitude value of the P1 port is displayed in the LCD monitor. After the whole program execution, the

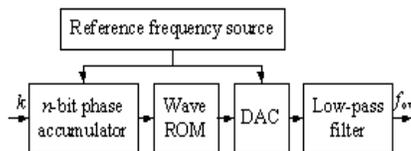


Fig. 3: DDS principal diagram

program returns to the keyboard scanning subroutine, successively own to execution.

KEY TECHNOLOGIES

Signal module: With random read/write memory for storage of the waveform RAM quantitative data, according to the different frequency, at the request of the frequency, control word K is as stepping on phase incremental cohorts, to accumulate phase value for existing and read waveform data within the memory address. D/A converter and amplitude control and then filtered to get the desired wave form. Because DDS has the relative bandwidth widely, the frequency conversion time is shortly (but less than 20 micro sec) and the frequency resolution is also higher (Feng *et al.*, 2010). All-digital architecture facilitates the integration and output phase-continuous, frequency, phase and amplitude can be programmed to achieve. The DDS principle diagram is shown in Fig. 3.

DDS technology has high resolution, frequency conversion speed, high purity, phase signal controllable, output signal no current pulse output can stack, smooth transition and phase can keep continuous change.

Display module: The LCD can display all characters and custom characters and can also shows that many sets of data of Chinese characters and the characters is clear. Because of its own controller, not only can reduce the burden of the single chip microcomputer, but also can

achieve the result that drive mode of menu and realize the full screen edit the editor module function, to friendly human-machine interface. LCD display can solve LED display numbers only several simple character shortcomings (Ding and Li, 2011).

It has the advantage of simple interface circuit, good performance, multi-effects and easy to control.

Phase accumulator: The role of phase accumulators is to linear accumulative the input frequency control word, through feedback a clock on the stack in the back of the adder input realize accumulate function. So that the output each clock cycle will increase k . Here, the n is the word length of phase accumulators; the k is called frequency control word. When phase accumulators are filled with can produce a spill, thus completing a cycle, the cycle is also a cycle of DDS. In the Fig. 3, the phase accumulators are made by a 32-bit adder and a 32-bit registers REG32. Among them, VHDL code of the binary adder addre32 is:

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;
use IEEE.STD_LOGIC_unsigned.all;
entity adder32 is
port(
  A:in STD_LOGIC_VECTOR(31 downto 0);
  B:in STD_LOGIC_VECTOR(31 downto 0);
  S:out STD_LOGIC_VECTOR(31 downto 0)
);
end adder32;
architecture bhv of adder32 is
begin
  s<=A+B;
  End bhv;
```

In Quartus environment, choose the new of file menu, select Create Symbol Files for Current File of Create<Update in new window, then completes the creation of the project. In the design of schematic diagram, click the mouse left key doubly, then pop up Symbol dialog box, it can find and call the 32-bit adder create in the Project.

To use the same method, it can create 32 registers REG32. VHDL code is:

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;
use IEEE.STD_LOGIC_unsigned.all;
entity REG32 is
port(
  LOAD:in STD_LOGIC;
  DIN:in STD_LOGIC_VECTOR(31 down to 0);
  DOUT:out STD_LOGIC_VECTOR(31 down to
0)
);
end REG32;
architecture bhv of REG32 is
begin  process(LOAD,DIN)
```

```
begin
if LOAD'event and LOAD='1' then
  DOUT<=DIN;
end if;
end process;
End bhv;
```

Through the encapsulation, in the design of the schematic diagram, click the mouse left key doubly, it can pop up Symbol dialog box. In the Project, it can find and call the 32 registers to create REG32.

ROM wave data: Before the design of waveform generator it must be completed for the design of the ROM wave data, using mega wizard plug-in manager custom ROM signal data macro module and will design good wave data loading in this ROM. First create mif data form and then In the File menu select new and in the new window choose other files page, then choose a memory initialization file. Click the ok button to produce the ROM data file size choice. In the design, choice the ROM data number for 256 and datamodels word is set to 8-bit. Click the ok button and it will appear empty mif data form and compile by the software and placed cycle 256 point waveform data of the triangle wave and square wave and sine wave.

To select the mega wizard plug-in manager in the tools menu and create a new custom interface, that is, a new custom module. Click next button and cause the LPM macro feature piece of setting dialog box and choose the LPM_ROM under the left column storage, finally input ROM deposit path and filename and follow the prompts to select the ROM control line and address lines and data lines. Finally, respectively ,tri.mif and squ.mif and sin.mif loaded into the waveform memory inside.

Waveform in memory of the corresponding is a function waveform lookup, corresponding to different phase code value of output by different code value. When the phase control word is 0, phase accumulate output sequence is for the waveform storage addressing and it will get a series of discrete amplitude of the code. The amplitude coded by the D/A transformation will get the corresponding ladder wave, finally, smoothed by the low-pass filter can be obtained the analog waveform. Phase accumulators under time and frequency standards action, carry on the linear phase accumulate, when phase accumulators filled with, it can produce a spill, thus completing a cycle, the cycle is also a DDS signal frequency cycle (He and Sun, 2010).

Lmp-mult 1 multiplier: Its input is waveform and amplitude control word processed. Its function is to adjust the waveform amplitude. The line multiplication accumulators is as a macro module structure, its calls and lmp_ROM calls general basic meet and it is shown Fig. 4.

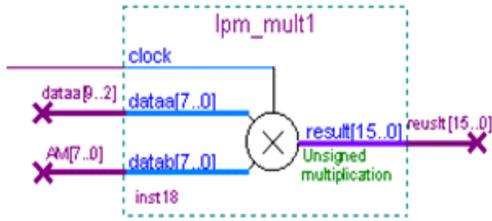


Fig. 4: Lmp-mult1multiplier

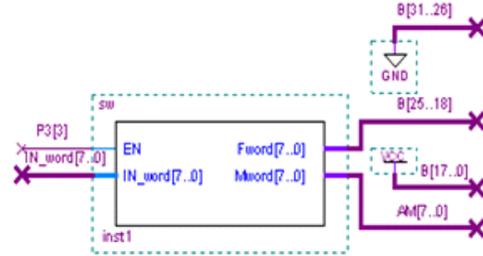


Fig. 6: Interface of 8051 and DDS

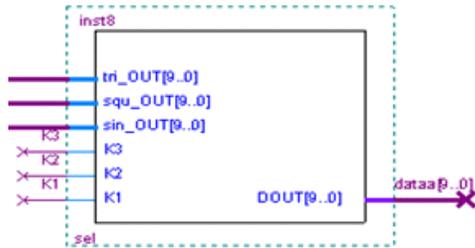


Fig. 5: Waveform selector

Waveform selector: The packaged sel isa waveform choice device. When press the switch K1,the output is a sine wave. When press the K2, the out put is a square wave. When press the K3, the out put is a triangular wave. It is shown in Fig.5. The VHDL code is:

```

library IEEE;
use IEEE.STD_LOGIC_1164.all;
use IEEE.STD_LOGIC_unsigned.all;
entity sel is
port ( K1,K2,K3:IN STD_LOGIC;
sin_ O U T , s q u _ O U T , t r i _ O U T : I N
STD_LOGIC_VECTOR(9 downto 0);
DOUT:out STD_LOGIC_VECTOR(9 downto 0)
);
end sel;
architecture bhv of sel is
signal q:STD_LOGIC_VECTOR(9 downto 0);
begin
process(K1,K2,K3)
begin
if K1='0'and K2='1'and K3='1'thenq<=sin_OUT;
--end if;
elsif K1='1'and K2='0'and K3 =
'1'thenq<=squ_OUT;
--end if;
elsif K1='1'and K2='1'and K3 =
'0'thenq<=tri_OUT;
--end if;
--end if;
end if;
DOUT<=q;
End process;
end bhv;

```

Interface of the microcontroller and DDS: Through the P0 port to the DDS, 8051 microcontroller outputs the signal frequency control word and the signal amplitude control word. LinkP3[3]toenable terminal EN, which is used to control the K8051exportcontrol the signal word. When the enable terminal EN is1, the output is a frequency control word; when the enable terminal EN is0, the output is an amplitude control word. By SW components, the frequency control word and phase control word will be out putted to the DDS specific location. It is shown in Fig.6.

The VHDL code is:

```

library IEEE;
use IEEE.STD_LOGIC_1164.all;
use IEEE.STD_LOGIC_unsigned.all;
entity sw is
port(
EN:in STD_LOGIC;
IN_word:in STD_LOGIC_VECTOR(7 downto 0);
Fword, Mword:out STD_LOGIC_VECTOR(7
downto 0)
);
end sw;
architecture bhv of sw is
begin
process(EN)
begin
if(EN = '1') then
Fword<=IN_word;
else
Mword<=IN_word;
end if;
end process;
end bhv;

```

DAC transformation: Each digital code has the certain bit right value. In order to convert digital to analog, this code according to the bit value of the right must be converted into the corresponding analog and then the analog sum can be obtained with digital proportional to the analog, so that it will achieve the digital-analog converter.

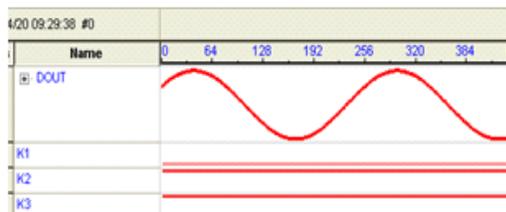


Fig. 7: Sinewave display

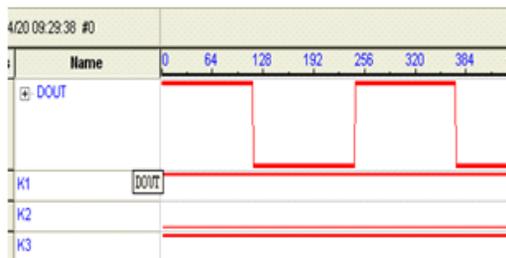


Fig. 8: Square wave display

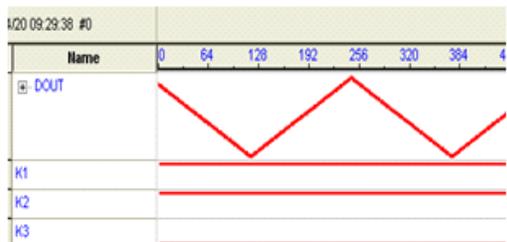


Fig. 9: Triangular wave display

```
VHDL code of the DAC is:
library IEEE;
use IEEE.STD_LOGIC_1164.all;
use IEEE.STD_LOGIC_unsigned.all;
entity DAC is
port(
CLK:in STD_LOGIC;
q:in STD_LOGIC_VECTOR(9 downto 0);
--wr:out STD_LOGIC;
DOUT:out STD_LOGIC_VECTOR(9 downto 0)
);
end DAC;
architecture bhv of DAC is
begin
process(CLK)
begin
if CLK'event and CLK='1' then
DOUT<=q;
end if;
end process;
```

```
--wr<='0';
end process;
end bhv;
```

Configuration file download and test: Embedded logic analyzer test, the waveform of sine, square and triangular wave is shown in Fig. 7, 8 and 9.

The sof file will be compiled into the FPGA. Open programming window and the configuration file. First, the test system and parallel communication lines connected turn on the power. Select programmer in the tool, if the file does no terror, click the add file but to non the left, configured file 8951. sof manually. Choose for programming and click on the download punctuation start button, namely into the target of the FPGA device configuration downloading operations. Quartus software owns embedded the logical analyzer can effectively for the testing of the system hardware. In the testing, Sinnal Tap II sample signal measured temporarily stored in the target device' s embedded RAM and then the acquisition signal will be sent to the computer for display and analysis (Luo, 2011). Open SinnalTap edit window and then call the being measured signal and set SinnalTap II parameter and save the file and compile and download and finally start SinnalTap II to sample and analyze the signal, at last the computer displays this adjective waveform.

CONCLUSION

This study took FPGA as signal generator. Frequency or amplitude value is input from the keyboard and it will be displayed in the LCD1602. Frequency or amplitude value is converted to frequency or amplitude control word sent to the DDS through the microcontroller. DDS rely on the delivery frequency or amplitude control word, the output waveform for frequency modulation and frequency modulation processing. The direct numerical frequency synthesizer based on FPGA has a lot of benefits, such as flexible joggle and way to control, relatively short transmuting time, relatively broad belt, the succession of change of phase position and high screen resolution, etc.

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