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Design of High Performance Phase Locked Loop for UHF Band in 180 nm CMOS Technology

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Abstract: The aim of this study was to design low phase noise 2.4 GHz ring oscillator with low power dissipation and small die area. This study presents the design of high performance PLL for UHF band. This PLL has been realized in 180 nm by Virtuoso Analog Design Environment of Cadence tool. After simulating various stages of the ring oscillators, a three-stage ring oscillator has been selected for the implementation of the PLL. A zero dead zone Phase Frequency Detector (PFD) and Charge Pump (CP) with loop filter have been designed and used in the PLL. The PLL has designed with lowest phase noise of-122.2 dBc/Hz @ 10 MHz offset frequency and figure of merit-134 dBc/Hz. The layout of complete PLL has been designed by Virtuoso LayoutXL tool of Cadence. The total area required to implement the PLL without package is (0.093 × 0.09783 mm) 0.0091 mm^2.

Keywords: Charge Pump (CP), Phase Frequency Detector (PFD), Phase Locked Loop (PLL), Voltage Controlled Oscillator (VCO)

INTRODUCTION

The PLL is used to synchronize the signal. In an Orthogonal Frequency Division Multiplexing (OFDM) techniques in multi carrier communications a PLLs are widely used to synchronize the signal (Yalcin and John, 2004). A PLL consist of Charge Pump (CP), Phase Frequency Detector (PFD), Voltage Controlled Oscillator (VCO), Low Pass Filter (LPF) and divider. The PLL acts as a high-pass filter against the VCO noise, the charge injection and clock feed through disturb the voltage at the cut-off frequency of LPF (Wenyou and Hu, 2009; Liang and Shen-Iuan, 2007; Seung and Sang-bock, 2007; Woogeun and Keith, 2008). To achieve a higher speed PFD than the specified, another design is proposed which depends on detecting the rising and falling edge of the input signals (Xiang and Klumperink, 2009; Cheng and Yang, 2001). A PLL is generally used in wireless communications and data recovery circuits. A VCO is the heart of the PLL and can be designed either by LC or RC. A LC VCOs have superior phase noise performance compared with ring VCO'S. However, an LC VCO has a small tuning range large layout area and possibly higher power (Yalcin and John, 2004). A challenging work in the CMOS technology is to design a low phase noise ring oscillator for a Charge Pump Phase Locked Loop (CPPLL) using CMOS technology. A design presented here is to improve the overall characteristics of PLL. The first component of the PLL is the PFD which has been designed to improve the speed by minimizing the dead zone. The CP circuit improves the performance of the PLL because it has been designed for high bandwidth. The main part of this PLL is the VCO, which has been designed to get superior phase noise.

METHODOLOGY

PLL architecture: To synchronize the frequency, various types of PLLs like analog linear and CPPLLs are being used in the application of wireless communication. Both PLLs are consists of CP, PFD, LPF, divider and VCO which is shown in Fig. 1. In addition with VCO, the PFD compares feedback signal with input signal and generates the error signal. A charge pump circuit along with LPF is used to minimize the disturbances at the input of VCO and to get a sharper and smooth signal at the VCO output (Razavi, 2001).

Phase frequency detector: The aim of designing PFD is to reduce size, static error and dead-zone. The dead zone occurs when output of the charge pump does not change. This is the one of the cause of getting the jitter (Lip-Kai and Kok, 2009; Bianchi, 2005; Lip-Kai *et al*., 2007; Zheng and Lili, 2007). A precharged PFD shown in Fig. 2 is used instead of sequential PFD because it is simpler to design and has smaller dead zone. It consists of two D-type Flip-Flops (DFF). A AND gate has been used to function as a reset circuit when the reference clock is applied to PFD. The input signal is applied to one input of a PFD and other input is connected to the output

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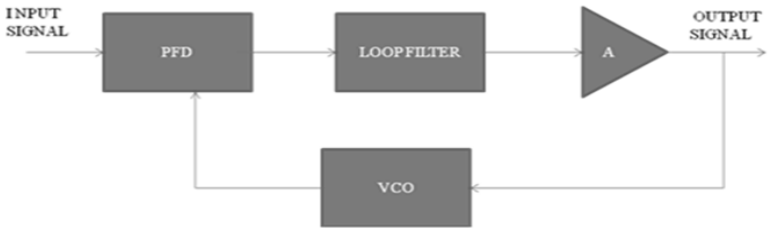

Fig. 1: Basic phase locked loop

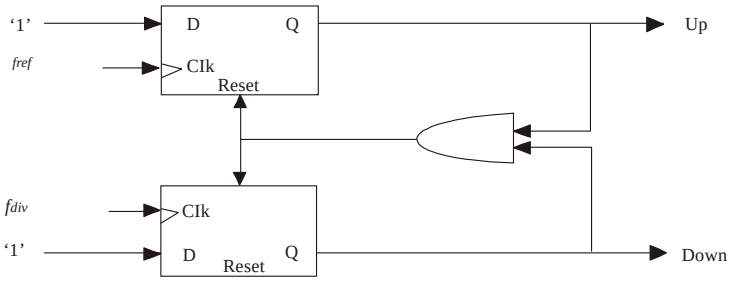

Fig. 2: Basic phase frequency detector

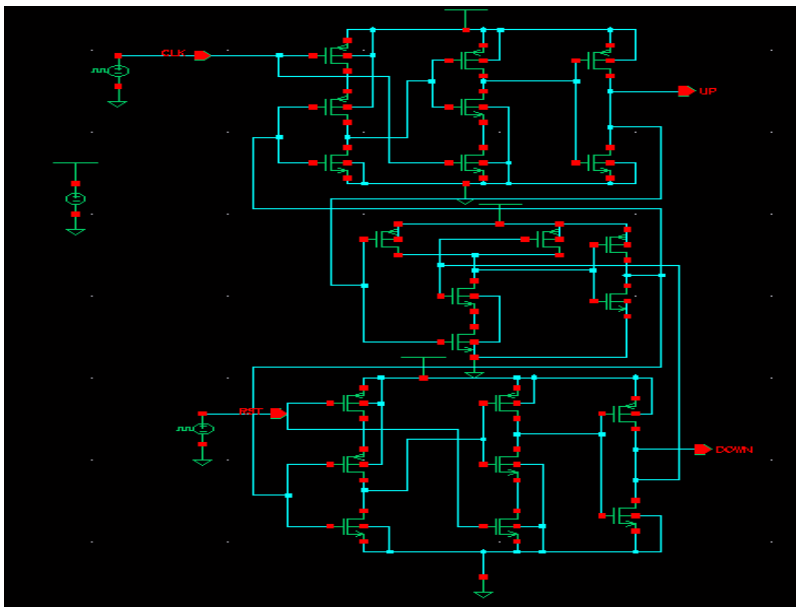

Fig. 3: Phase frequency detector

of a divide by N counter. The phase difference between two input signals, i.e., the reference signal and the N-counter output signal, can be processed by the PFD for getting the phase error relative to the input and reference frequency. After detecting the phase error in terms of voltage, PFD can generate two signals named as UP and DN, which are connected to the charge pump circuit. The delay time of logic components and reset time of feedback path of flip-flop causes a PFD to detect phase and frequency with distortion (Roland, 2003). The PFD doesn't generate wrong information and reduces the acquisition time drastically without fast locking skill (Arshak and Jafer, 2004). The proposed PFD logic is shown in Fig. 3.

Charge pump with loop filter: A charge pump in a PLL is an electronic switch that gives an output current, depending on the control signals from the phase detector.

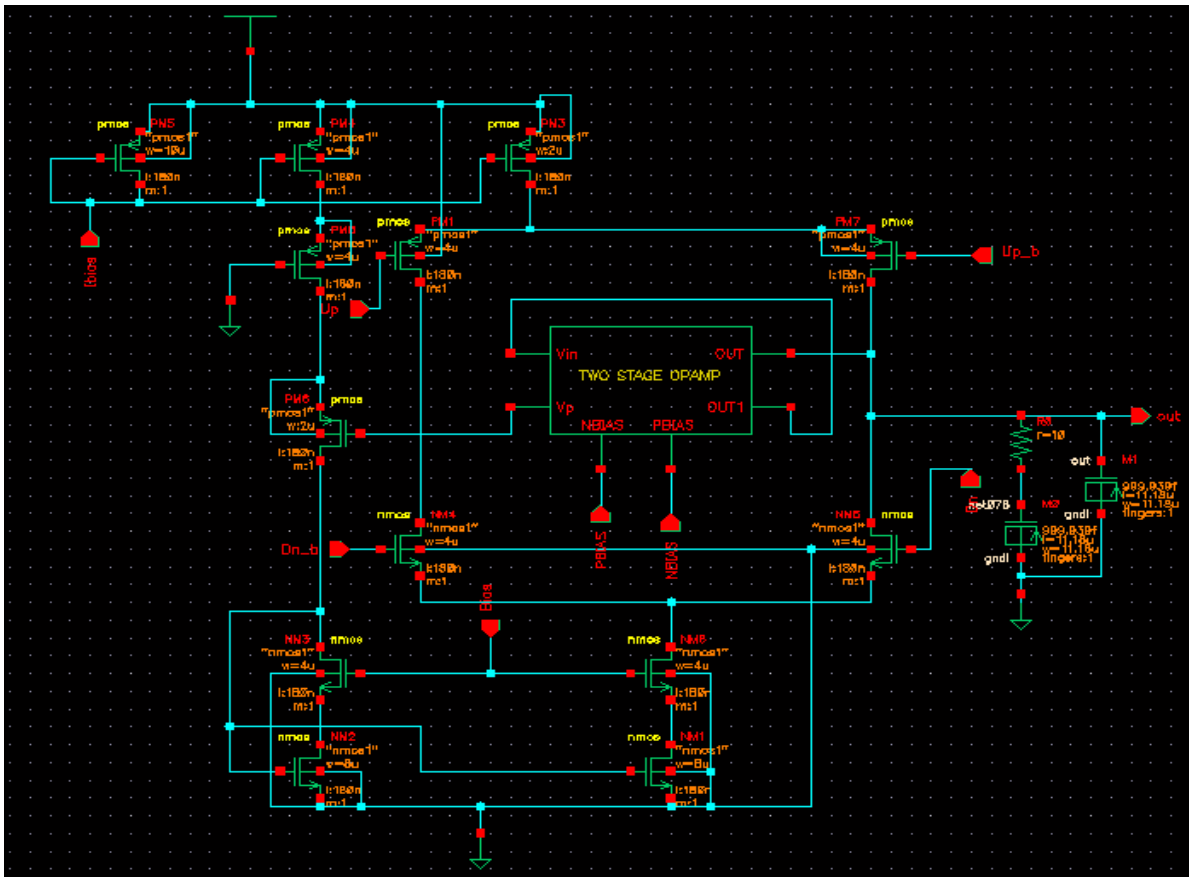

Fig. 4: Charge pump

Basic elements of charge pumps are current source, a current sink and switches. In conventional circuits of charge pump circuits, switches are replaced by pull up and pull down circuits in terms of NMOS and PMOS. To convert charge pump current to voltage\a charge pump is usually followed by a passive loop filter. Figure 4 shows the CP in which two stage op amps designed at 100 uA has been directly used because of high bandwidth. The VCO frequency and phase depends upon the control signal from the charge pump. A supply noise has been improved by adjusting the gain of voltage controlled oscillator at low level (Stephen *et al*., 2004). A current mismatch and current noise are the most important factor to study while designing the high performance CPPLL which deteriorates due to non-ideal charge pump effects. The transient responses of the charge pump degraded by increased parasitic capacitance coupling between the inputs and output of charge pump due to charge sharing and charge injection. The mismatch has been occurred due to difference in the charging and discharging currents of the charge pump. The long-channel transistors give the larger input capacitance and degrade the speed and power of the pump (Hwang *et al*., 2009). Current mismatch comes from device mismatch, channel-length modulation and parasitic capacitors. The proposed charge pump is shown in Fig. 4 at which gain at low frequencies has kept large so that the PLL can lock to the desired frequency at all occasions including different voltage and temperature conditions (Krzysztof *et al*., 2004; Daniels and Ronan, 2006). The Op-Amp has been designed and introduced into CP to increase the output impedance is shown in Fig. 5.

Ring oscillator: LC oscillators were giving low phase noise but due to the large die area utilization ring oscillators are used. The ring oscillators are utilizes less area as compared to LC oscillator but in a conventional oscillators it has been observed that many oscillators are not giving low phase noise at low power. Delay cell is based upon the differential buffer delay stage with symmetric loads and the outputs of the last stage are cross coupled with the inputs of the first stage (Keith *et al*.,

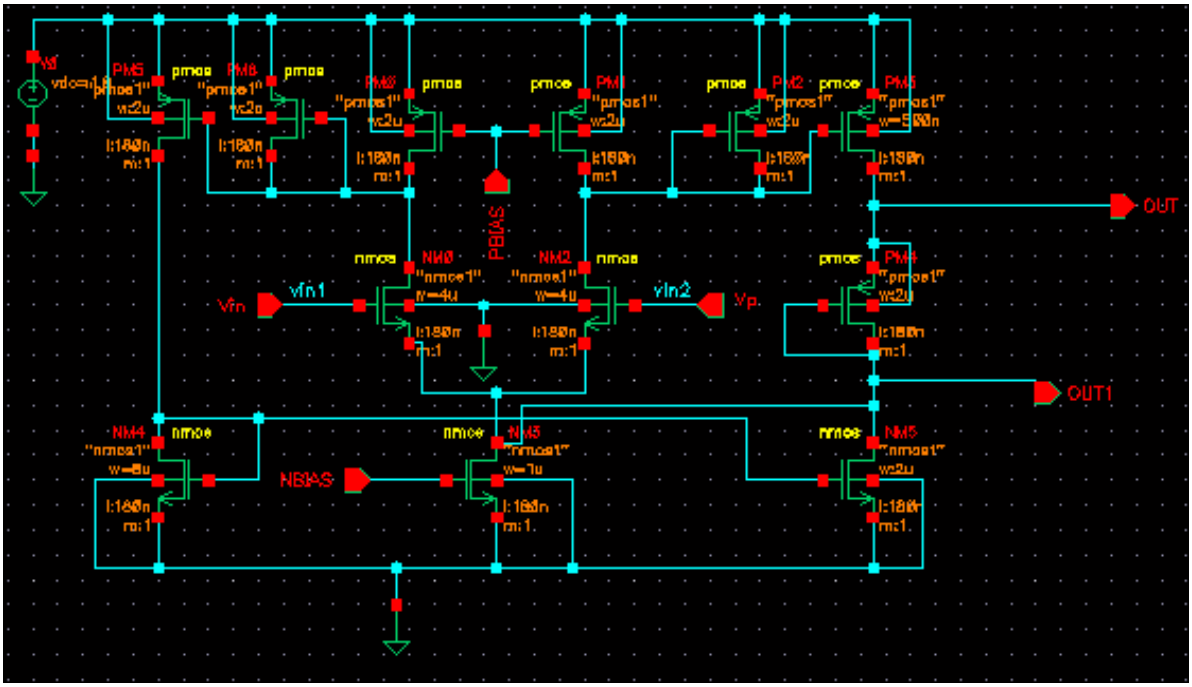

Fig. 5: Operational amplifier

2006; Chakraborty and Pal, 2007). To maintain a high current into the charge pump in order to get fast lock time of oscillator, it is must to decrease the oscillator gain (van de Beek and van der Weide, 2006; Rahajandraibe *et al*., 2007). A low power, low phase noise ring oscillator has been designed using three-stage delay element. To obtain an oscillation, the circuit should be with multiple pole stages, because as two significant pole systems gives frequency dependent phase shift of 180ºC due to the signal inversion from the gate to drain and three pole systems 270ºC. If three identical stages are used for the construction of ring oscillator, the minimum voltage gain per stage must be equal to unity (Razavi, 2001). The propagation delay of inverter is proportional to W/L ratio of the transistor as the delay adjustment is possible by varying W/L ratio (Chan-Hong and Beomsup, 1999; Dai and Ramesh, 2002; Tomar *et al*., 2007). To design Ring oscillator a new approach has been used in this study that is positive feedback and cross-coupled circuit which senses the voltage at the output. Generating an oscillation by ring oscillator based on the delay time and the number of stages of delay cell. Reduction of delay time of the ring oscillator was possible by adding a set of secondary inputs and switching these earlier than the primary inputs. Three stage and nine stage conventional ring oscillators designed have been giving the frequency ranges from 5.16-5.93 and 1.1-1.86 GHz, respectively (Yalcin and John, 2004). It means increasing the number of stages reduces the oscillation frequency. Figure 6 shows basic delay cell used in conventional three-stage (Fig. 7) to nine stage ring oscillators. The frequency of the oscillation is represented in Eq. (1):

$$fosc = \frac{1}{2N\tau} \& \tau = R_{eq}.C_{eq} \quad (1)$$

A VCO accepts the signal as a control signal from filter and accordingly gives the oscillations. Control voltage changes the frequency of the VCO in a direction that reduces the phase difference between the input signal and the local oscillator (Chel *et al*., 2004; Hwang *et al*., 2007). The primary loop connected as a normal differential and secondary loop connected output transfer function to reduce the slew time of the voltage controlled oscillator. To avoid the loss of oscillation pmos transistor PM3 and PM4 have been introduced in the proposed delay cell. By using PMOS which has usually slower switching time PMOS which enhances the rise time of the output, the phase noise of the overall VCO can be reduced.

Phase noise: A two crossed coupled buffers N_5 and N_6 have been used to improve the supply noise rejection and 1/f noise Due to periodic on-off switching in a MOS

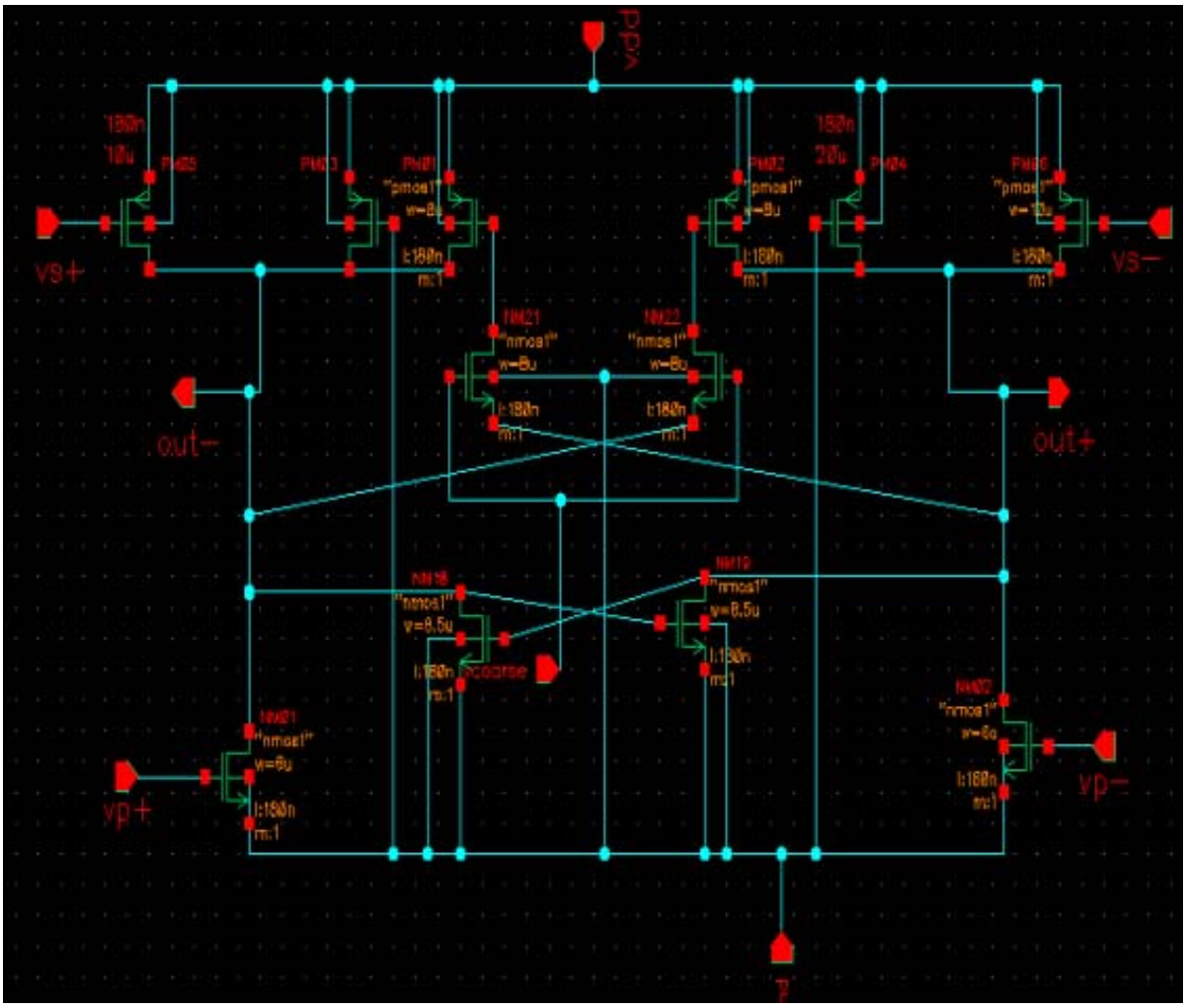

Fig. 6: Proposed delay cell for ring oscillator

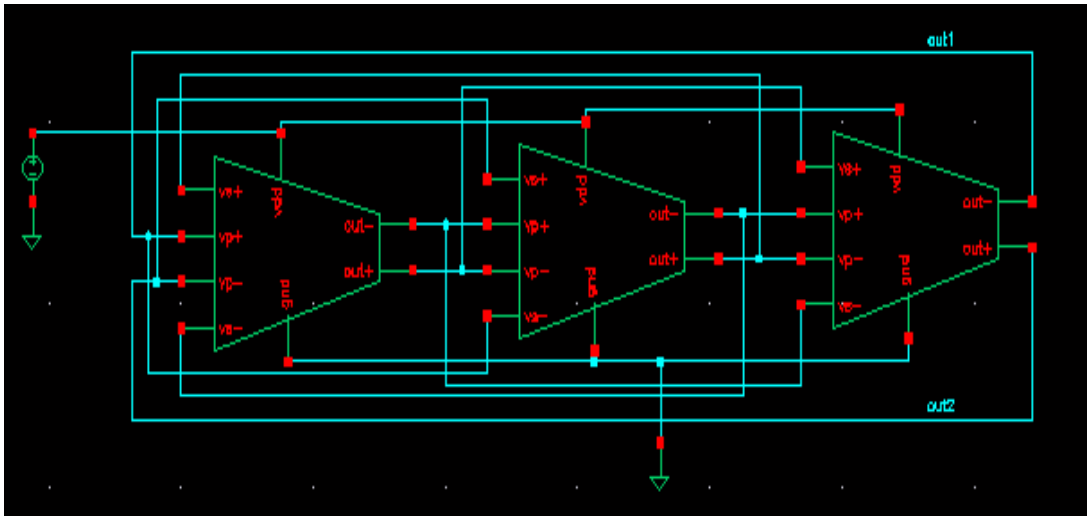

Fig. 7: Symbol of proposed three-stage ring oscillator

transistor 1/f noise in the on-state is reduced and the amount of reduction strongly depends on the gate-source voltage in the off-state and $1/f_3$ phase noise is dependent on the gate source voltage of the MOS transistor in the off state (Chan-Hong and Beomsup, 1998). The phase noise and figure of merit have been determined by the Eq. (2) (Liu *et al*., 2009) and Eq. (3) (Woogeun and Keith, 2008) and expressed in the result section:

$$L_{\min}(\Delta f) = 10\log\left[\frac{7.33kT}{P_{MIN}}\left(\frac{f0}{\Delta f}\right)^2\right] \quad (2)$$

$$FoM = L(\Delta f) - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_m W}{1_m W}\right) \quad (3)$$

where, FoM is the figure of merit of VCO, £ (Δf) is a measured phase noise in dBc/Hz.

Divider: To design integer-N frequency divider for getting the accurate frequency to PFD used in PLL in CMOS 180 nm technology to improve the high frequency characteristic has been carried out by by synchronous technique (Razavi, 2001; Pan and Tsutomu, 2007). The synchronous counter constitutes the critical element for good performance in terms of speed. A divide by 5 and divide-by-16 divider chip has been implemented with the help of DFF combination which is shown in Fig. 8. By selecting integer N of 5 as well as 16 by dynamic flip flops, the system made to very faster and more compact than the static ones (Weste and Eshragrian, 2001; Centurelli and Olivieri, 2004). The power consumption increases as input frequency increases. Integer-N divider

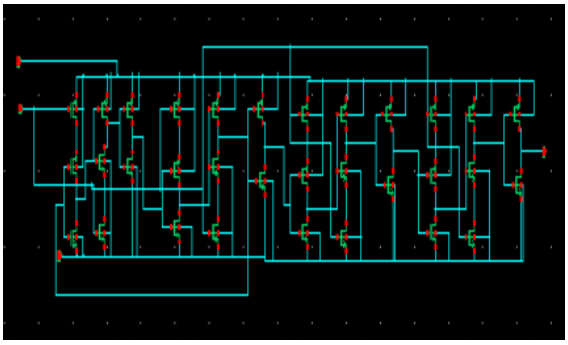

Fig. 8: Divide-by-5 and divide-by-16 logic

in a PLL is responsible on channel selection. It divides the output frequency with certain value according to reference frequency.

Complete PLL: The proposed components FD, CP, VCO and divider combined to form the complete PLL shown in Fig. 9. The PFD which has been used to complete the PLL is a giving the zero dead zone. According error signal from the PFD, CP either increases or decreases the amount of charge to the low pass filter. This charge either speeds up or slows down the VCO. The loop continues this process until the phase difference between the input reference signal and the feedback signal is zero. A frequency divider has been used in the feedback loop in order to synthesize a frequency that is different from that of the reference signal.

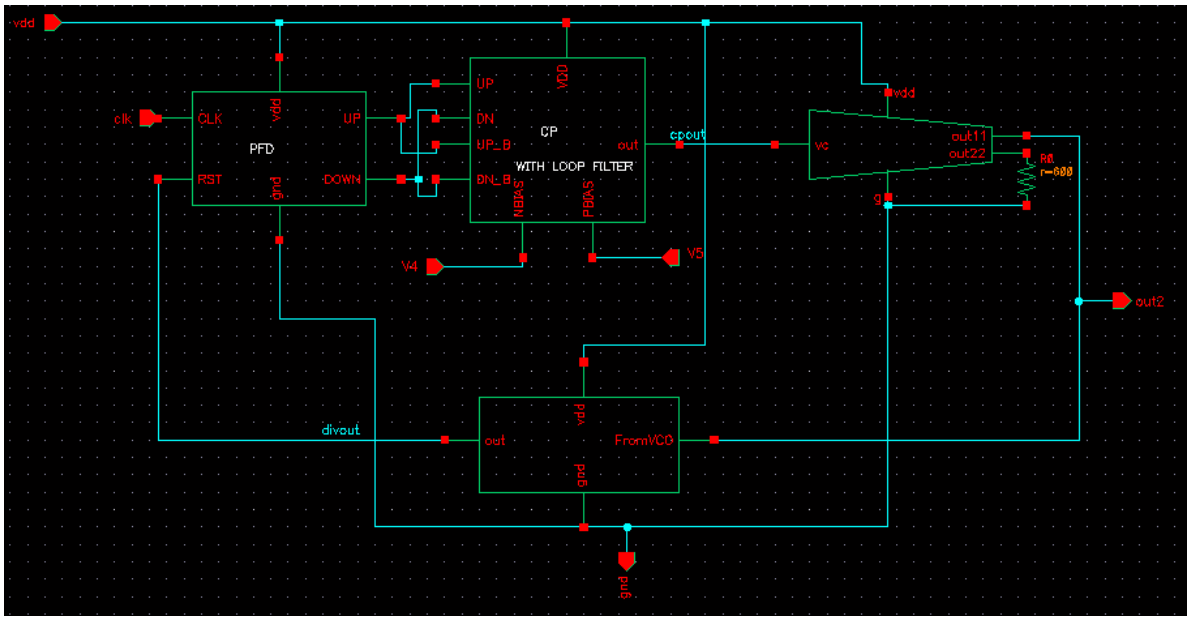

Fig. 9: Phase locked loop

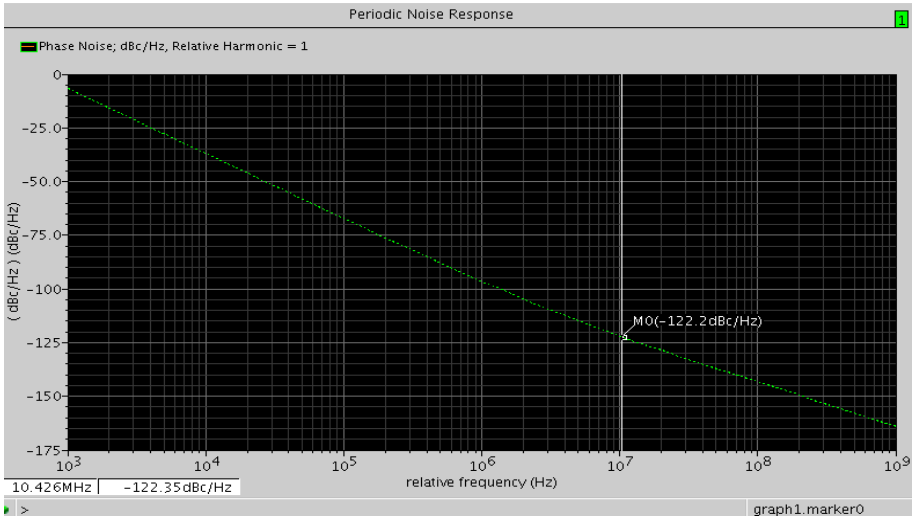

Fig. 10: Phase noise response of three-stage ring oscillator @10 MHz offset frequency

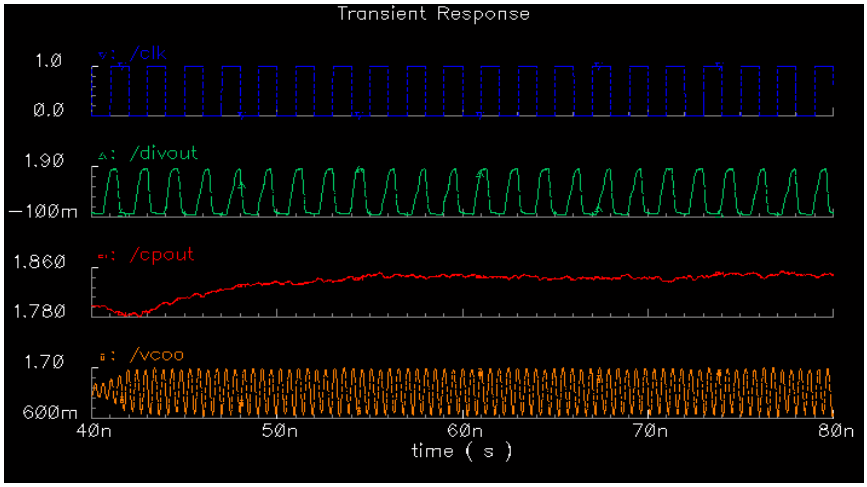

Fig. 11: Output waveforms of charge pump

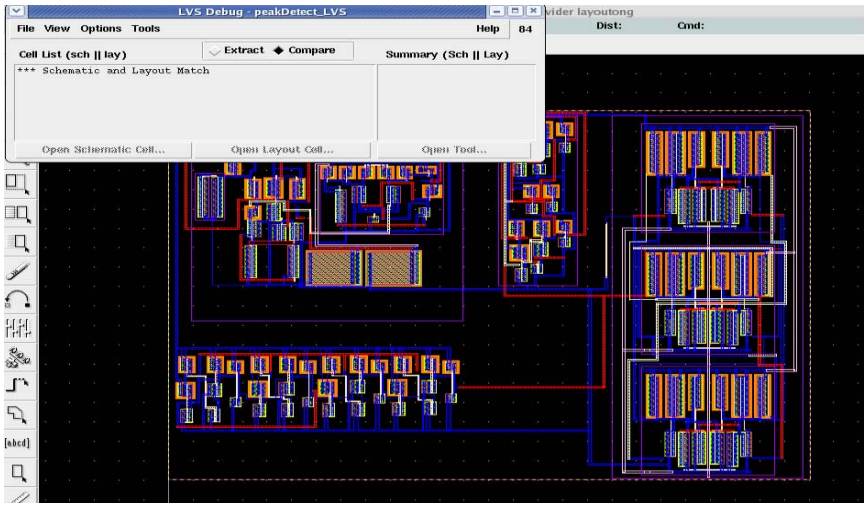

Fig. 12: Layout of complete PLL

Table 1: Phase noise versus control voltages

Sr. No	Vctrl (v)	Phase noise @1 MHz dBc/Hz	Phase noise @10 MHz dBc/Hz
1	0.93	5.0	0.1
2	1.15	-36.0	-45.0
3	1.58	-93.2	-122.0
	1.80	-93.2	-122.0

RESULTS AND WAVEFORMS

The PLL for high performance application have been designed using 180 nm CMOS technology with 36.516 mA. and simulated by Cadence SpectrRF. The phase noise obtained is-122.2 dBc/Hz @ 10 MHz offset frequency, which is shown in Fig. 10. The proposed voltage controlled oscillator has designed for getting optimized 2.4 GHz frequency. The charge pump has been designed for high gain, high band width which is shown in Fig. 4. A design has been completed with 180 nm CMOS technology and 1.8 Volt supply voltage. The final output waveform of complete PLL is shown in Fig. 11. The phase noise versus various controlled voltages is shown in Table 1. The figure of merit of PLL found to be-134 dBc/Hz. The layout of complete PLL is shown in Fig. 12. The total area required to implement the PLL without package is (0.093 X 0.09783 mm) 0.0091 mm^2.

CONCLUSION

The PLL has been designed with low power, small chip size area and better phase noise using 180 nm CMOS technology for high performance PLL and simulated by Cadence SpectreRF. While increasing the number of stages for getting the 2.4 GHz frequency frequency the power dissipation and size of oscillator was going to increase. Hence instead of increasing the number of stages and time constant again a Vctrl and width of the transistor can be adjusted for getting the 2.4 GHz frequency. To match the impedance a 120 and 600 ohm resistor have been connected to PLL output at different control voltages.

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