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Using One hot Residue (OHR) in Image Processing: Proposed a Scheme of Filtering in Spatial Domain

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Abstract: In this study, the use of the One Hot Residue (OHR) number system for digital image processing and its application for designing fast, high-speed and low area image processors are studied. Since digital image filtering in space domain requires many algebra computations, we're going to propose a system with high computing speed based on OHR. Using proposed system can significantly enhance the speed of the computation operations and hence the system. In the proposed image coding scheme the delay of implementation is equal to delay of a transistor which is a good improvement in compare with the conventional methods such as direct method. Other advantages of using One Hot Residue (OHR) number system are its simplicity of implementation and minimum power dissipation. Design of adder and multipliers commonly used for filtering with selected moduli set $\{2^{n-1}+1, 2^n-1, 2^n\}$ for one hot coding are presented here. MATLAB was used for simulation studies while VLSI tools have been employed for design analysis. The preliminary results show the capability of the proposed method to speed incensement of operation, decreasing of consumption power, facilitating designed hardware and finally decreasing chip production for image processing.

Keywords: Digital image processing, filtering, One Hot Residue (OHR) number system, space domain

INTRODUCTION

There is no doubt that every branch of science benefit from the processing of digital images. Digital images are currently widely considered in all aspects of technology development. Machine vision, satellite imaginary, medical applications, machine control products, military science and security, agriculture, urban design, graphic arts and multimedia are some examples of this category (Arnold, 2005; Mousavi and Taleshmekaeil, 2010). Due to the large volume of computational operations in digital image processing techniques, exploring a way to increase the processing speed and reduce power consumption seems to be essential. One hot encoding is a promising way in designing Integrated Circuits (ICs) with high speed and low power consumption. Using this method introduces the lowest delay for addition and multiplication operations in RNS moduli and hence will increase the speed and reduce power consumption of the image processing circuits (Jassbi *et al*., 2007; Hosseinzadeh *et al*., 2007).

In Labafniya and Eshghi (2010), new circuits for OHR addition and subtraction using one barrel shifter structure are proposed. The proposed circuits have reduced amount of hardware and are able to generate the addition and subtraction results simultaneously.

Hosseinzadeh *et al*. (2010) has proposed adder modulo (r^n-1) with improvements power consumption. The authors have reached a significant reduction of applied transistors by scarifying the speed of the circuit and increasing the delay to 4 times the conventional OHR adders. In this study, design of adder and multipliers commonly used for filtering with selected moduli set {2n-1+1, 2^n-1, 2^n} for one hot coding are presented.

FILTERING OF DIGITAL IMAGES

One of the most important operations in processing digital images is the image convolution operation. Convolving digital images and the selected mask for many applications results in sharpening, noise removing and edge detection.

To display a grey scale image, a 2-D array (matrix) M*N is used where each index represents the brightness level of that point in the image. The eight-bit grey value of each array element has a value between zero and 255. An image can be represented in MATLAB as below (Taleshmekaeil and Mousavi, 2010):

$$F(x,y) = \begin{Bmatrix} F(1,2) & F(1,1) & & F(1,N) \\ F(2,1) & F(2,2) & \dots & F(2,N) \\ & & \vdots & \\ F(M,1) & F(M,2) & \dots & F(M,N) \end{Bmatrix} \quad (1)$$

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Table 1: Decimal, binary and one hot residue moduli mi

Decimal	Binary	One-hot
0	000…00	1000…0
1	000…01	0100…0
2	000…10	0010....0
.	.	.
.	.	.
.	.	.
m^i-1	000…01	0000…1

Convolution based image processing can be applied either directly like Fourier transforms or indirectly as Hartley transform. It states that element wise multiplications of two transformed sequences correspond to a cyclic convolution in the spatial domain. The transforms directly possessing the convolution property can be defined generically as Wang and Swamy (2004):

$$X_k = \sum_{n=0}^{N-1} X_n W^{kn}$$

$$k = 0\ldots N-1 \qquad (2)$$

where, N is the transform length, X_n is the sequence to be transformed, X_k is the transformed sequence and w is the transform kernel.

One hot residue number system: One way to increase the speed of adding operation is using one hot encoding. To represent the numbers in this system, m signals are used for m modulus where at each clock cycle only one signal is high (active) and other signals are low (deactivate). Each active signal is the respective residue in that moduli set Toivonen and Heikkila (2006). Table 1 shows decimal, binary and one hot residue moduli m_i:

To represent the numbers in this system, the residues modulo m_i are from zero to m_{i-1}. Implementation of circuits using OHR number system is simple and has regular structure since implementation of the adders using one hot system can be done by shift and rotates (Ammar *et al*., 2001).

Structure of one hot adder for modulo m_i: In this structure, the first input is shifted according to the value of the second input and the result will be revealed at the output. The delay of this operation is equal to delay of a transistor. For subtraction it is needed to reverse shift the first input data respecting to the value of the second input. Difficulties in implementing these types of circuits with one hot system are for large moduli sets since the number of transistors is increased exponentially. Hence they are not usually recommended for large moduli sets (Pirsch and Stolberg, 1998). Figure 1a shows two entries for a moduli m_i OHR adder: data entry and shift entry and Fig. 1b illustrates how all operands are related to each other on the base of reminders (Jassbi *et al*., 2010).

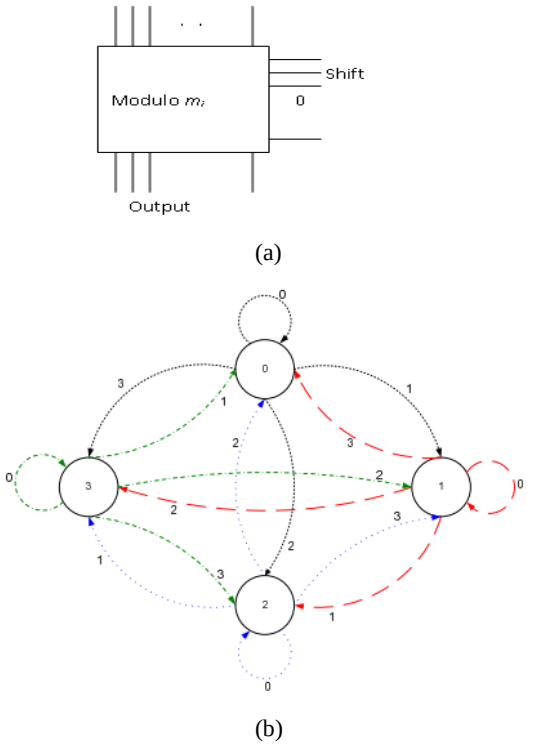

Fig. 1: (a) Block diagram of the one hot adder, (b) Addition position for moduli four

PROPOSED FILTERING OPERATION:

Considering that the number of pixel values in a digital image is too much, a huge number of multiplications and additions of pixel values and the mask values is needed in digital filtering operations. As a result, implementation of the filtering operation, or general operations related to processing digital images require a lot of overhead in processing speed and consumed power. Hence, we should seek ways for processing operation in which multiplication and addition of pixel values can be done with high speed and low power consumption.

Since the values of image pixels are in a limited range, we intended to employ the OHR number systems that feature minimal power consumption and high speed of processing in the range of pixel values. The OHR number system has a delay as small as delay of a transistor. Additionally, because only one signal is active at each clock cycle, power consumption is at its minimum and arithmetic operations are done with more speed. All these advantages make the use of one hot encoding for implementation of convolution operations efficient.

Designing B/R and R/B converter circuits: For convolution operations using OHR number system, we need circuits to convert binary numbers to OHR number

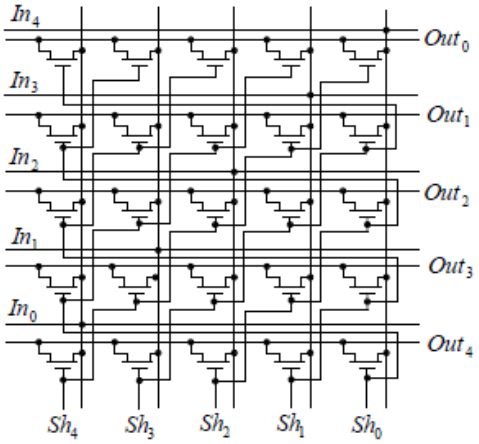

Fig. 2: Structure of the one hot moduli 5 adder

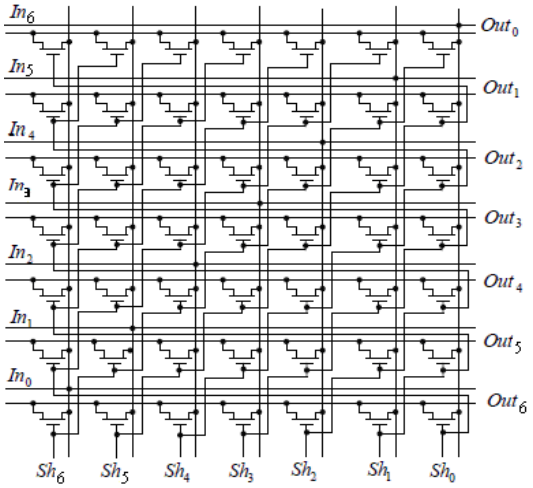

Fig. 3: Structure of the one hot moduli 7 adder

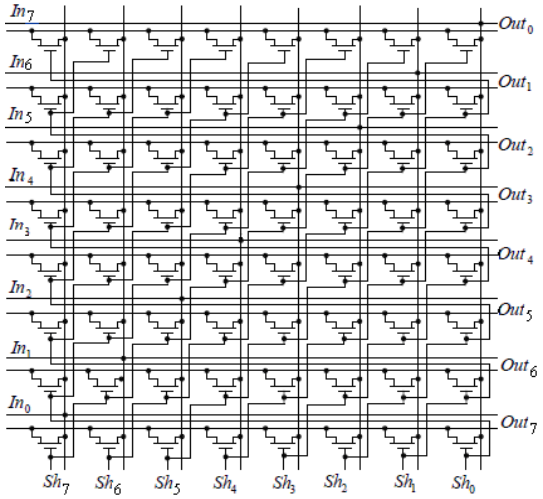

Fig. 4: Structure of the one hot moduli 8 adder

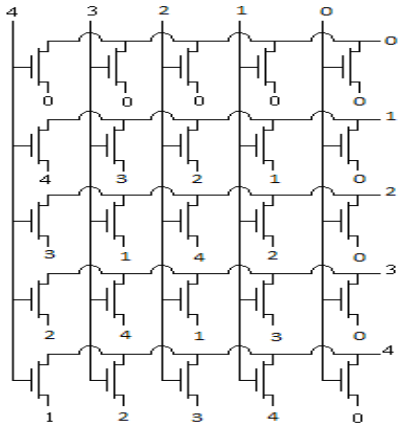

Fig. 5: Structure of one hot moduli 5 multiplier

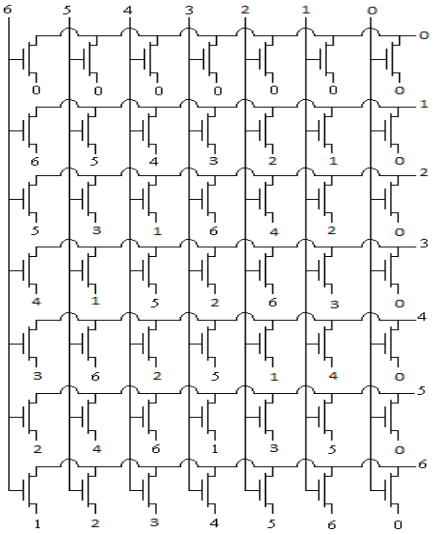

Fig. 6: Structure of one hot moduli 7 multiplier

and vice versa. Converters can be designed to get the pixel values and convert them to OHR and then perform convolution operation on the residues using one hot adder and multipliers and then the resulting values must be converted back to binary weighted system.
So this process is divided into three main parts:

- Converting pixel values from binary numbers to OHR (B/R converter)
- Image convolution operations using one hot multipliers and adders
- Convert the results from OHR back to binary numbers (R/B converter)

For conversion from binary to OHR, image pixels must be read first and then be converted to the OHR with the appropriate moduli set which is suitable for the pixels of digital images. In R/B converters, the results of the

Table 2: Comparison of performance of different arithmetic demos for digital image processing

	Implementation complexity	Delay	Speed of operations	Power consumption
Binary	high	very high (maximum number of bits) (8δ)	low	high
RNS	medium	high (maximum number of bits selected module)(3δ)	medium	medium
OHRNS	low	low (delay of a transistor)	high	low

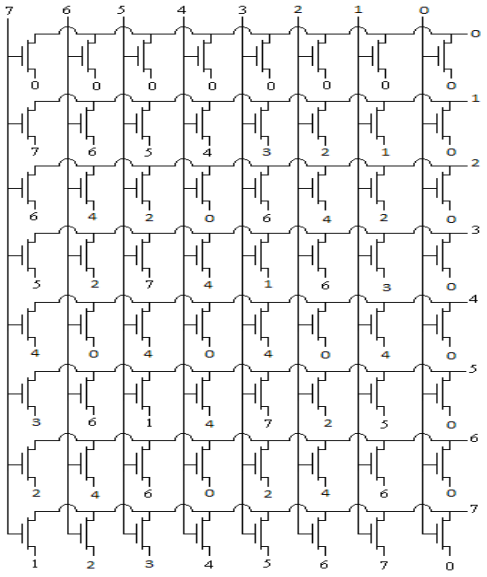

Fig. 7: Structure of one hot moduli 8 multiplier

filtering on images should be converted back to binary representation.

Moduli set selection: Moduli set selection and dynamic range has direct effect on speed of the process and implementation of efficient VLSI circuits for B/R and R/B converters. Since the values of picture elements (pixels) in images have limited grey levels ranged between zero and 255, so to set up the system in OHR we should choose moduli set in a way that it cover the pixels of digital images.

The best moduli set for digital image processing operations are $\{2^{n-1}+1, 2^n-1, 2^n\}$. For n = 3 the moduli set is {5, 7, 8}. This moduli set has dynamic range M = 5*7*8 = 280, i.e., [0, M) is a range of numbers that certainly will cover digital image pixel values.

Design one hot adder and multiplier for selected moduli set: Given the selected moduli set of {5, 7, 8}, so the circuits of adders and multipliers should be designed and implemented according to the given moduli set. Adder and multiplier moduli 5, 7 and 8 are depicted in Fig. 2-4 and 5-7, respectively:

Comparison: Since the number of adding and multiplying operations for digital image filtering is very high, further comparisons have been done based on the time of these operations. If any delay of the carry is considered as δ, addition operation for the binary numeral system, for an 8-bit grey scale image introduces a delay of 8δ to the system.

However, the delay of computation in residue number systems for the selected moduli set {5, 7, 8} is equal to the delay for the maximum modulus (3δ) and the delay for the proposed OHR system is equal to delay of one transistor. Table 2 compares some performance criteria's of one hot system with conventional numerical systems that are used for digital image processing. OHR system has higher computational speed, lower power consumption and also simple structure in hardware implementation.

CONCLUSION

Since adding and multiplying operations in digital image filtering introduces a huge overhead in processing speed and power consumption, arithmetic operations are performed using proposed one hot adder and multiplier which has only a delay of one transistor on each operation. The proposed system is fast and also because only one signal is active at each clock cycle, the power consumption is less. This system is very simple and has regular structure for the proposed moduli set. All these advantages make the use of one hot encoding the best choice for implementation of circuits that can be used for processing of digital images. The proposed system can also be used for any other types of images.

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