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A Hybrid SET/MOS (7, 3) Counter Circuit Based on Threshold Logic Gates

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Abstract: In this study, we present a threshold logic gate based implementation of a (7, 3) counter using Single-electron Transistor (SET) and Mtal-oxide-Semiconductor (MOS) transistor. The unique properties of the SET/MOS hybrid circuit are exploited in the realization of power and area efficient threshold logic gates. It is merely composed of three threshold logic gates and two inverters. The total device count is substantially reduced to 13, i.e. 5 PMOS transistors, 5 NMOS transistors, and 3 SETs, while the conventional Boolean logic gate based (7, 3) counter designed only by MOS transistors consumes nearly 194 devices. Moreover, the power consumption of the proposed (7, 3) counter is only 6.92 nW. The correctness of the proposed circuit is verified through HSPICE simulation. Simulation results show that the proposed (7, 3) counter is superior to the Boolean logic gate based CMOS one in terms of circuit complexity and area efficiency. These features make the proposed (7, 3) counter very attractive in the applications of multiplier circuits and other high density and high performance digital circuits.

Key words: Counter, HSPICE simulation, hybrid SET/MOS circuit, threshold logic

INTRODUCTION

As the CMOS technology is expected to reach its physical limits, many nanoscale devices have been intensively investigated as the alternatives of the MOS transistors to enhance the future circuit design to overcome the physical limitations (Zheng and Huang, 2009). Such novel devices include quantum cellular automata (QCA) (Porod *et al*., 1999), resonant tunneling diodes (RTD) (Mazumder *et al*., 1998), and single-electron tunneling devices (Chen *et al*., 1996). Many novel circuit structures have been proposed to implement the nanodevices. Among those novel structures, the hybrid MOS/nanodevice structure is much more attractive as it combines the novel properties of nanodevices with those of the MOS transistors. Moreover, the fabrication process of the hybrid structure is highly compatible with the current IC technology, which enables the hybrid structure to utilize the advantages of the CMOS's large-scale infrastructure, proven design methodologies, and economic predictability (Santanu and Adrian, 2006).

The emerging of nanoscale devices not only introduce the power and area efficient circuits but also provides a revision of the conventional computation models and digital methodologies. The threshold logic is such a typical example. Although the threshold logic exhibits powerful computational properties, it is rarely implemented in the conventional CMOS circuits for the reason that the implementation of the threshold logic in CMOS is expensive (Rajendran *et al*., 2010). However, this scenario can be changed as the novel nanodevices provide full supports for the implementation of the threshold logic. The unique characteristics of the novel devices are fully demonstrated in the implementation of the threshold logic. The threshold logic is expected to greatly improve the circuit functionalities while substantially reduce the complexities.

HYBRID SET/MOS (7, 3) COUNTER

The threshold logic is more powerful than the conventional Boolean logic, which is able to implement more complex functions using a smaller number of devices. The fundamental operation of the threshold logic is to compute the weighted sum of its inputs and compare the sum with a threshold value θ. If the sum is larger than θ, the output is logic '1', otherwise the output will be logic '0'. The threshold logic function is given as:

$$F(x) = \mathrm{sgn}\left(\sum_{i=1}^{n} w_i x_i - \theta\right) = \begin{cases} 1, & \sum_{i=1}^{n} w_i x_i \geq \theta \\ 0, & otherwise \end{cases} \quad (1)$$

where x_i represents the input variables, w_i represents the inputs weight corresponding to x_i, and n is the number of inputs. The symbol of the threshold logic gate with n binary inputs and a threshold θ is shown in Fig. 1.

Counter is one of the most important components in the arithmetic circuit, which generates a binary encoded output vector corresponding to the number of logic '1's in

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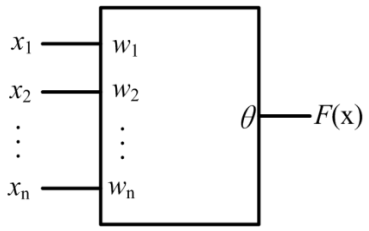

Fig. 1: Symbol of the threshold logic gate

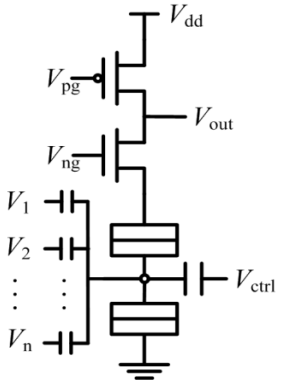

Fig. 2: Schematic of the multi-input hybrid SET/MOS circuit

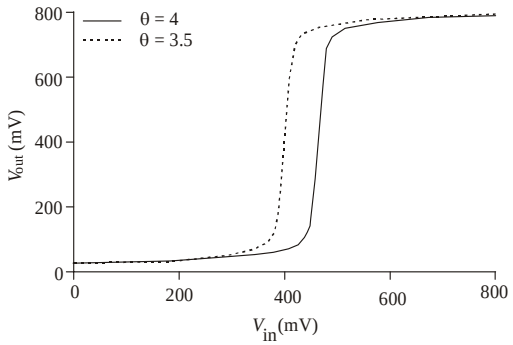

Fig. 3: The threshold operation of O_2

the input vectors. Counter has a wide range of applications including the parallel multipliers, multi-input adders, and digital signal processing applications (Leblebici *et al.*, 1996). A (7, 3) counter counts the number of logic '1's in its 7 inputs (X_0, X_1, …, X_6) and encodes the result as a 3-bit binary number output denoted as (O_2, O_1, O_0). The threshold logic equations of the (7, 3) counter are given below (Leblebici *et al*., 1996):

$$\overline{O}_2 = \text{sgn}(\sum_{i=0}^{6} X_i - 4) \quad (2)$$

$$\overline{O}_1 = \text{sgn}(\sum_{i=0}^{6} X_i - 4O_2 - 2) \quad (3)$$

$$O_0 = \text{sgn}(\sum_{i=0}^{6} X_i - 4\overline{O}_2 - 2\overline{O}_1 - 1) \quad (4)$$

In this study, we implement the threshold logic equations of the (7, 3) counter using the SET/MOS hybrid circuit. Figure 2 illustrates the schematic of a multi-input hybrid SET/MOS circuit, which is originated from the universal literal gate proposed by (Inokawa *et al*., 2003). It comprises a PMOS transistor, an NMOS transistor, and an SET. In this structure, multi-inputs can be coupled to the Coulomb island of SET through capacitors. The circuit is capable of handling multiple inputs simultaneously. Thus, we exploit the multi-input characteristic of the circuit to realize the threshold function. We apply the inputs of the (7, 3) counter to the structure and set the capacitance of the coupling capacitors to represent the corresponding input weights. Hence, the weighted sum of the inputs is calculated by the capacitor array. With proper device parameters, the circuit has a threshold voltage and performs the threshold operation. Therefore, its output is generated by comparing the weighted sum of its inputs with the threshold value.

Since the negative weights in Eq. (3) and (4) can't be directly implemented by the SET/MOS hybrid circuit, $-O_2$,$-O_1$ are replaced by the equivalent expressions $\overline{O}_2 - 1, \overline{O}_1 - 1$, respectively. Hence, Eq. (3) and (4) are rewritten as:

$$O_1 = \text{sgn}(\sum_{i=0}^{6} X_i + 4\overline{O}_2 - 6) \quad (5)$$

$$O_0 = \text{sgn}(\sum_{i=0}^{6} X_i + 4\overline{O}_2 + 2\overline{O}_1 - 7) \quad (6)$$

Meanwhile, the threshold operation performed by the hybrid SET/MOS circuit is mainly based on the inverting characteristic of the input-output voltages, as shown in the Fig. 3. The solid line shows the threshold function of O_2. As can be observed, when the sum of inputs (V_{in}) reaches the threshold value of 4, the corresponding output voltage is only 0.4V which is not the expected output logic (logic '1') according to O_2. This is because the inverting characteristic is not stiff enough to sharply shift the output (V_{out}) from logic '0' to logic '1'. There remains a voltage transition margin, which leads to the malfunction of the circuit when the input voltage is within the transition margin. Thus, we change the threshold value from 4 to 3.5 in order to avoid that the input voltage has the value in the transition margin, while the logic function of O_2 remains the same. Hence, the inverting characteristic with the threshold value of 4 is shifted to the left as shown in Fig. 3 (the dot line). Although the voltage transition margin still exists, the circuit can have the correct

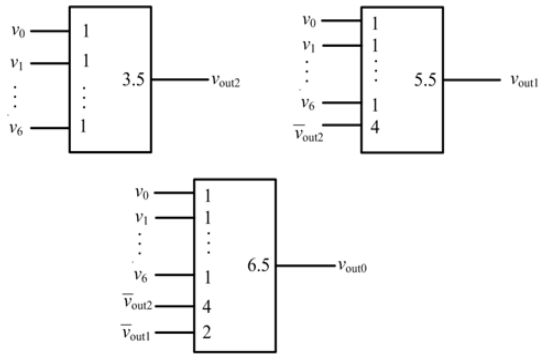

Fig. 4: Schematic of the threshold logic gate based hybrid SET/MOS (7, 3) counter

correct operation as the input value of 4 is beyond the transition area. As can be seen, when the sum of inputs reaches 4, the output voltage is 0.74V (logic '1'), which is the expected output logic. Therefore, the circuit has the correct operation. With the same method, we change the threshold value of O_1 and O_0 from 6 and 7 to 5.5 and 6.5, respectively. Hence, the final threshold logic expressions of the (7, 3) counter are described as:

$$O_2 = \mathrm{sgn}(\sum_{i=0}^{6} X_i - 3.5) \quad (7)$$

$$O_1 = \mathrm{sgn}(\sum_{i=0}^{6} X_i + 4\overline{O}_2 - 5.5) \quad (8)$$

$$\overline{O}_0 = \mathrm{sgn}(\sum_{i=0}^{6} X_i + 4\overline{O}_2 + 2\overline{O}_1 - 6.5) \quad (9)$$

The schematic of the proposed threshold logic gate based hybrid SET/MOS (7, 3) counter is illustrated in Fig. 4. As can be observed, the (7, 3) counter is composed of three threshold logic gates with different threshold values. The outputs V_{out2}, V_{out1}, V_{out0} correspond to the O_2, O_1, O_0 in Eq. (7), (8) and (9), respectively. The weights of the seven inputs V_0, V_1,…,V_6 are all 1, while the inverted outputs $\overline{V}_{out2}$,$\overline{V}_{out1}$ are with the input weight of 4, 2, respectively. The inversions of V_{out2}, V_{out1} are realized by the standard CMOS inverters.

RESULTS AND DISCUSSION

SET circuits are usually simulated by SIMON, a simulator only for single electron circuits (Wasshuber *et al*., 1997). As SIMON has no co-simulation environment with MOS devices, it couldn't be used to simulate the hybrid SET/MOS circuit. However, if the SET can be considered as an independent element and described by the SPICE macro model, the hybrid circuit can be simulated by the SPICE simulator. As shown in Fig. 2, the source and drain of SET are connected to the ground and source of the NMOS transistor, respectively. The capacitance of the connection node between the SET and NMOS transistor is much

Table 1: Device parameters for SPICE simulation

Temperature		300K
PMOS	W_p	22nm
	L_p	154nm
	V_{pg}	0.4V
NMOS	W_n	22nm
	L_n	154nm
	V_{ng}	0.4V
SET	C_s, C_d	0.1aF
	R_s , R_d	600 KΩ
	V_{ctrl}	0.762V
	C_{ctrl}	0.1050aF
	C_2	0.0150aF
	C_1	0.0095aF
	C_0	0.0080aF

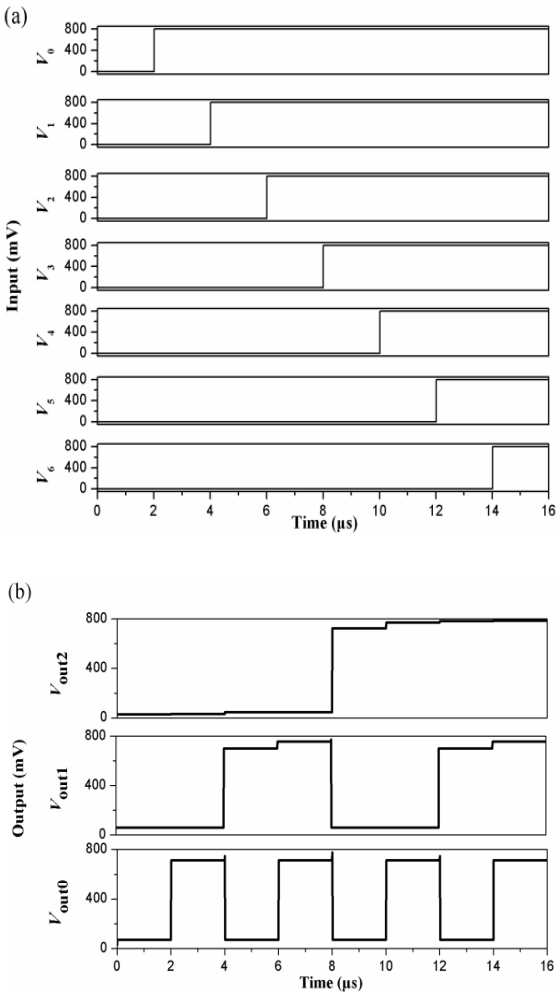

Fig. 5: Simulation result of the proposed (7, 3) counter (a) the waveforms of seven inputs, (b) the waveforms of three outputs

larger than that of tunneling junctions. Thus, we can consider the SET as an independent element. Therefore, it's possible to describe the SET by the SPICE macro model and simulate the whole circuit by the SPICE simulator.

In this study, the compact macro model (Inokawa and Takahashi, 2003a) is used to describe the behavior of SET, whose accuracy has been verified by SIMON and experiments (Inokawa and Takahashi, 2003b). The predictive technology model for high performance applications of 22-nm MOS transistor (Zhao and Cao, 2006) is used to simulate the behavior of MOS transistors. The performance of the hybrid SET/MOS (7, 3) counter is simulated by the HSPICE simulator. The three threshold logic gates all have the same device parameters except for the coupling capacitors C_2, C_1, C_0, corresponding to V_{out2}, V_{out1}, V_{out0} respectively. The main device parameters used in SPICE simulation are given in Table 1.

The simulation results of the (7, 3) counter are depicted in Fig. 5. The inputs are rectangular pulses, whose value of 0V and 0.8V are set for logic '0' and logic '1', respectively. The input waveforms take into account the seven possible states of inputs. The 3-bit binary number encoded output is generated as shown in Fig. 5(b). As can be seen, the outputs of the (7, 3) counter depend on the number of logic '1's in its 7 inputs. Simulation results show that the proposed circuit can well realize the function of counting the number of logic '1's in its 7 inputs and encoding the results in the outputs with a 3-bit binary number.

The proposed (7, 3) counter consists of three threshold logic gates and two inverters. The total device count is only 13, i.e. 5 PMOS transistors, 5 NMOS transistors, and 3 SETs, while the conventional Boolean logic gate based (7, 3) counter designed only by MOS transistors consumes nearly 194 devices (Inokawa *et al.*, 2004). Moreover, the power dissipation of the proposed (7, 3) counter is only 6.92 nW. Compared to the Boolean logic gate based CMOS (7, 3) counter, the proposed circuit consumes much less area and provides a simpler and compacter structure. The proposed threshold logic gate based (7, 3) counter offers a wide range of applications such as the parallel multipliers, multi-input adders, and digital signal processing applications.

CONCLUSION

In this study, a threshold logic gate based implementation of a (7, 3) counter with SET/MOS hybrid circuits is proposed. We leverage the unique properties of the SET/MOS hybrid circuit to implement the power and area efficient threshold logic gates. The threshold logic gate has the capability of implementing complex logic functions with a smaller number of devices. The proposed circuit is composed of three threshold logic gates and two inverters. The total device count is greatly reduced to 13, i.e., 5 PMOS transistors, 5 NMOS transistors, and 3 SETs, while the conventional Boolean logic gate based (7, 3) counter designed only by MOS transistors consumes nearly 194 devices. The performance of the hybrid SET/MOS (7, 3) counter is evaluated through HSPICE simulation. Simulation results show that the power consumption of the proposed (7, 3) counter is only 6.92nW. When compared to the Boolean logic gate based CMOS (7, 3) counter, the proposed circuit has a simpler circuit structure and smaller area consumption. These features make it very attractive in the design of multiplier circuits and other high density and high performance digital circuits.

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