

Single Core Hardware Modeling of Built-in-Self-Test for System on Chip Design

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Abstract: This study describes a hardware modeling environment of built-in-self-test (BIST) for System on Chip (SOC) testing to ease the description, verification, simulation and hardware realization on Altera FLEX10K FPGA device. The very high speed hardware description language (VHDL) model defines a main block, which describe the BIST for SOC through a behavioral and structural description. The three modules test vector generator, circuit under test and response analyzer is connected using its structural description. 8-bit pseudorandom test vector generator is a linear feedback shift register circuit consists of D latches and XOR gates produces 255 different patterns of test vectors for CUT which consists of a 3 to 8 line decoder and a 4 bit adder circuit. In response analyzer, the multiple-input pattern compressor circuit is used to produce signature and a comparator circuit is used for signature analysis. The design is modularized and each module is modeled individually using hardware description language VHDL. This is followed by the timing analysis and circuit synthesis for the validation, functionality and performance of the designated circuit, which supports the practicality, advantages and effectiveness of the proposed hardware realization for the applications with a maximum clock frequency of 31.4 MHz.

Key words: Built-in-self-test, circuit under test, design for testability, latches, system on chip, VHDL

INTRODUCTION

One of the most widely researched self-testing techniques is built-in-self-test (BIST), which uses embedded hardware test generators and test response analyzers to generate and apply test patterns on-chip at the speed of the circuit, thereby eliminating the need for an external tester (Yuejian *et al.*, 2011; Tseng *et al.*, 2010). BIST techniques can be classified into two categories, namely on-line BIST and off-line BIST (Lusco *et al.*, 2011; Abramovici, 1990). Embedded BIST functions match the chip's capabilities, which can make them very effective testing mechanisms. Also, BIST stays with the chip throughout its life. Moreover, the addition of BIST features to electronics hardware frequently doesn't significantly increase a product's size, cost, and production time, as was the case in the past.

Adopting BIST and DFT (Design for Testability) is accompanied by size overhead and delay. But many companies are adopting them to reduce the testing cost. For example, Intel is adopting the BIST (Built-In Self Test) technique from 80386, boundary scan in the Pentium processors (Needham and Gollakota, 1996). Sun microsystems were adopting the BIST technique and boundary scan in the SuperSPARC and SuperSPARCII (Rajiv and Yarlakadda, 1993; Hong and Avra, 1995).

FPGA offers a potential alternative to speed up the hardware realization. From the perspective of computer-aided design, FPGA comes with the merits of lower cost, higher density, and shorter design cycle. It comprises a wide variety of building blocks. Each block consists of programmable look-up table and storage registers, where interconnections among these blocks are programmed through the hardware description language (Reaz *et al.*, 2007). This programmability and simplicity of FPGA made it favorable for prototyping digital system. FPGA allows the users to easily and inexpensively realize their own logic networks in hardware. FPGA also allows modifying the algorithm easily and the design time frame for the hardware becomes shorter by using FPGA (Akter *et al.*, 2008).

Several methodologies for testing of microprocessors have been presented in recent years and almost these methods have area and performance overhead (Shen and Su, 1988; Talkhan *et al.*, 1989; Hetherington *et al.*, 1995). Since the need for self testing is most acute for high performance processors, this research propose a model of built-in-self-test for system on chip using VHDL. The use of VHDL for modeling is especially appealing since it provides a formal description of the system and allows the use of specific description styles to cover the different abstraction levels (architectural, register transfer and logic

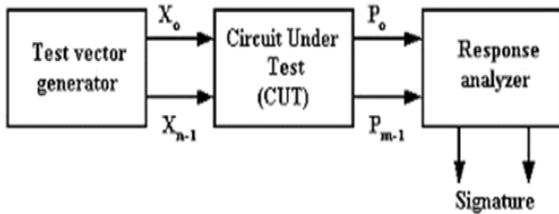


Fig. 1: Block representation of built-in-self-test

level) employed in the design (Yasin *et al.*, 2004; Zamfirescu, 1993). In the computation of method, the problem is first divided into small pieces; each can be seen as a submodule in VHDL. Following the software verification of each submodule, the synthesis is then activated. It performs the translations of hardware description language code into an equivalent netlist of digital cells. The synthesis helps integrate the design work and provides a higher feasibility to explore a far wider range of architectural alternative (Reaz *et al.*, 2003).

This research project is targeted to develop a Single Core Hardware Modeling of Built-in-self-test for System on Chip Design. In order to fulfill the objective, this research has taken the strategy of a top-down design process. The design is broken up into small blocks for the easy hardware implementation. The method provides a systematic approach for hardware modeling, facilitating the rapid prototyping of the Built-in-self-test for System on Chip Design.

MATERIALS AND METHODS

Design for Testability (DFT) and built-in-self-test (BIST) techniques for analogue and mixed signal circuits have recently been attracting considerable industrial interest for helping alleviate increasing test related difficulties. Testability is predicted to become a primary design specification and has to be addresses in the early design stages, as escalating test time and costs need to be controlled and quality levels improved. In addition to improved manufacturing test, BIST offers an extension towards in-field verification while also allowing test reuse and providing a promising approach to automate mixed signal test generation. The study was conducted at the System Design lab, Universiti Kebangsaan Malaysia in the middle of 2010. This paper describes a VHDL model of built-in-self-test for system on chip design. The model is well off with the following principles:

- Test sequences are generated directly on a chip
- Output test responses or their compact characteristics are stored in the chip
- Self-test requires only test initialization and response analysis

- Self-test implementation offers a minimum number of extra primary nodes and hardware overheads

The BIST structure comprises of three blocks, test vector generator, Circuit Under Test (CUT), and response analyzer. Response analyzer is the comparison tool between the initial and expected output. The output of the compression circuit inside the response analyzer will produce output called signature. The whole process is called signature analysis.

Instead of trying to implement the design of a large system all at once, a divide and conquer strategy is taken in a top-down design process. Top down design is referred to as recursive partitioning of a system into its subcomponents until all subcomponents become manageable design parts.

For design, the system is broken up into small blocks. The blocks are interconnected to form the system. The function of each block and the interface between them are carefully defined that the system formed by interconnecting the blocks obeys the system specification. Figure 1 illustrates the block representation of BIST model.

Test vector generator: Pseudorandom test generator is used in designing test vector generator due to its versatile and economical arrangement for generating test vectors. Pseudorandom pattern tests (PRPTs) contain the arrangement inear feedback shift register (LFSR) with the feedback connection via exclusive-OR (XOR) gate. It consists of D latches and XOR gates. The 8-bit LFSR shift the bit value at the rising edge of the clock. When the clock value is 1, the shift register shifts the bit value to the next D latch. When the clock value is 0, there is no shift operation and the D latches retain its previous value. In this design, 8-bit test vector generator is considered thus produces 255 different patterns of test vectors to the CUT block. The pattern with all zero is avoided due to the infinite lock of the system. A graphical representation of pseudorandom binary sequence geberator is illustrated in Fig. 2.

Circuit Under test (CUT): Two different circuits are considered under test, a 3 to 8 line decoder and a 4-bit adder. For 3 to 8 line decoder, only 3 bits out of 8 output bits from the test vector generator are used in the CUT block where 5 bits including the carry out are used for 4-bit adder. The remaining bits are left as undefined variable for the both circuits. For each circuit under test, the output is passed to the response analyzer for compress and further analyze.

Response analyzer: A Multiple-Input Pattern Compressor (MIPC) circuit consists of D latches and XOR gates are used to get the signature, which is the compressed form of used to get the signature, which is the compressed form of the response of the multiple input

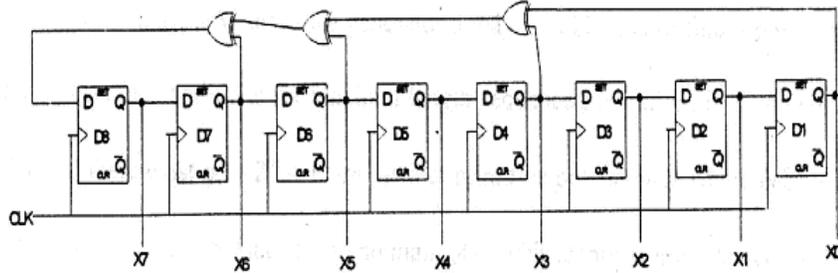


Fig. 2: Logic diagram of pseudorandom binary sequence generator

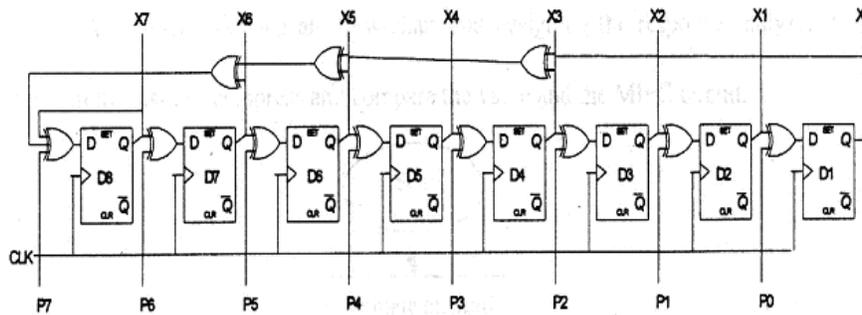


Fig. 3: Logic diagram of MIPIC

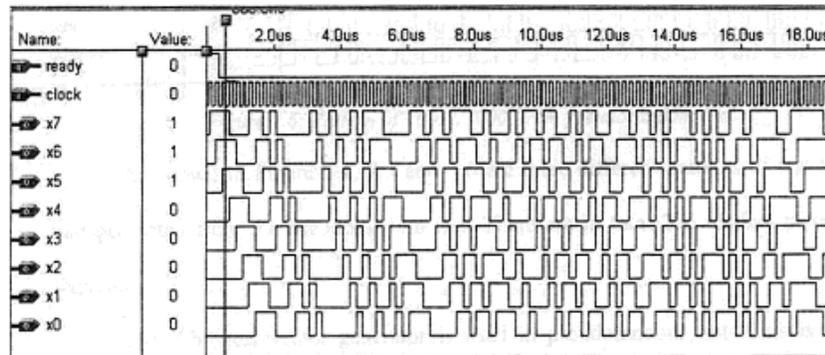


Fig. 4: Pattern of 110 0000 from pseudorandom test

from CUT. The signature is then passed to a comparator circuit to match the expected output with the signature. The MIPIC function as the LFSR. When there exist of rising edge of clock pulse, the D latches shift the value and XOR with the gates level. The logic diagram of 8-stage MIPIC is shown in Fig. 3.

RESULTS AND DISCUSSION

Simulation: The compilation and simulation of the model is run through MAX+PLUS II version 9.23. Simulation of design is done in a bottom-up fashion to verify the correctness. Two snapshots for pattern 110 0000 and 011

1000 out of 255 simulated output waveform from test vector generator are shown in Fig. 4 and Fig. 5 respectively which proves the correctness of the test vector generator.

A simulated waveform for the input 10 is shown in Fig. 6 for a 3 to 8 line decoder which shows its perfection through the output 100 0000. Another snapshot is shown in Fig. 7 for a 4-bit adder.

A simulated waveform for a sequence of compressed output called signature is illustrated in Fig. 8.

The three blocks of BIST are mapped together into one in order to simulate the overall project output. The 4-bit adder is applied as CUT circuit. The output from the

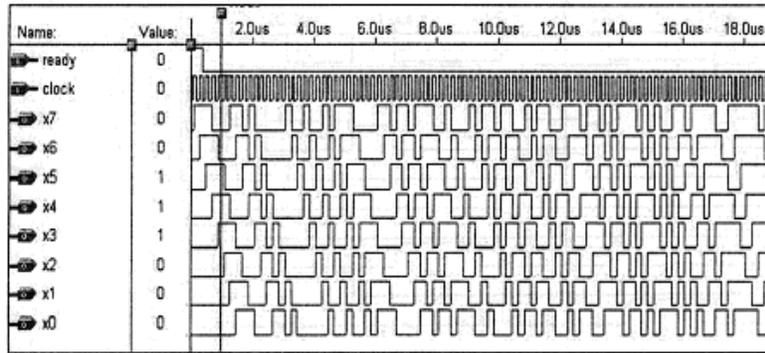


Fig. 5: Pattern of 111 0000 from pseudorandom test

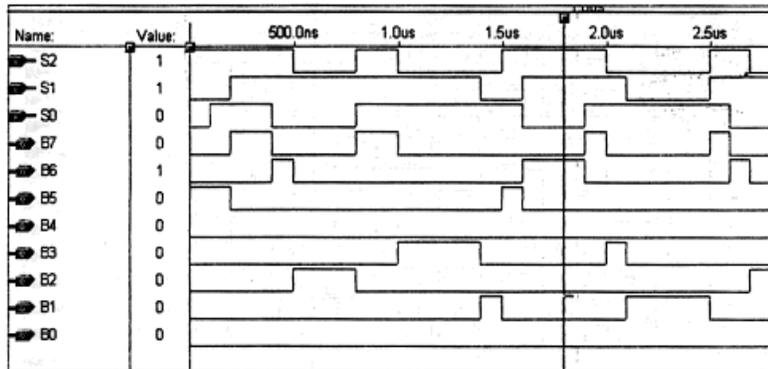


Fig. 6: Simulation waveform of 3 to 8 line decoder

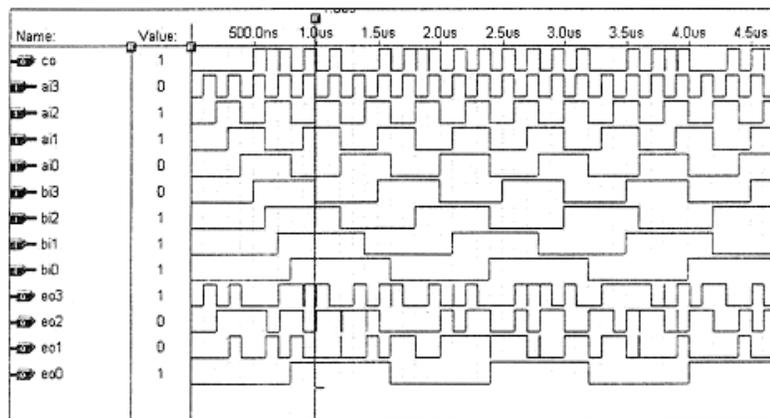


Fig. 7: Simulation waveform of 4-bit adder

CUT circuit passed into the response analyzer, which compressed through the MIPC, this followed by the comparison of compressed output with the expected output that stored in the on-chip memory. Figure 9 illustrates the simulated waveform of BIST using a 4-bit adder as pure CUT and Fig. 10 illustrates the simulated waveform of BIST using a 4-bit adder as faulty CUT.

Synthesis: Concerning the designated hardware realization, The VHDL code is synthesized by considering Altera FLEX10K: EPF10K10LC84-3 FPGA chip on LC84 package. The physical hardware layout is generated using the synthesis tool Synplify version 7.0. The FLEX 10 K families provide the density, speed, and features to integrate entire systems, including multiple 32

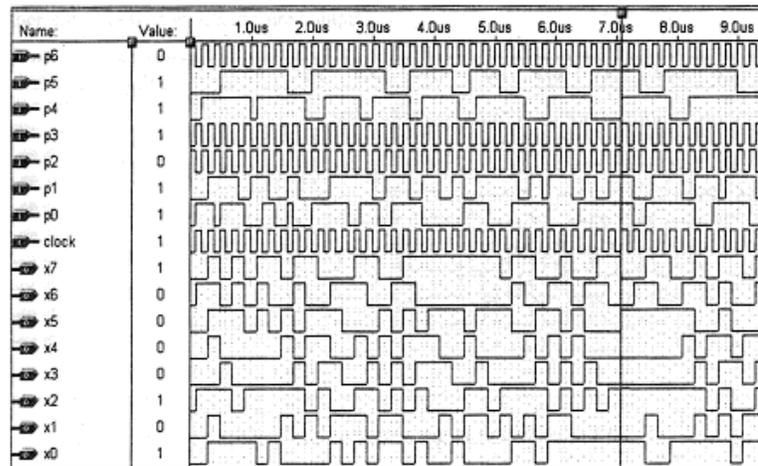


Fig. 8: Simulation waveform of MIPC

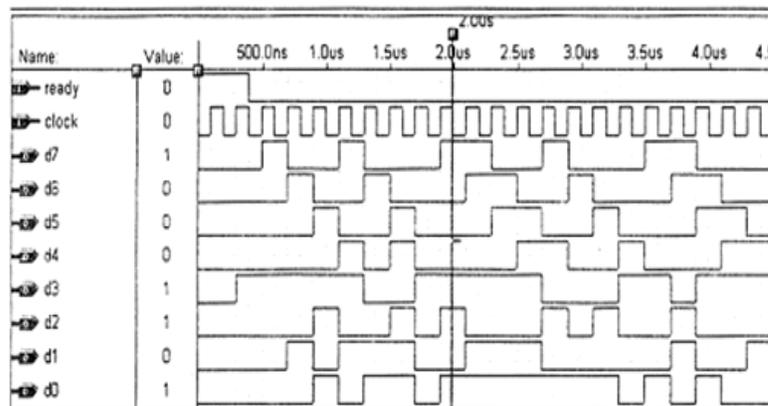


Fig. 9: Simulation waveform of BIST using 4-bit adder as CUT

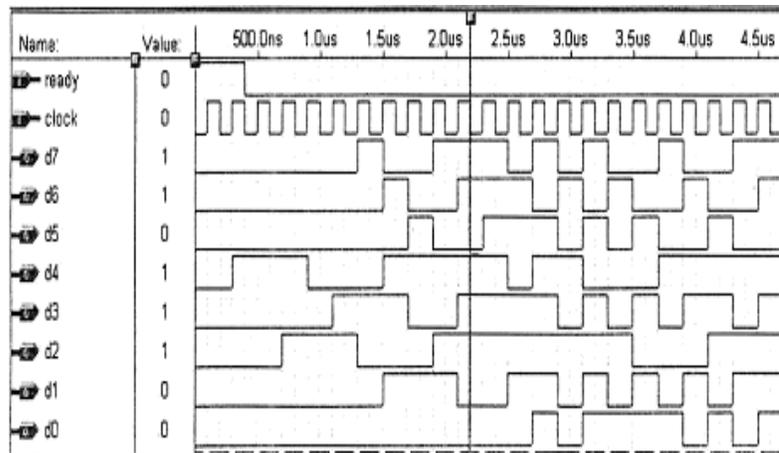


Fig. 10: Simulation waveform of BIST using 4-bit adder as faulty CUT

Table 1: The usage of logic resources in EPF10K10LC84-3

LCs used	366 L Cs out of 576 (63.54%)
Number of nets	444
Number of inputs	1843
I/O cells	66
Cells in logic mode	323
Cells in cascade mode	43

-bit buses into a single chip. A comparatively low critical path frequency was achieved which was 31.4 MHz. The design took a minimum resource i.e., 366 logic cells, which is 63.54% of the device EPF10K10LC84. Table 1 shows a details report of the usage of resources.

CONCLUSION

The objective of this project was to hardware prototyping of a Built-in-self-test for System on Chip Design. By simulating with 3 to 8 line decoder and 4-bit adder circuit as CUT the proposed VHDL model of built-in-self-test for system on chip design was successfully designed and implemented on Altera FLEX10K: EPF10K10LC84 FPGA chip on LC84 package. The modules were successfully compiled, simulated and synthesized, which achieved maximum frequency of 31.4 MHz and a minimum resource usage of 63.5% of the total cells. The hardware implementation demonstrated complete, correct functionality and met all the initial system requirements.

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