

Review of Efficient and Innovative Mathematical Models on VLSI Circuit Partitioning

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Abstract: Classical Problems on any discipline of study has to undergo a series of alternative approaches at different points of time. Many experimental verification of fundamental theoretical results have to be framed in the domain of mathematical modeling based on iterative approaches. One such area of our interest is VLSI Design issue in particular Circuit Partitioning. We present here chronological order of different procedures based on variety of graph theoretical and optimization techniques. These fall into major classification of deterministic and Probabilistic tool kits. A clear cut understanding of these collection will facilitate the researchers engaged in this field for creditable contribution. Hypergraph method is better than the vertical and horizontal procedure in wing and cell partitioning. New type of hypergraph called unimodular hypergraph gives better results for VLSI Cell partitioning.

Key words: Circuit partitioning, graph theoretical algorithms, mathematical model, partitioning

INTRODUCTION

The study is presented in three sections. In section I, we deal with relevance of hyper graph in coprocessor design and its development through circuit partitioning. In section II, the problem of reduction in complexity and minimization of time delay in multilevel sequential partitioning is studied and related study in this direction is listed. In section III, we deal with unimodular graph and stochastic functions placed on them to study circuit partitioning. The objective of this study is to review the conventional methods for VLSI cell partitioning and effectiveness of new type of partitioning based on unimodular hypergraph.

SECTION I: COPROCESSOR DESIGN FOR VLSI PARTITIONING PROBLEMS

The main problem of partitioning in VLSI Design and other related domain of study can be placed as getting sub domain of vertices in a given hyper graph. Earliest researchers like Kernighan-Lin (KL) and Fiduccia-Mattheyses (Alpert and Khang, 1996; Alpert *et al.*, 1997; Bui and Jones, 1993) have given algorithms of iterative refinement on the specific nodes of relative importance. Some have placed the problems in searching for Max-Min cut on graphical representation of the design. In a paper on hyper graph and co processor design, an approach made to give a probability algorithm through Markov

chain in which additional model for a FPGA layout suggested using SAT Problem. The reduction in complexity is tackled through SAT Problem. (Thiyagarajan and Manikandan, 2011).

The hypergraph can be converted into ordinary spanning tree of a regular graph:

- Step 1:** Average of each row is subtracted from every entry d_1
- Step 2:** Average of each every column is subtracted from every entry d_2
- Step 3:** Product is summed and the average is taken.
- Step 4:** We find the cross correlation between this movements

Row variance = 12.36

Column variance = 14.66

Covariance between row and column entities = 9.38

Correlation between row and column = 0.7

This shows that the hypergraph method is better than the vertical and horizontal method procedure in wing and cell partitioning. Markov distribution is shown in Fig. 1.

Boolean SAT based FPGA detailed routing formation (Saveena *et al.*, 2010): In this approach geometric FPGA routing task is transformed into a Boolean satisfiability (SAT) equation with the property that any assignment of input variables that satisfies the equation specifies a valid

1	1	2	3	4	5	6	7
2	0.00	0.12	0.14	0.19	0.14	0.31	0.60
3	31.0	0.00	0.28	0.00	0.20	0.21	0.00
4	0.37	0.17	0.14	0.11	0.50	0.80	0.50
5	0.15	0.13	0.18	0.90	0.00	0.26	0.17
6	0.31	0.00	0.28	0.00	0.20	0.20	0.00
7	0.15	0.12	0.18	0.90	0.00	0.25	0.18

Fig. 1: Markov distribution

rou. The satisfiability equation is then modeled as constraint satisfaction problem, which helps in reducing procedural programming. Satisfying assignment for particular route will result in a valid routing and absence of a satisfying assignment implies that the layout is unroutable.

SECTION II: CIRCUIT PARTITIONING FOR DELAY MINIMIZATION OF VLSI CIRCUITS

Graph partitioning place an important role in Circuit design and testing. The objective is to divide the circuits into blocks such that the components fall within prescribed sizes. The complexity of the connection between these component is reduced. Controlling of cut size for various types of graph have been studied by Hendrickson and Leland (Hendrickson and Leland, 1993) and Karypis and Kumar (Karypis and Kumar, 1995). Multilevel algorithms compare spectral methods and parallel formulation for such sequential circuit partitioning. Delay minimization of VLSI circuits have been studied through global clustering and connectivity information (Yang and Wong, 1995). Prim’s algorithm can complete an optimal solution if node duplication is allowed in circuit design.

Somasundram (Somasundram, 2007) has given multilevel sequential circuit partitioning for delay minimization of VLSI circuit using special type of K-Partitioning algorithm and as achieved bench mark circuits. Any given partitioning problem is to decompose given circuit into K blocks and for given K with balanced area. Circuit delay is a measure as the longest combinatorial for delay from premier input of flip flop output to a premier output or flip of input. Researchers had an objective to perform multilevel partitioning with retiming for minimum delay in reducing cut size as much as possible.

SECTION III: UNIMODULAR HYPERGRAPH IN VLSI CELL PARTITIONING

A new type of hypergraph called unimodular hyper graph was introduced by Thiyagarajan (Thiyagarajan, 2007) to study stochastic function defined on this graph. Special case of Hoffman and Kruskal was used to study the

stochastic function defined on hypergraph. Principles component analysis and vector decomposition have been introduced to study the VLSI partitioning problems (Thiyagarajan and Manikandan, 2010) through unimodular hyper graphs. This gives a better result than the earlier approaches.

Theorem of Hoffman and Kruskal (1956): An $n \times m$ matrix A is totally unimodular if, and only if, for any integer m -vectors b and b' and for any integer n -vector a and a' , each face of the polytope

$$\{x/x \in R^n; a \leq x \leq a'; b \leq Ax \leq b'\}$$

Contains an integer point.

It follows that each vertex of this polyhedron has integer coordinates.

Theorem of Ghouila-Houri (1962): An $n \times m$ matrix $A = (a_{ij})$ is totally unimodular if, and only if, each set $J \subseteq \{1, 2, \dots, n\}$ can be directed in to two disjoint sets J_1 and J_2 such that:

$$\left| \sum_{j \in J_1} a_{ij} - \sum_{j \in J_2} a_{ij} \right| \leq 1 (i \leq m)$$

Lemma (Thiyagarajan, 2007): If $H = (X, \epsilon)$ is a hypergraph that has a stochastic function, then the support of this function contains a strongly stable traversal of H .

Theorem (Thiyagarajan, 2007): If H is unimodular hypergraph that has a stochastic function, then each stochastic function $f(x)$ associated with H can be expressed in the following form:

$$F(x) = \sum p_i \phi_i(x)$$

$$0 \leq p_i \leq 1; \sum p_i = 1$$

where ϕ_i is a $(0, 1)$ stochastic function.

If $f_k(x)$ is not identically zero, then $1 - \sum p_j > 0$, and the function is stochastic.

$$\frac{1}{1 - \epsilon} f_k(x)$$

Therefore, from the lemma, its support contains a set T_{k+1} that is strongly stable and is a traversal. With the characteristic function $\phi_{k+1}(x)$ the procedure can be continued as above, etc.

The procedure terminates only when the function $f_k(x)$ is identically zero, which implies that:

$$1 - \sum_{j=1}^k p_j \sum_{x \in E_i} f^k(x) = 0$$

Then, function f is equal $\sum_{i=1}^k p_i \phi_i$ where, $\sum p_i = 1$

A set of the form $S = \cup_{i=1}^k T_i$ is the support of a stochastic function:

$$f(x) = \sum_{i=1}^k \frac{1}{k} \phi_i(x)$$

where $\phi_i(x)$ is the characteristic function of set T_i .

FUTURE DIRECTION

Earlier KL regarded as Problem Max-Min cut in the algorithmic approach of constrained weighted graph algorithm. Later, the weighted graph theory has been placed in theory of permanence and allied NP-Complete problems to make the NP-Complete Problem solvable in polynomial time. Somasundram and others have regarded a simple VLSI Design problem as a graph theoretical problem. These alternative approaches could not address on uncertainty hidden in the hypergraph approach of VLSI Circuit partitioning. A stochastic hypergraph helped us to force the problem in a probabilistic environment. In future, the circuit partitioning may lead strong conjecture in major VLSI Design issue.

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