

## Application of Implicit Space Mapping in Aid of Design of Sub-harmonic Mixer with CMRC Filter

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**Abstract:** In recent years, the CMRC filter has been an attractive candidate for use in mixer and frequency multiplier circuits to improve the performance due to its low-insertion loss, sharp rejection, shorter size and wider stop-band. However, complex structures, too much variables and inefficient design method hindered its widespread use. In this study, we report on the application of the implicit space mapping algorithm in design of CMRC filter to greatly improve the design efficiency. Finally, a mixer with CMRC filter is designed and fabricated based on Rogers substrate process. The measured performance of this mixer is sufficient for engineering applications.

**Keywords:** Compact microstrip resonant cells, implicit space mapping algorithm, planar anti parallel GaAs schottky diodes, sub-harmonic mixer

### INTRODUCTION

The Compact Microstrip Resonant Cell (CMRC) filter is proposed by Xue *et al.* (2000). CMRC filter has been applied in harmonic mixer to reduce the conversion loss (Tsz *et al.*, 2003; Xue *et al.*, 2003). In recent years, our team successfully used the CMRC filter in sub-harmonic mixer in millimeter-wave band and the mixer's performance was improved (Zhang *et al.*, 2011; Yang *et al.*, 2010, 2011). Compared with the traditional low-and-high-impedance microstrip filter, the CMRC filter is characterized by low-insertion loss, sharp rejection, shorter size and wider stop-band. These superior characteristics can be used to improve the performance of the mixers and multiplier in microwave and millimeter-wave band. However, complex structures, too much variables and inefficient design method hindered its widespread use.

Implicit Space Mapping (ISM) technology (Bandler *et al.*, 2004) addresses the issue of reducing the time-consuming full-wave Electromagnetic (EM) simulations of microwave structures with the help of a fast physics-based model or surrogate for device modeling and optimization. In this study, we adopt the simplified space mapping implementation in Agilent ADS, all the space mapping steps are integrated into one ADS schematic. The whole processing of design for microstrip CMRC filter was described. Finally, a sub-harmonically pumped mixers, which operate in the 91-98 GHz band for millimeter-wave communication using the designed CMRC filter, is designed and fabricated based on rogers substrate process.

So far, many sub-harmonic mixers have been reported, such as the mixer of Sanjay with a conversion loss of 7~10 dB operating at RF frequencies of 92-96 GHz (Raman *et al.*, 1997) and Yuh-Jing Hwang's sub-harmonic mixer with a conversion loss of 10~14 dB over the band 78-114 GHz (Hwang *et al.*, 2002). The mixer with CMRC filter designed in this study exhibits the conversion loss of 8~11 dB over the band 91-98 GHz. Compared to the mixers with narrowband property (Raman *et al.*, 1997) or high conversion loss (Hwang *et al.*, 2002), the sub-harmonic mixer is designed as a fix-tuned component with the least number of parts to minimize the cost and maximize its potential for volume manufacture.

### APPLICATION OF IMPLICIT SPACE MAPPING IN DESIGN OF CMRC FILTERS

**ADS schematic design framework:** We implement implicit space mapping optimization in the ADS schematic framework in an interactive way to greatly raise efficiency of CMRC filter design. The space mapping is implemented in 5 steps is as follows:

- Step 1:** Set up and optimize the coarse model in ADS schematic.
- Step 2:** Create the parameterized fine model in HFSS; the structure dimension is same as the value obtained in Step 1.
- Step 3:** Simulate the fine model and import the S parameter into ADS. Check the stopping criteria which are that the difference between responses of the fine model and coarse model

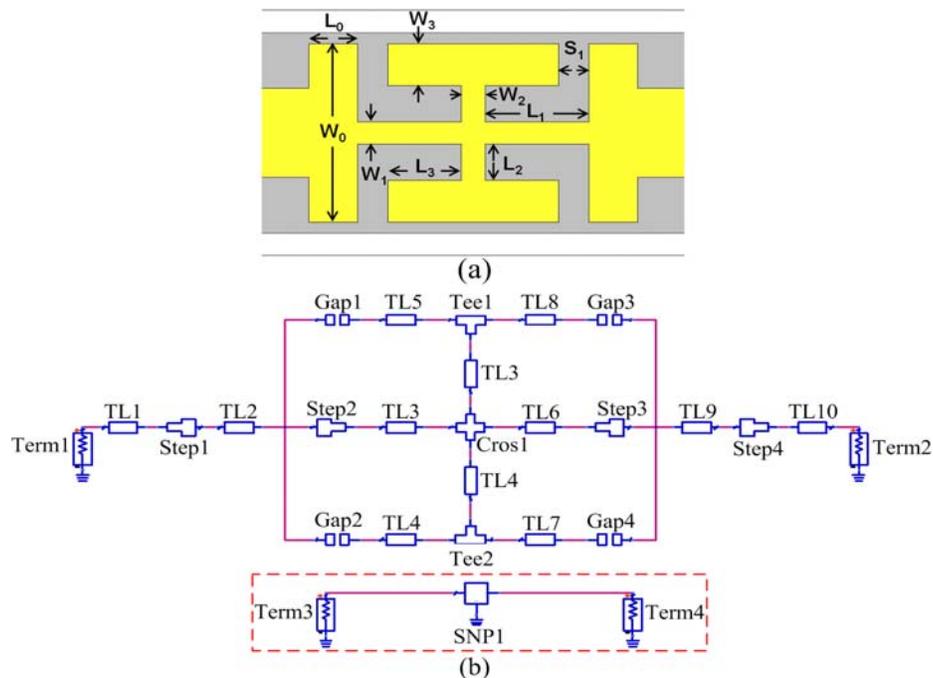


Fig. 1: (a) The structure of microstrip CMRC filter, (b) the parameter extraction in ADS

is very small; if satisfied, stop. Otherwise, optimize ADS coarse model to match fine model to perform parameter extraction.

**Step 4:** Re-optimize the calibrated coarse model design parameters to predict the next fine model design.

**Step 5:** Update the fine model design and go to Step 3.

**Design of CMRC filter:** Microstrip CMRC filter is designed based on a rogers5880 substrate, as shown in Fig. 1a. Design parameters are  $x = (L_0, L_1, L_2, L_3, W_0, W_1, W_2, W_3, S_1)^T$  mm. Thickness of the substrate is  $H = 0.254$  mm, dielectric constant is  $\epsilon_r = 2.2$ , loss tangent is 0.0009 and the metallization is copper. The design specifications are  $|S_{11}| < 25$  dB for DC  $\leq$  w  $\leq$  50 GHz and  $|S_{21}| \leq -25$  dB for 80 GHz  $\leq$  w  $\leq$  120 GHz.

Because the CMRC filter work at millimeter wave frequency, we use the scale model with scale factor of 10 to improve the accuracy of the coarse model in ADS. In this design, the fine model is simulated in a soft HFSS, the coarse model, which is above the dash box in Fig. 1b, is constructed and optimized in Agilent ADS. The dielectric constant and the height of the substrate of the components in Fig. 1b are defined as follows:

- Tee1, Tee2 and Cros1 correspond to  $\epsilon_1$  and  $H_1$
- Gap1, Gap2, Gap3 and Gap4 correspond to  $\epsilon_2$  and  $H_2$
- Step1, Step2, Step3 and Step4 correspond to  $\epsilon_3$  and  $H_3$
- Ideal transmission line TL correspond to  $\epsilon_4$  and  $H_4$

The initial values of  $\epsilon_1, \epsilon_2, \epsilon_3, \epsilon_4$  are set as 2.2, which is the dielectric constant of rogers5880 substrate and the initial values of  $H_1, H_2, H_3, H_4$  are set as 2.54 mm, which is 10 times of the thickness of rogers5880. Then the optimization of the scale model is carried out according to the specifications for pass band over 0~5 GHz and stop band over 8~12 GHz.

The initial guess is  $x^{(0)} = [1.88, 3.83, 1.52, 2.83, 8, 1.07, 1.03, 1.95, 1]^T$  mm, the response of our initial tuning model and fine model is shown in Fig. 2a. One of the most important steps, parameter extraction, is implemented entirely in ADS (Fig. 1b).

We compensate the deviation between the tuning model and the fine model by calibrating the dielectric constant  $\epsilon_1, \epsilon_2, \epsilon_3$  and the height  $H_1, H_2, H_3$  of the substrate as tuning parameters, with  $\epsilon_4$  and  $H_4$  kept as two constants that are the same as their initial values. We can see that the specification is not satisfied after the first iteration, but the parameter extraction using ISM yields a good match between the coarse and fine models (Fig. 2b). The coarse model is then optimized in ADS with respect to the design specifications. The new design parameters are then assigned to the fine model. Finally, the optimal values obtained are  $x^* = [4, 4, 2.5, 3, 8, 1, 3, 1, 1]^T$  mm after three iterations. The optimized tuning model and the corresponding fine model responses are shown in Fig. 2c. After structure Dimensions of the scale model are divided by the scale factor of 10, we can get the final CMRC filter satisfying the design specifications (Fig. 2d).

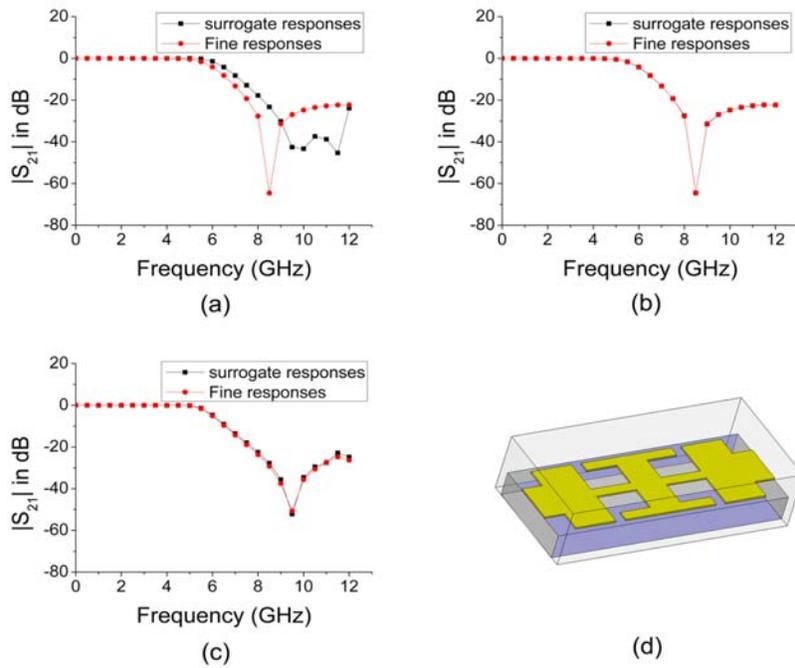


Fig. 2: (a) The response of our initial tuning model and fine model, (b) the response of our tuning model and fine model after the first iteration, (c) the optimized tuning model and the corresponding fine model responses, (d) the structure of final CMRC filter

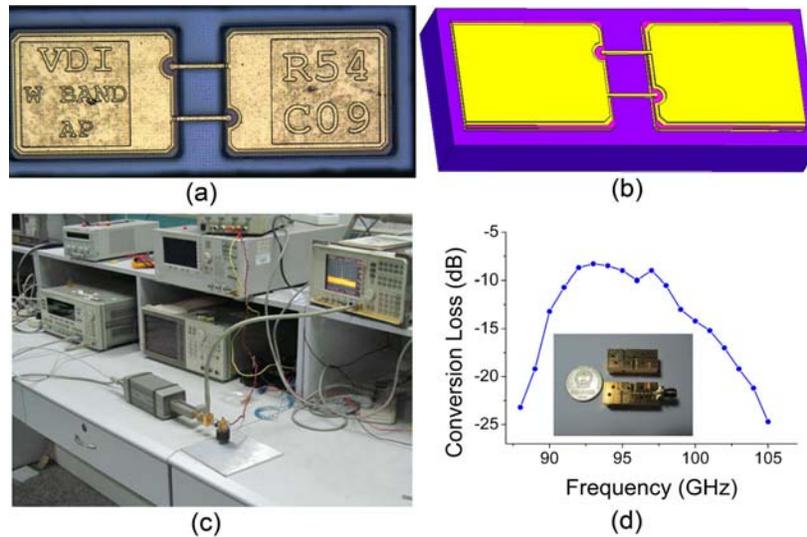


Fig. 3: (a) SEM microscopy of W-band anti parallel diodes purchased from Virginia diodes, (b) the electromagnetic model of the anti parallel schottky diodes, (c) photograph of measurement branch, (d) measurement results of mixer and the inset figure is photograph of the mixer

### DEVICE MODELING

**Schottky diode nonlinear modeling:** The junction parameters of the anti parallel Schottky barrier diode fabricated by VDI chosen here include an anode diameter of 3.8  $\mu\text{m}$ , a pad to pad capacitance  $C_{pp\_self}$  of 15 fF, a finger to pad  $C_{fp}$  capacitance of about 1 fF, zero biased junction capacitance for single anode  $C_{j0}$  of 22

fF, an ideality factor  $\eta$  of 1.176, a series resistance  $R_s$  of 4  $\Omega$ , a saturation current  $I_{sat}$  of 71.9 fA and a built-in potential of 0.75 V. The schottky diode model in ADS library is used to create the diode nonlinear analysis model.

**Electromagnetic model of anti parallel schottky diodes:** The diode considered is a anti parallel GaAs

Schottky diode version of Virginia Diode. Figure 3a show a SEM microscopy of the whole device. The diode structure was modeled using a soft HFSS FEM simulator. A SEM microscopy was used to obtain physical dimensions of the diode structure. The effect of the planar diode chip structure on the diode's embedding impedance could be modeled by using HFSS to solve for the fields within the diode chip when mounted in the microstrip channel. Small coaxial ports were attached to probes on each anode so that the individual embedding impedances for each diode could be monitored directly (Fig. 3b) (Alderman *et al.*, 2007; Porterfield, 2007; Maestrini and Ward, 2008).

### MIXER FABRICATION AND MEASUREMENT

After the design of CMRC filter is finished and the diode junction model has been determined, optimal parameters of the mixer are obtained with assistant of ADS and HFSS. The circuit is fabricated on rogers5880 substrate of 0.254 mm thickness and the photograph of the measurement branch for SHP mixers is shown in Fig. 3c. The mixer is pumped with a widely tunable LO source, the calibration of the RF and LO power was performed using Erickson's PM-4 power-meter and the IF signal has been measured with the Agilent spectrum analyzer 8563EC. According to experiment report, our test errors include power meter about 5% and the spectrum analyzer about 0.5 dB. The test results in Fig. 3d are average values of three sets of test data to reduce the test error. It can be found that the conversion loss was obtained in the range of 8-11 dB from 91 to 98 GHz when the LO frequency was fixed at 47 GHz with 6 mW of power.

### CONCLUSION

The design of a 94 GHz fixed-tuned subharmonically pumped mixer using commercially available GaAs flip-chip Schottky barrier diodes has been demonstrated in this study. The accuracy of design is improved by building three dimensional electromagnetic model of anti parallel GaAs Schottky diode to consider the influence of parasitic parameter. Design efficiency is greatly improved by use of ISM algorithm. The measured performance of this mixer, with 6 mW of LO power and with conversion losses 8~11 dB obtained over a frequency range from 91 to 98 GHz, is sufficient and robust for the foreseen applications.

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