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Design of an Inductor-Less LNA Using Resistive Feedback Topology for UWB Applications

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Abstract: Low Noise Amplifier (LNA) is one of the essential components in Ultra Wideband (UWB) devices. Conventional LNA suffers from large chip area, high power consumption and inadequate Noise Figure (NF). A compact UWB LNA in the bandwidth of 3.1 to 10.6 GHz is proposed. The design is based on inductor-less configuration using the resistive shunt feedback topology and noise canceling techniques for wideband and high gain characteristics. Designed in 0.18-µm CMOS technology without applying any inductors and capacitors in the core circuit, the chip area is only 0.001 mm^2 and consumes 16.11 mW of power at 1.5-V supply. The maximum gain is 18.01 dB and the minimum NF noise is 1.324 dB.

Keywords: CMOS, inductor, LNA, noise-canceling, resistive feedback, UWB

INTRODUCTION

UWB system is a wireless technology which is capable of data transmission over a wide spectrum of frequency bands from 3.1-10.6 GHz with very low power and high data rates (Akter *et al*., 2008a, b; Reaz *et al*., 2007a, b; Marufuzzaman *et al*., 2010; Reaz *et al*., 2003; Reaz *et al*., 2005; Chang *et al*., 2008; Chang and Hsu, 2010; Chen and Liu, 2012). LNA is one of the essential components in developing UWB devices (Reaz *et al*., 2006; Reaz and Wei, 2004; Mohd-Yasin *et al*., 2004; Mogaki *et al*., 2007; Lu *et al*., 2006; Moezzi and Bakthiar, 2012; Belmas *et al*., 2012). Due to Federal Communication Committee's (FCC) limitation on bandwidth (not lesser than 500 MHz) and low power emission (EIRP lower than 41.3 dBM/MHz) for an UWB applications, several stringent requirement in designing an UWB LNA needs to be fulfilled.

The UWB LNA needs to provide a good input matching over the bandwidth of 500 MHz and sufficient gain to amplify the weak signal at the receiver as well as to overcome the noise effects from subsequent stages. On top of that, the NF of the UWB LNA must be minimized as low as possible since it plays a main role in defining the receiver's sensitivity. Moreover, the size of LNA needs to be physically small in order to provide power efficient and reduce the fabrication cost respectively.

Significant research and various approaches have been proposed to design UWB LNA. There are several techniques that commonly used to achieve wideband input matching for UWB LNA such as the inductive peaking, the Distributed Amplifier (DA), the filter type amplifiers, the common gate amplifier and the resistive shunt feedback amplifier (Chen *et al*., 2011). However, these techniques may suffer from several disadvantages which include large chip area, high power consumption and inadequate NF (Nilsaz *et al*., 2010; Hsu *et al*., 2010).

This study presents the design of an UWB LNA that aims to achieve low power, small size and medium gain (Power gain >10 dB). The gain enhanced resistive shunt feedback based on noise canceling techniques is used in designing inductor less UWB LNA as it is able to accomplish wideband input matching, relative low NF, sufficient voltage gain and high linearity. Furthermore, this technique is widely used to release the tradeoff in the UWB LNA.

CONVENTIONAL ARCHITECTURE

Resistive feedback topology: Basically, feedback is a common technique that is applied in the design of wideband amplifiers to obtain the input matching. In the resistive feedback, LNA can achieve very wideband (from 0-22 GHz) and also it has low power consumption and high gain. This technique takes into the consideration since negative feedback had a tendency to minimize the input impedance of amplifier as well as extend its bandwidth with reduction of trade-off gain. As compared to the other techniques, a smaller chip area can be achieved by resistive feedback LNAs configuration since there are no or less inductors being introduced and utilized. To enhance the performance of

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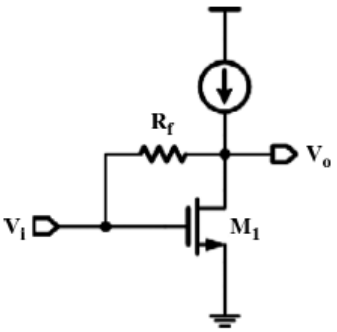

Fig. 1: CS amplifier with resistive feedback (Chang and Hsu, 2010)

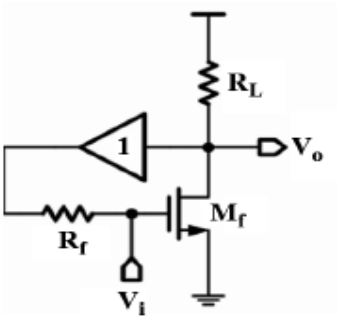

Fig. 2: Resistive feedback amplifier with an ideal voltage buffer (Chang and Hsu, 2010)

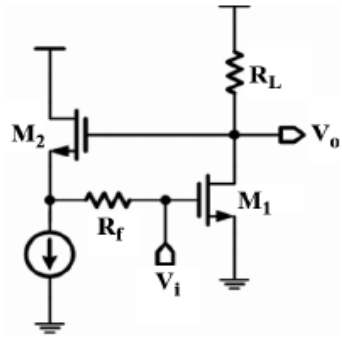

Fig. 3: Source follower buffer in the resistive feedback amplifier configuration (Chang and Hsu, 2010)

LNAs in terms of bandwidth extension and input matching, numerous techniques were proposed and developed based on the resistive feedback approach. The basic schematic of the common source amplifier with a resistive feedback is shown in the Fig. 1 (Chang and Hsu, 2010).

However, this Common Source (CS) amplifier is incapable to achieve a good input matching and low NF. In regards to this limitation, the voltage buffer has been introduced and used with feedback resistor in order to improve input matching and NF. This modified design schematic is shown in Fig. 2.

In this topology, theoretically the increasing of the transistor transconductance g_m is resulting to the reduction of the NF. By appropriate designing of a feedback resistor R_f and load resistor R_L respectively, the input matching can be enhanced. Voltage buffer implementation via a source follower is widely used as indicated in Fig. 3 (Chang and Hsu, 2010).

Noise cancelling technique: The noise cancelling concept is to generate the noises with the opposite phase polarities in different path and cancel the noises at the output. Since, the cancelation is not relevant to the input impedance, this technique allows for simultaneously noise cancellation and impedance matching. Figure 4 shows a simplified resistive shunt feedback LNA by using noise canceling technique. This LNA composed of a transistor M_1, a resistor R_F and feed forward voltage amplifier with a gain of A_X (A_X>0). To have maximum power transfer, the input impedance Z_{in} is designed to match to source impedance, Rs.

METHODOLOGY

The proposed UWB LNA consists of a noise cancelling and an output buffer stages using resistive feedback topology as shown in Fig. 5. R_S is 50Ω source impedance which connects the input pad via a capacitor C_{in}. In the noise cancelling stage, R_{F1} is a shunt feedback resistor which purposely used for

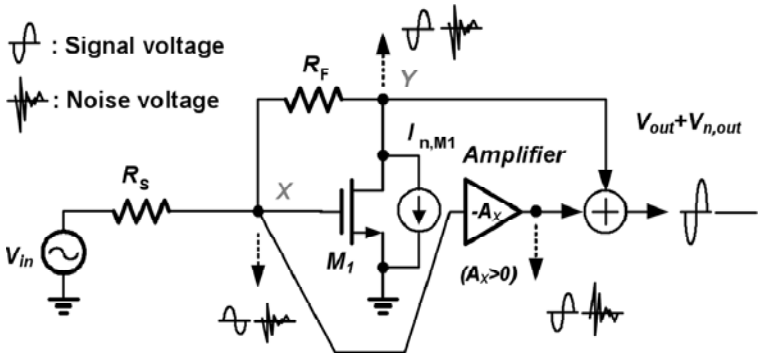

Fig. 4: Simplified resistive shunt feedback using noise cancellation technique

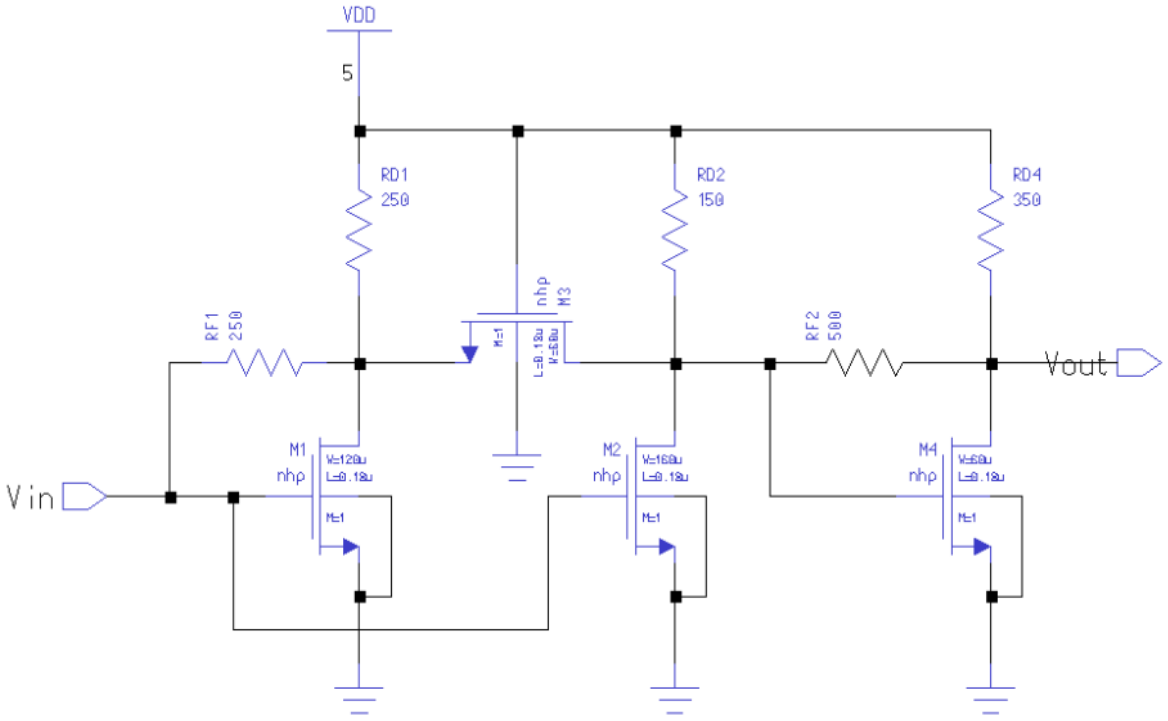

Fig. 5: Proposes resistive shunt feedback noise cancelling UWB LNA

wideband matching as well as for sensing the signal and noise of the input transistors M_1, M_2 and M_3 respectively to combine the signal and subtract the noise of M_1. R_{D1} and R_{D2} are being used as the load resistors. To subtract the noise at the drain of M_2, the polarities of the signal at the drains of M_1 and M_2 will be in-phase. If A_2 is implemented in a common source configuration, the signals at the drains of M_1 and M_2 will be out of phase. Therefore, a subsequent stage is needed to convert the polarities. In this way, the linearity will be decreased and power consumption increases. Hence, the common gate configuration has been adopted in this UWB LNA design rather than a common source.

The input impedance Z_{in} is equal to the parallel combination of the input parasitic capacitance C_A and resistance R_{in}. C_A is the gate to source capacitance of M_1, M_2 and R_{in} is $[RF1 + (1/gm_3)] / [1 + (gm_1/gm_3)]$ at low frequency, the input matching is achieved by setting R_{in} to 50Ω. As the frequency increases, Z_{in} will deviate from 50Ω because the admittance of C_A increases as well. Therefore, to keep C_A as small as possible is important for wideband input matching. By adding M_3, the part of the current of M_3 flows into M_1 which increases gm_1. As a result, for a given gm_1, the required size of M_1 is small which reduces C_A and maintains a wideband input matching.

In order to achieve wideband output matching, the source follower is commonly incorporated in UWB amplifier. However, for low voltage applications, source follower suffers from poor driving ability and consumes large voltage headroom. A resistive shunt feedback output stage is used in this UWB LNA design which is composed of M_4, R_{F2} and R_{D4}. The voltage gain A_{buffer} and output resistance R_{out} is calculated as (1) and (2):

Table 1: UWB LNA design parameters

Parameters	Values	Parameters	Values
R_{F1}	250Ω	W_1	120 µm
R_{F2}	500Ω	W_2	160 µm
R_{D1}	250Ω	W_3	60 µm
R_{D2}	150Ω	W_4	60 µm
R_{D4}	350Ω	L_1, L_2, L_3 & L_4	0.18 µm

$$A_{Buffer} = \frac{Vo}{V_{D2}} = \frac{R_{D4}(1-g_{m4}R_{F2})}{(R_{F2}+R_{D4})}) \quad (1)$$

$$R_{out} = \frac{R_{D4}}{1+g_{m4}R_{D4}} \quad (2)$$

R_{out} is designed to be 50Ω. It not only provides 50Ω wideband output matching, but also increases the overall gain. The design parameters are summarized in a Table 1.

RESULTS AND DISCUSSION

The circuit simulations of the proposed CMOS UWB LNA design are performed in Mentor Graphics environment based on CEDEC 0.18 um CMOS process

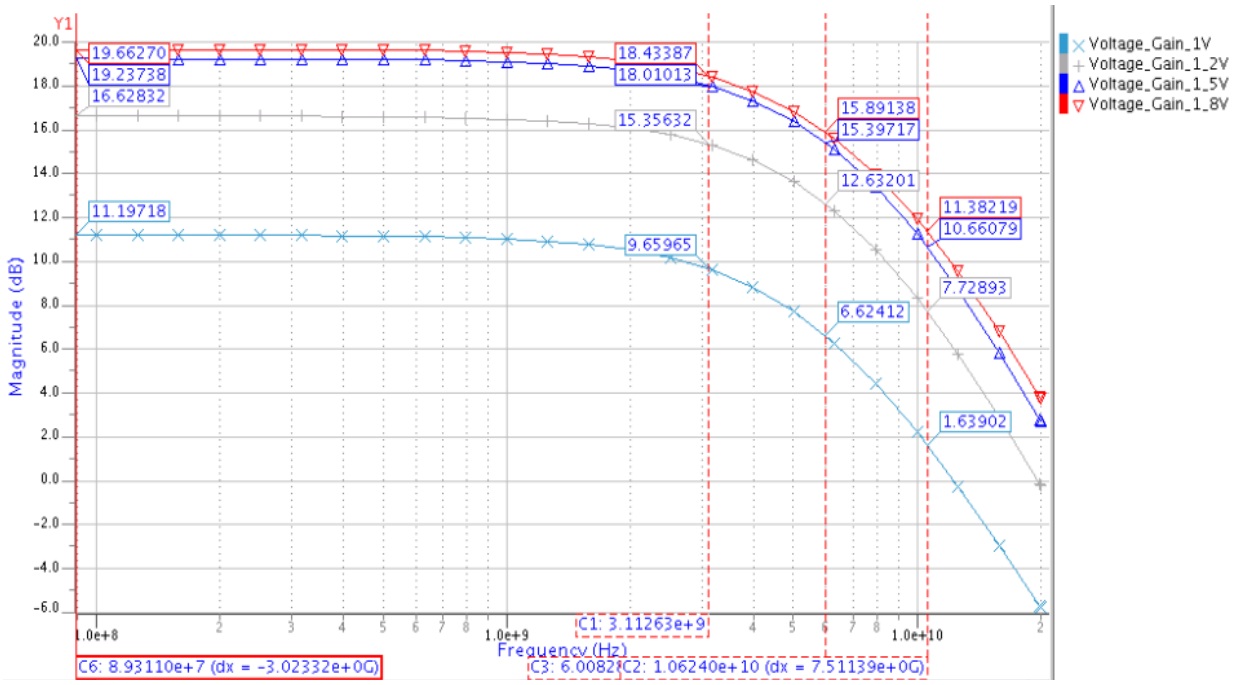

Fig. 6: Simulation results of voltage gain versus frequency with difference supply voltage

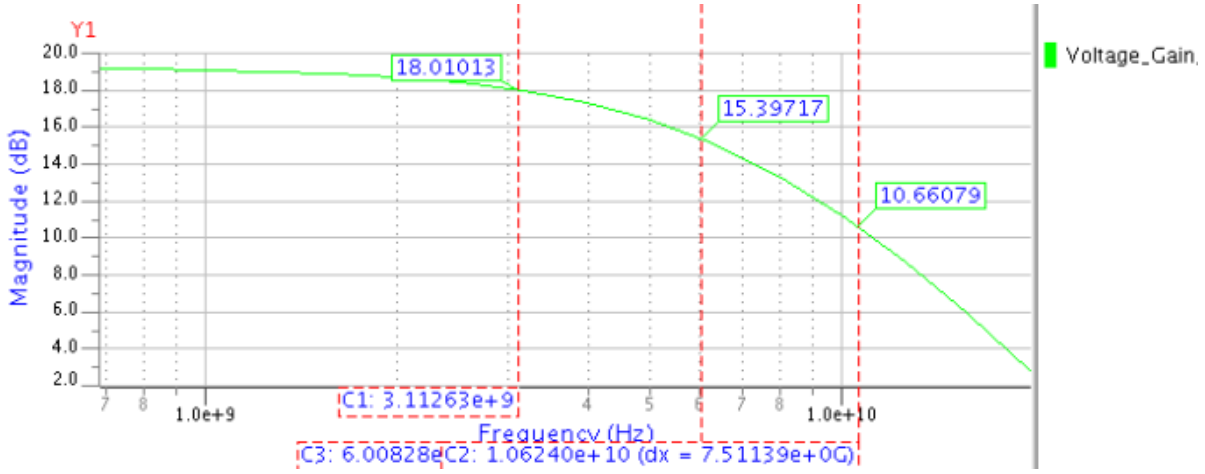

Fig. 7: Simulation result of voltage gain versus frequency for 1.5 V supply voltage

technology. For the simulation, four different supply voltages have been used to examine the voltage gain of the proposed UWB LNA. Figure 6 shows that the voltage gain increases with the increment of supply voltage but utilization of high supply voltage will increase the power consumption of the device. Table 2 represents the relationship of the supply voltage and power consumption that has been simulated.

Therefore, in this UWB LNA design, a supply voltage 1.5 V has been selected since it is able to produce high voltage gain over 10-dB when operated in 3.1 to 10.6 GHz frequency. As shown in Fig. 7, with 1.5V supply voltage, the proposed UWB LNA provides maximum 18.01 dB of gain (S21) over frequency band of 3.1 to 10.6 GHz with a power consumption of 16.11 mW. The input and output noise for UWB LNA is shown in the Fig. 8. Hence, NF that has been obtained for frequency band of 3.1 GHz is 1.73 dB whilst 1.324 dB at 10.6 GHz. The voltage gain is gradually degraded when operating in the high frequency bandwidth

Table 2: Gain (dB) and power consumption (mW) when applying difference supply voltage

Supply Voltage (V)	Voltage gain (dB) 3.1 GHz	6.0 GHz	10.6 GHz	Power consumption (mW)
1V	9.66	6.62	1.64	5.76
1.2V	15.36	12.63	7.73	9.14
1.5V	18.01	15.40	10.66	16.11
1.8V	18.43	15.89	11.38	25.45

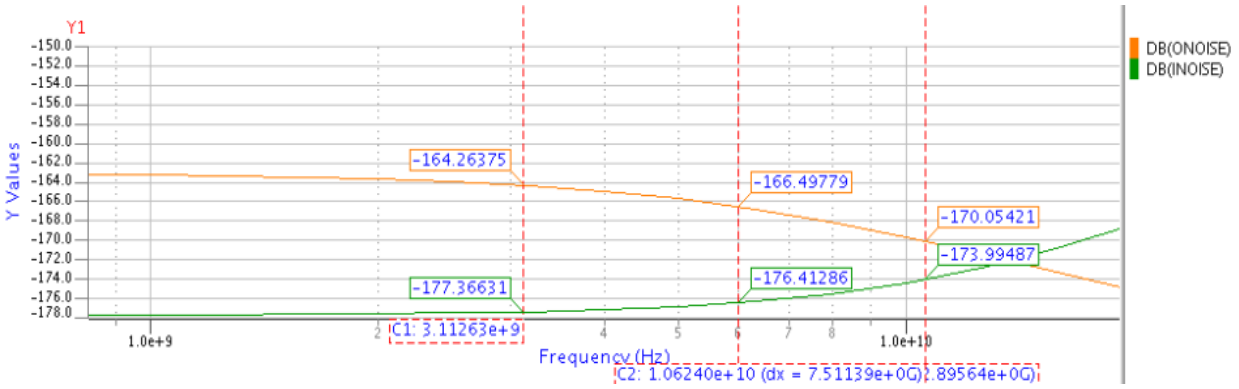

Fig. 8: The input and output noise of UWB LNA

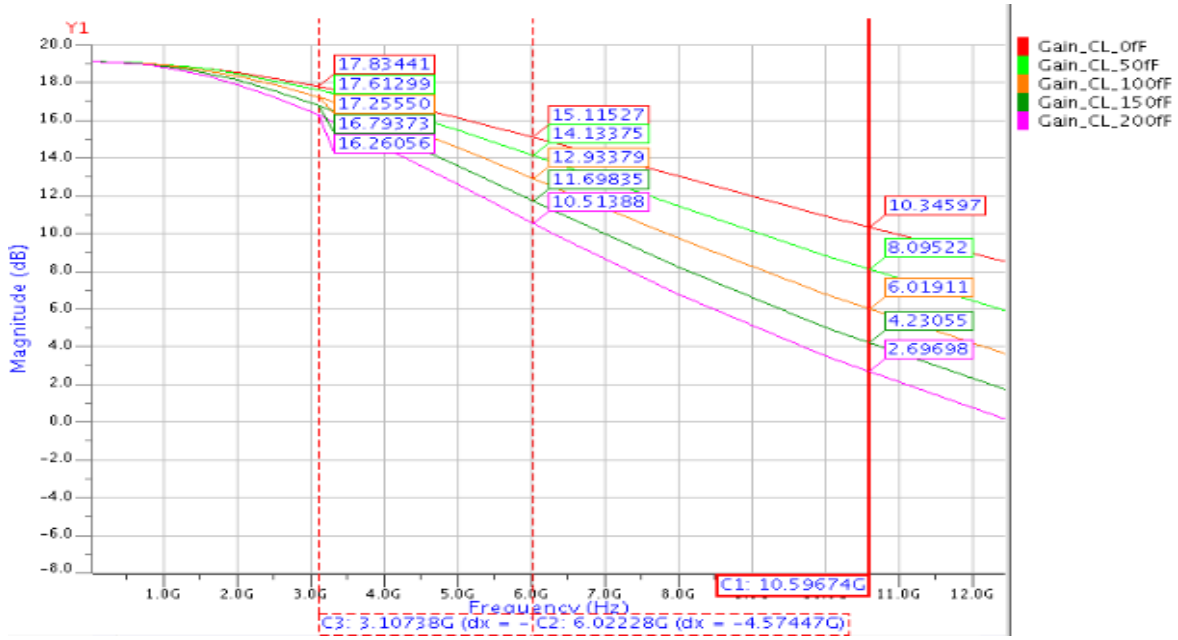

Fig. 9: Voltage gain (dB) for UWB LNA using variety load capacitor

Table 3: Comparison of performance summary on the previous literatures

	CMOS (μm)	Freq (GHz)	S_{21} (dB)	NF (dB)	ESD	Power (mW)	Vdd (V)	Active area (mm^2)
This work	0.180	3.1-10.6	10.7-18	1.73	No	16.11	1.5	0.001
Chang and Hsu (2010)	0.130	3.1-10.6	11.1-12.4	2.70-3.70	No	14.40	1.8	0.031
Chang *et al*. (2008)	0.090	0.2-9	10	4.20 min	Yes	20	1.2	0.066
	0.090	0.2-3.2	15.5	1.76 min	Yes	25	1.2	0.134
Chen and Liu (2012)	0.065	10	10.5	2.70-3.30	No	13.70	1	0.020
Chen and Liu (2012)	0.065	5.2	10.7	2.90-5.40	No	7	1	0.030
Lu *et al*. (2006)	0.180	3.1-10.6	15.9-17.5	3.10-5.70	No	33.20	1.8	0.500
Moezzi and Bakhtiar (2012)	0.180	0.32-1.0	18-23.5	2.20-2.70	No	15.30	1.8	0.100
Belmas *et al*. (2012)	0.130	0.1-2.7	20	4.00	No	1.32	1.2	0.007
Chen *et al*. (2011)	0.180	35	20.5	6.80-8	No	250	2.8	0.780
Nilsaz *et al*. (2010)	0.180	0.4-5.7	18.94	3.15-3.86	No	5.77	1.8	NA
Hsu *et al*. (2010)	0.180	5.2-11.2	13.9	4.90-6.70	No	8	2	0.300

which is mainly due to the parasitic capacitance of the input pad.

Load capacitor has been introduced to the circuit at the output stage which purposely to perform correlation analysis and effects to the voltage gain. As shown Fig. 9, degradation of the gain was observed with increment of load capacitor. Selected value of load capacitor is 50, 100, 150 and 200 fF, respectively.

Based on this study, resistive shunt feedback incorporated in noise cancelling technique is able to

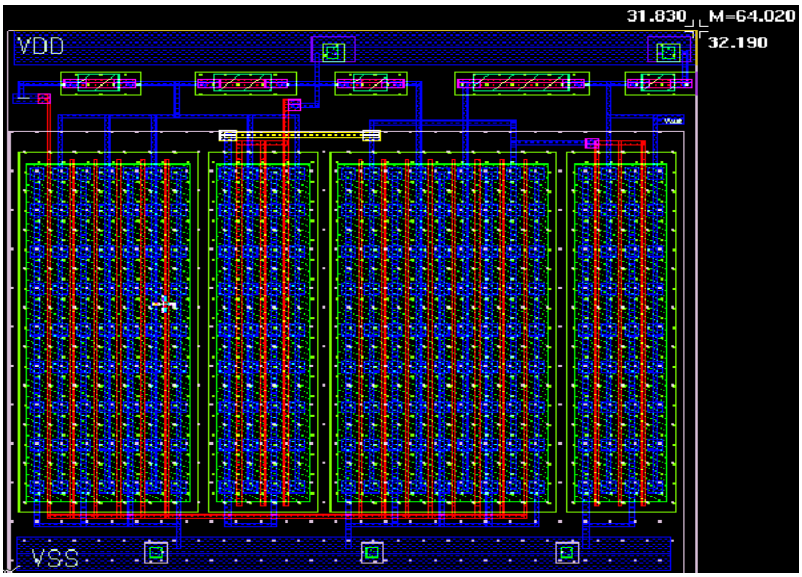

Fig. 10: Layout of the proposed UWB LNA layout

achieve a better performance in term of voltage gain, noise Fig., low power consumption and extend the bandwidth as well as small chip area. Unfortunately, the performance was degraded when the LNA was operated in the high frequency band; this is due to the effect of parasitic capacitances. Table 3 shows comparative performance summary of the proposed design with the other reported UWB LNAs. The layout of the proposed UWB LNA drawn in Mentor Graphics 0.18 um CMOS process technology is shown in Fig. 10 environment based on CEDEC. The core area is only 0.032 × 0.032 mm^2 (0.0010 mm^2).

CONCLUSION

Inductor-less UWB LNA in 0.18-um CMOS technology with core area of only 0.001 mm^2 is proposed in this study. Based on inductor-less design configurations, the resistive shunt feedback and noise canceling techniques were employed. The amplifier was operated at frequency band 3.1 to 10.6 GHz with maximum gain of 18.01 dB and minimum NF of 1.324 dB.

REFERENCES

Akter, M., M.B.I. Reaz, F. Mohd-Yasin and F. Choong, 2008a. A modified-set partitioning in hierarchical trees algorithm for real-time image compression. J. Commun. Technol. El., 53(6): 642-650.

Akter, M., M.B.I. Reaz, F. Mohd-Yasin and F. Choong, 2008b. Hardware implementations of an image compressor for mobile communications. J. Commun. Technol. El., 53(8): 899-910.

Belmas, F., F. Hameau and J.M. Fournier, 2012. A low power inductorless LNA with double gm enhancement in 130 nm CMOS. IEEE J. Solid-St. Circ., 47(5): 1094-1103.

Chang, P.Y. and S.S.H. Hsu, 2010. A compact 0.1-14-GHz ultra-wideband low noise amplifier in 0.13-µm CMOS. IEEE T. Microw. Theory, 58(10): 2575-2581.

Chang, T., J. Chen, L.A. Rigge and J. Lin, 2008. ESD-protected wideband CMOS LNAs using modified resistive feedback techniques with chip-on-board packaging. IEEE T. Microw. Theory, 56(8): 1817-1826.

Chen, K.H. and S.I. Liu, 2012. Inductorless wideband CMOS low-noise amplifiers using noise-canceling technique. IEEE T. Circuits Syst., 59(2): 305-314.

Chen, P., J. Kao, P. Huang and H. Wang, 2011. A novel distributed amplifier with high gain, low noise and high output power in 0.18 µm CMOS technology. Proceeding of IEEE MTT-S Microwave Symposium Digest, Baltimore, USA, Jun 5-10, pp: 1-4.

Hsu, Y.Y., B.J. Huang, J.L. Kuo and H. Wang, 2010. A compact fully integrated 5.2-11.2 GHz low noise amplifier using 0.18-µm CMOS technology. Proceeding of Asia Pasific Microwave Conference, pp: 338-341.

Lu, Y., K.S. Yeo, A. Cabuk, J. Ma, M.A. Do and Z. Lu, 2006. A novel cmos low-noise amplifier design for 3.1 to 10.6-GHz ultra-wide-band wireless receivers. IEEE T. Circuits Syst., 53(8): 1683-1692.

Marufuzzaman, M., M.B.I. Reaz, M.S. Rahman and M.A.M. Ali, 2010. Hardware prototyping of an intelligent current dq PI controller for FOC PMSM drive. ICECE 6th International Conference on Electrical and Computer Engineering, Art no. 5700559, Malaysia, pp: 86-88.

Moezzi, M. and M.S. Bakthtiar, 2012. Wideband LNA using active inductor with multiple feed-forward noise reduction paths. IEEE T. Microw. Theory, 60(4): 1069-1078.

Mogaki, S., M. Kamada, T. Yonekura, S. Okamoto, Y. Ohtaki and M.B.I. Reaz, 2007. Time-stamp service makes real-time gaming cheat-free. Proceeding of the 6th ACM SIGCOMM Workshop on Network and System Support for Games, NetGames '07, pp: 135-138.

Mohd-Yasin, F., A.L. Tan and M.I. Reaz, 2004. The FPGA prototyping of Iris recognition for biometric identification employing neural network. Proceeding of the International Conference on Microelectronics, ICM, Malaysia, pp: 458-461.

Nilsaz, A.S., M.K. Parashkoh, H.G. Zadeh, Z. Zou, M.B. Nejad and L.R. Zheng, 2010. Low power 0.18µm CMOS ultra wideband inductor-less LNA design for UWB receiver. Proceeding of IEEE Conference Circuits and Systems, Iran, pp: 855-858.

Reaz, M.B.I. and L.S. Wei, 2004. Adaptive linear neural network filter for fetal ECG extraction. Proceeding of the International Conference on Intelligent Sensing and Information Processing, ICISIP. Chennai, India, Jan 4-7, pp: 321-324.

Reaz, M.B.I., F. Mohd-Yasin, S.L. Tan, H.Y. Tan and M.I. Ibrahimy, 2005. Partial encryption of compressed images employing FPGA. Proceeding of IEEE International Symposium on Circuits and Systems, Art No. 1465105, pp: 2385-2388.

Reaz, M.B.I., M.T. Islam, M.S. Sulaiman, M.A.M. Ali, H. Sarwar and S. Rafique, 2003. FPGA realization of multipurpose FIR Filter. Proceeding of the 4th International Conference on Parallel and Distributed Computing, Applications and Technologies, PDCAT, Malaysia, pp: 912-915.

Reaz, M.B.I., F. Choong and F. Mohd-Yasin, 2006. VHDL modeling for classification of power quality disturbance employing wavelet transform, artificial neural network and fuzzy logic. Simul., 82(12): 867-881.

Reaz, M.B.I., F. Choong, M.S. Sulaiman and F. Mohd-Yasin, 2007a. Prototyping of wavelet transform, artificial neural network and fuzzy logic for power quality disturbance classifier. Electr. Pow. Compo. Syst., 35(1): 1-17.

Reaz, M.B.I., M.I. Ibrahimy, F. Mohd-Yasin, C.S. Wei and M. Kamada, 2007b. Single core hardware module to implement encryption in TECB mode. Inform. Midem, 37(3): 165-171.