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Design of a High Speed Low Power 2's Complement Adder Circuit

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Abstract: Most modern computers use the 2's complement system to represent negative numbers and to perform subtraction by using adder circuit. Several criteria such as speed, power consumption and propagation delay must be taken into account in the design of arithmetic circuits. This study proposed a technique to build an improved 2's complement adder circuit using the combination of existing XOR and new full adder structure. The design is implemented in CEDEC 0.18 µm CMOS process at 3.3v supply voltage. The results showed that the circuit is required only 0.83nW with maximum delay of 50.08 ns for 1-bit adder. Delay and power dissipation of different adder circuits for various numbers of inputs are also simulated and analyzed. Comparison study showed that the design is given a better critical delay and low power dissipation compared to other research studies. Moreover, because of using less number of transistors, the design occupied small die area. The compact size of the circuit with low power and low propagation delay is highly required in arithmetic circuits.

Keywords: CMOS, full adder, 2's complement adder, PTL, PDP, XOR

INTRODUCTION

Addition is a fundamental operation in any digital system. Adder circuit is very important component in digital systems as it is used in other basic digital operations like subtraction, multiplication and division (Akter *et al*., 2008a, b; Reaz *et al*., 2007a, b; Marufuzzaman *et al*., 2010; Reaz *et al*., 2003; Reaz *et al*., 2005). Adder and subtract or circuit are widely used in electronic and communication systems such as digital encoders, AM and FM modulation and neural networks (Reaz *et al*., 2006; Reaz and Wei, 2004; Mohd-Yasin *et al*., 2004; Mogaki *et al*., 2007). Several designs have been proposed by researchers since 1990's (Tsay and Newcomb, 1991; Chaoui, 1995; Floyd, 1998). Among them Chaoui (1995) proposed voltage adder but only positive voltage is produce although both positive and negative supply voltages are applied. The adder based on op-amp circuit offers a simple technique to get positive and negative voltage at the output (Floyd, 1998). New technique for programmable voltage adder has been proposed by Monpapassorn (2005) using a current conveyor analog switch and Montree (2011) has been designed a fully CMOS programmable voltage adder to overcome the drawbacks in Monpapassorn (2005).

Recently, most researchers have moved to design the adder circuit based on reversible gates for quantum computing. Rangaraju *et al*. (2010) proposed reversible parallel n-bit adder with a control input signal. Emam and Elsayed (2010) proposed 2 novel designs of adder using reversible, i.e. reversible gate that can study singly as a full adder and 2's complement reversible adder. A novel design to detect an overflow in 2's complement computation using modified reversible controlled adder has been designed by Sultana and Radecka (2011). Kaur and Dhaliwal (2012) designed reversible adder that offers less hardware complexity and more efficient in terms of garbage outputs. Nevertheless, these design the adder using reversible gates have complexity circuit and produce more power dissipation.

In this study, novel 2's complement adder circuit is proposed that can be implemented in modern digital systems. The circuit is designed in CEDEC 0.18µm process by combining the Static Energy Recovery (SER) XOR with modified 10T full adder in order to reduce the power dissipation and die area (Bui *et al*., 2002). The proposed adder is then applied to design a 4-bit and 8-bit ripple adder. The new structure of adder shows less power dissipation and low propagation delay compared to conventional and previous studies and it is very suitable to be implemented in compact module arithmetic.

2'S COMPLEMENT ADDER CIRCUIT ARCHITECTURE

The operations of addition and subtraction of signed/unsigned numbers can be performed using only

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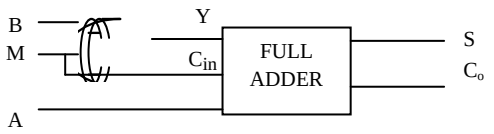


Fig. 1: Block diagram of 1 bit full adder circuit (Mano and Ciletti, 2006)

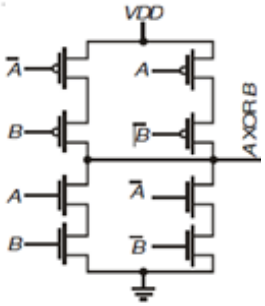


Fig. 2: Conventional XOR (Weste and Harris, 2010)

the addition operations if 2's complement form is used to represent negative numbers. The 2's complement adder circuit is based on block diagram as shown in Fig. 1, which consists of XOR and full adder circuit (Mano and Ciletti, 2006). XOR is implemented as a complementary system with input M as a controller. M is connected to Cin to perform the 2's complement process. In LOW state of M, XOR past the B-number to the full adder and the circuit performs addition of the A and B numbers. When the M level is HIGH, XOR invert the B-number and Cin = 1 will add with $\overline{B}$ to complete the 2's complement. Then, full adder circuit adds the 2's complement of B with the A-number. This operation shows that when M = 1, the circuit subtracts B-number from the A-number.

Previous XOR and full adder architectures: From the theory described above, XOR is implemented as a complementary system. The Boolean function of XOR is given by Eq. (1):

$$Y = \overline{M}B + M\overline{B} = M \oplus B \quad (1)$$

Figure 2 shows the conventional gates level of XOR using static complementary CMOS. The method is robust and can operate with full output voltage swing. The layout design is straightforward and using a small number of interconnection wires. However, the design needs complementary signal values to control nMOS and pMOS gates and needs an inverter to fit the complementary output. Besides, the power dissipation and cell delay of this circuit is high because of large number of transistors (12T included 4T inverter) (Weste and Harris, 2010).

XOR gate can also be implemented by various type of XOR design in the literature with less number of

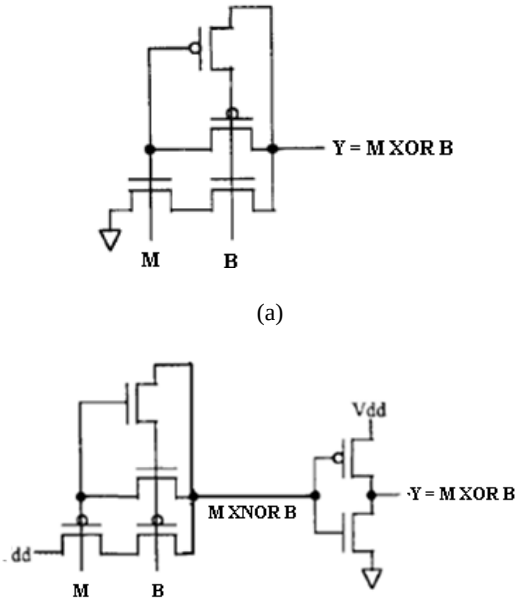


Fig. 3: SER XOR (a) without driving output (b) with driving output (Wang *et al*., 1994)

Table 1: Comparison output between SER XOR in Fig. 3

M	B	Y (a)	Y (b)
0	0	Weak 0	Strong 0
0	1	Strong 1	Strong 1
1	0	Strong 1	Strong 1
1	1	Strong 0	Strong 0

transistors. Static Energy Recovery (SER) XOR (Wang *et al*., 1994) with low complexity can be achieved with only 4 transistors in Pass Transistor Logic (PTL) as shown in Fig. 3a. It consumes less power dissipation compared to conventional XOR (Wang *et al*., 1994). Despite the saving in transistor numbers, the output voltage level is degraded at certain input combinations due to the threshold problem. It may cause circuit malfunction at low supply voltage. The drawback of the SER XOR can be overcome by cascading a standard inverter to the SER XNOR circuit, a new type of XOR structure as shown in Fig. 3b (Wang *et al*., 1994). With driving output, the signal at the output end will be prefect in all cases. The defect of a 4 transistors type is that the output level will be higher or lower than the normal case by the threshold voltage (Wang *et al*., 1994). Table 1 shows comparison output of 4T SER XOR and 6T SER XNOR.

A detailed study was carried out by Mishra *et al*. (2010) to determine the best design of XOR. They found that XORs with pass transistor logic (Bui *et al*., 2002) consumed less power and XOR with feedback transistor is best in speed performance (Chang *et al*., 2005), Nevertheless, XOR with feedback transistor have high total of transistor, therefore increase the size and cost.

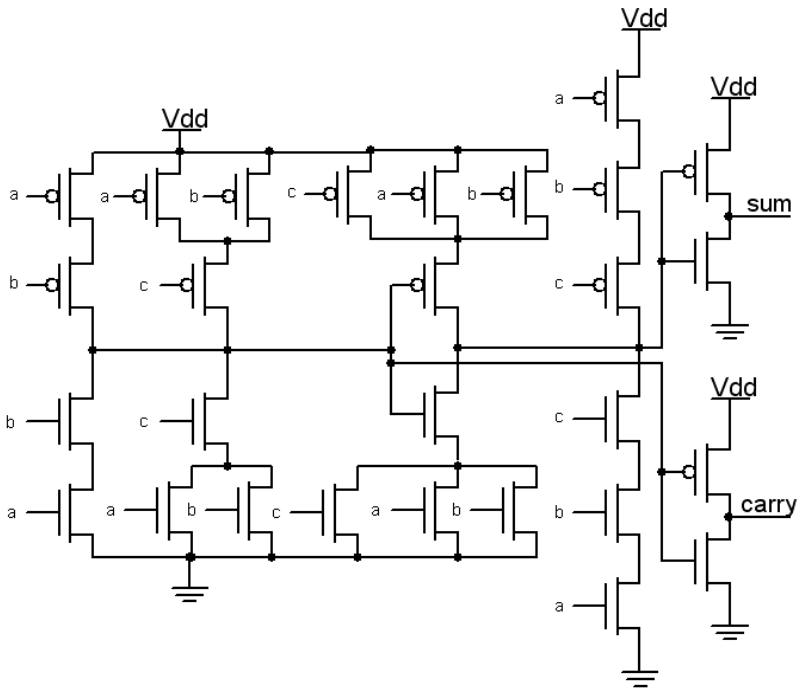


Fig. 4: Conventional CMOS full adder (Weste and Harris, 2010)

Full adder is a combinational circuit that performs the arithmetic sum of three numbers: A, Y and a carry in, Cin, from previous addition. The logic function of a full adder can be presented as Eq. (2) and (3):

$$\text{Sum} = \overline{A}.\overline{Y}.C_{in} + \overline{A}.Y.\overline{C_{in}} + A.\overline{Y}.\overline{C_{in}} + A.B.C_{in} = A \oplus Y \oplus C_{in} \quad (2)$$

$$C_{out} = A.Y + Y.C_{in} + A.C_{in} \quad (3)$$

The above equations can rewrite as:

$$\text{Sum} = \overline{\overline{A \oplus Y} \oplus C_{in}} \quad (4)$$

$$C_{out} = (\overline{A \oplus Y})C_{in} + (A \oplus Y)A \quad (5)$$

The conventional CMOS full adder as shown in Fig. 4 is implemented by 28 transistor (Weste and Harris, 2010). It advantages and disadvantages similar to XOR conventional circuits that have been mentioned above since it used the static complementary CMOS. The equations of the conventional full adder are present as Eq. (2) and (3).

There are variety of adders that implemented by 10 transistors (10T) in the literature with different performances (Bui *et al*., 2002; Shalem *et al*., 1999). The Static Energy Recovery Full adder (SERF) as shown in Fig. 5 is realized by 2-XNOR gates and one 2x1 MUX (Shalem *et al*., 1999). 2-XNOR with 4 transistors is used for Sum and 2x1 MUX with 2 transistors is used for carry output function. The design

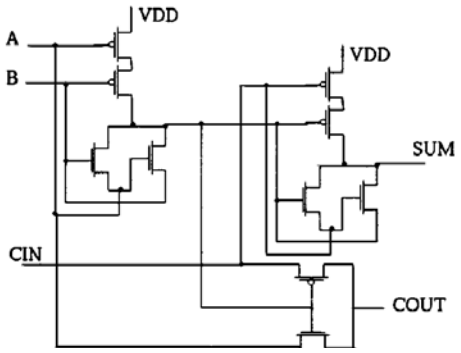
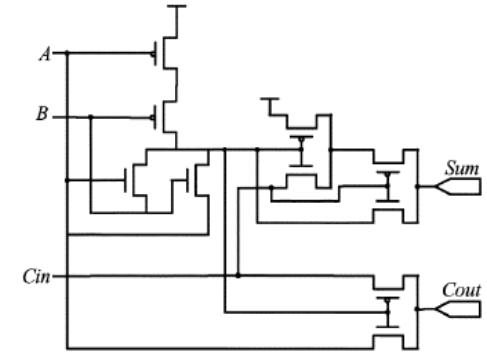


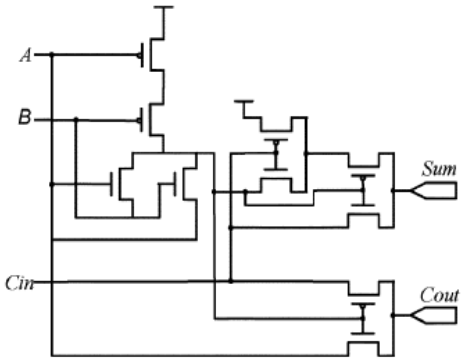
Fig. 5: SERF full adder (Shalem *et al*., 1999)

is low power consumption because no direct path to the ground and the charge stored at the load capacitance is reapplied to the control gates. This condition reduces the total power consumption by reducing the short circuit power consumption. Nevertheless, it may malfunction at low supply voltage and have degraded output at certain input combinations (Shalem *et al*., 1999).

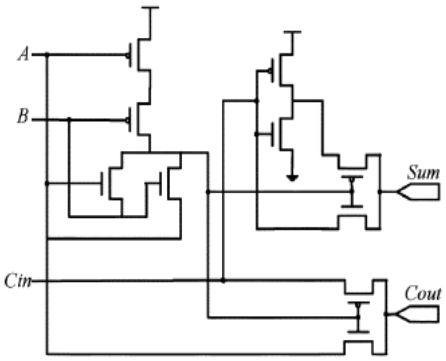
Based on Static Energy Recovery, (Bui *et al*., 2002) proposed 41 new designs of full adders. The 3 best designs are 9A, 9B and 13A. The full adder 9A is shown in Fig. 6a implemented by SER XNOR, 4T groundless XNOR and 2X1 MUX while full adder 9B can be designed by interchanging the inputs of 4T groundless XNOR of 9A design as shown in Fig. 6b. The full adder 13A structure, which is consisting of SER XNOR and inv MUX, is shown in Fig. 6c. The 9B and 13A designs have lowest power dissipation



(a)



(b)



(c)

Fig. 6: Various full adder design based on SER XNOR (a) 9A (b) 9B (c) 13A (Bui *et al*., 2002)

compared to conventional and SERF style. Both structure consume on average 10% less power and have higher speed compared with previous circuits. At low supply voltage, these structures have problem in threshold-voltage loss of PTL.

For recent years, most researchers designed a full adder by using more than 10 transistors to solve the threshold-loss problem and to avoid the malfunction of the circuit at low supply voltages (Sinha *et al*., 2011; Hassoune *et al*., 2010; Hernandez and Aranda, 2011). Sinha *et al*. (2011) proposed anew circuit using the 11T

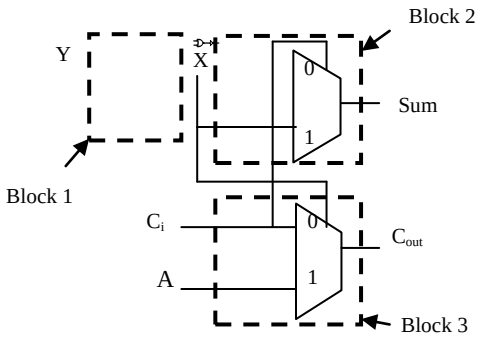


Fig. 7: Full adder cell formed by three main logical blocks

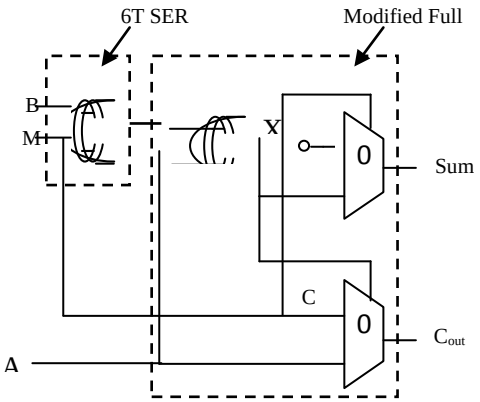


Fig. 8: Block diagram of the proposed adder circuit

full adder that can generate a full swing voltage and can operate at low voltage. Several researchers proposed full adder based on pass transistor with the number of transistors more than 20T to achieve better performance (Hassoune *et al*., 2010; Hernandez and Aranda, 2011). Nevertheless, design with high count of transistor would increase the area and cost.

Proposed adder circuit architecture: Adder circuits play an important role in classical computing. Before presenting the proposed circuit for addition and subtraction, a new 10 transistor (10T) full adder circuit, modified from 13A structure is modeled. 13A structure is chosen as it has less number of transistors and minimum power delay product (Bui *et al*., 2002). This full adder is divided into three blocks that is Block 1, Block 2 and Block 3. Block 1 implements the SER XNOR gate; Block 2 and Block 3 implement the 2x1 MUX for Sum and Count Function respectively. Figure 7 shows the proposed full adder cell formed by three main logical blocks. Both multiplexer is implemented by using PTL and total transistor for our full adder is 10 transistors.

This research is proposed a new 2's complement adder with less number of transistors. The design is based on block diagram in Fig. 1. To realize these

Table 2: Main design parameters of the proposed circuit

Voltage (min/max)	Temp.	Freq.	W/L (μm)
2 V/3.3 V	27 °C	10 MHz	nMOS : 1/0.18 pMOS Inverter (2/0.18) pMOS XOR (4/0.18) pMOS MUX (4/0.18)

structures, a combination of XOR gate with new full adder circuit is used. The adder circuit is implemented by one XOR, one XNOR and two 2x1 multiplexers. XOR gate used 6 Transistors (6T) with driving output and XNOR gate used 4 transistors without driving output. Fig. 8 shows the proposed 2's complement adder circuit block diagram.

The main design parameters of the proposed circuit are shown in Table 2. The design is simulated with 3.3V supply voltage at 10 MHz frequency and in 27°C temperatures. The performance of power dissipation, propagation delay and power delay product is analyzed. Proper (W/L) ratio is being chosen for optimizing the design performance without decreasing the power supply.

Schematic diagram of the proposed adder circuit is shown in Fig. 9. The proposed circuit is designed and simulated in CEDEC 0.18 μm CMOS process. The conventional adder and prior 10T full adders are redesigned using the same process technology. All prior 10T full adders are combined with 6T SER XOR to realize the adder function.

RESULTS AND DISCUSSION

Four different input sets along with conventional CMOS adder at the schematic level are designed in this research. Default values of the channel Width (W) and Length (L) for NMOS and PMOS in CEDEC's 0.18-micron technology are 1.4 and 0.18 μm, respectively. With the default value, the minimum power delay product of proposed circuit is 50.06×10-18 J. To reduce the delay and power consumption, W is varied from 2μm to 4μm for PMOS and 1μm for NMOS. All prior and new circuit were designed with minimum transistor sizes and then simulated. The new transistor sizing can reduce the Power Delay Product (PDP) up to 41.57×10-18 J for 1-bit circuit.

Each adder circuit has been analyzed in terms of power dissipation, propagation delay and PDP at supply voltage and frequency of 3.3V and 10MHz respectively with temperature 27°C. Propagation delay is the time between the fastest input signal and the output signal. The maximum value of the delay measured for the sum and carry output is the critical delay. The PDP is a quantitative measure of the efficiency and a compromise between power dissipation and speed and can be calculated by equation:

$$\text{PDP} = \text{Average Power X Critical Delay} \quad (6)$$

The simulated snapshot input/output waveform of the proposed circuit is shown in Fig. 10 and the corresponding truth table is shown in Table 3. The delay is measured from 50% of the input voltage swing to 50% of the output voltage swing for each transition. The maximum delay is taken as the cell delay.

According to Table 3, XOR have a strong output (Y) for all input combinations. Nevertheless, the proposed design has some degraded output. This result shows that the proposed circuit has limitation in the

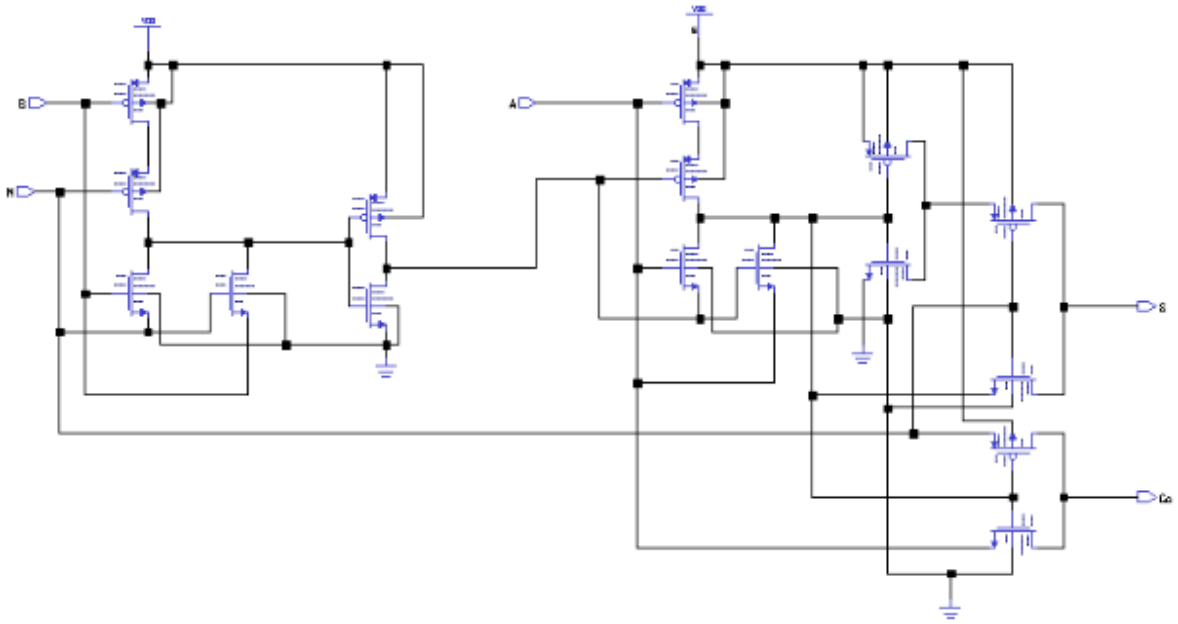


Fig. 9: Schematic of the proposed adder circuit

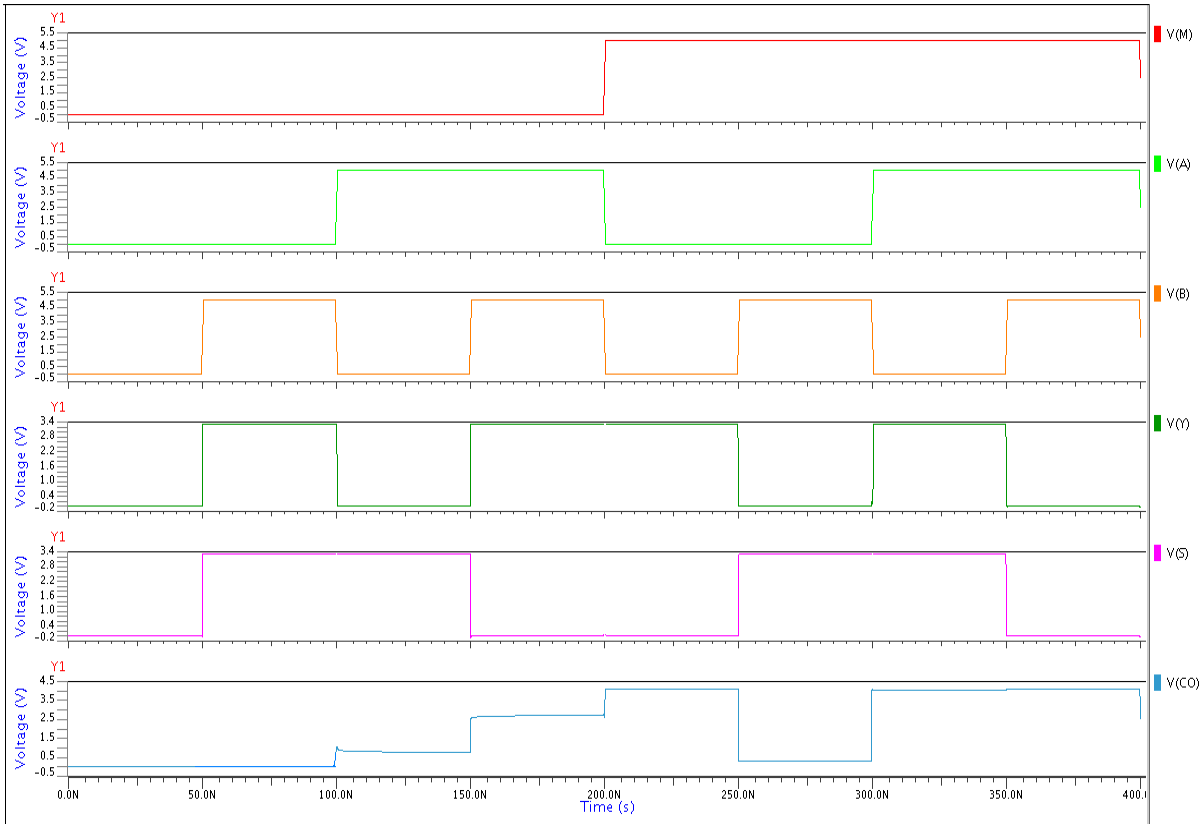


Fig. 10: Simulation snapshot waveforms of the proposed 1-bit adder

Table 3: Truth table of the proposed 1-bit adder

M	A	B	Cin	Y	Cout	Sum
0	0	0	0	Good 0	Strong 0	Strong 0
0	0	1	0	Good 1	Strong 0	Strong 1
0	1	0	0	Good 0	Weak 0	Strong 1
0	1	1	0	Good 1	Weak 1	Strong 0
1	0	0	1	Good 1	Strong 1	Strong 0
1	0	1	1	Good 0	Strong 0	Strong 1
1	1	0	1	Good 1	Strong 1	Strong 1
1	1	1	1	Good 0	Strong 1	Strong 0

Table 4: Comparative performance for all 1-bit adders

Design	Power (nW)	Max. delay (ns)	PDP (x10-18)
Conventional	1.38	51.92	71.65
6T SER XOR and SERF	0.95	70.13	66.62
6T SER XOR and 9A FA	1.07	52.24	55.90
6T SER XOR and 13A FA	0.90	60.18	54.16
6T SER XOR and This FA	0.83	50.08	41.57

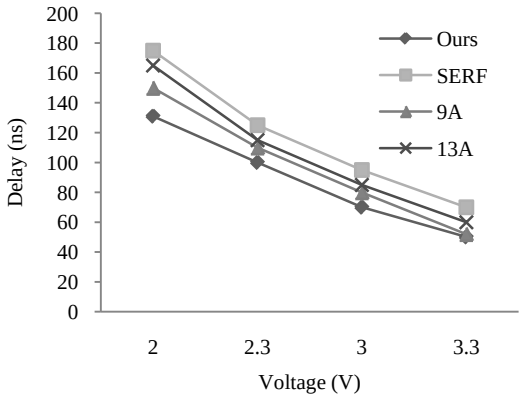


Fig. 11: Delay comparison between various designs of adder

threshold-loss of the pass transistors. The comparative performance for all 1-bit adders is shown in Table 4 at 3.3V supply voltage.

All design with 10T full adder requires the minimum VDD of 2V for properly function. For VDD below 2V, design with full adder 13A produce a wrong SUM for input combination of ABC in = 011 while the rest give the wrong Cout at the same input combination. The delay and power comparison is shown in Fig. 11 and 12 respectively, which show that the delay and power dissipation of the proposed design is the lowest among all other designs. Moreover, for different supply voltage varied from 2V to 3.3 V the proposed design is also tested and the results are similar.

The simulation is conducted for difference adder sizes: 4-bit and 8-bit. The comparison is done for average power dissipation as shown in Table 5. It is being shown that the proposed design gives the lowest power dissipation compared to others research studies.

Finally, the new adder circuit layout is implemented in CEDEC 0.18 µm CMOS process. The

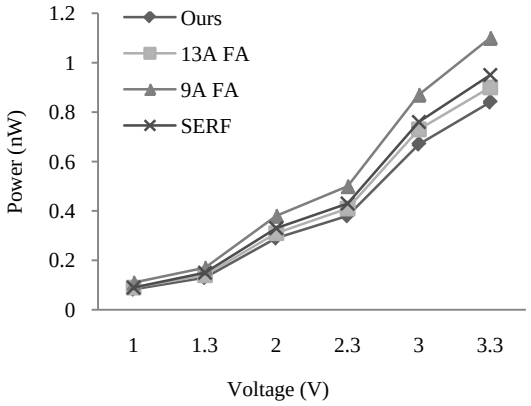


Fig. 12: Power comparison between various designs of adder

Table 5: Average power comparison between various adders for 4-bit and 8-bit IO

	Average Power (µW)	
Design	4-bit	8-bit
Conventional	22.83	45.67
6T SER XOR and SERF	9.90	19.80
6T SER and 9A FA	6.84	13.67
6T SER and 13A FA	12.44	29.44
6T SER and our FA	3.71	9.674

layout is designed for 1-bit and 8-bit inputs as shown in Fig. 13 and 14 respectively. Form the figures it is also shown that the total area of 1-bit adder is only 411.6 µm 2 and for 8-bit adder the area is only 4014.9 µm 2. The small area of the proposed circuit is a good candidate for arithmetic logic circuit.

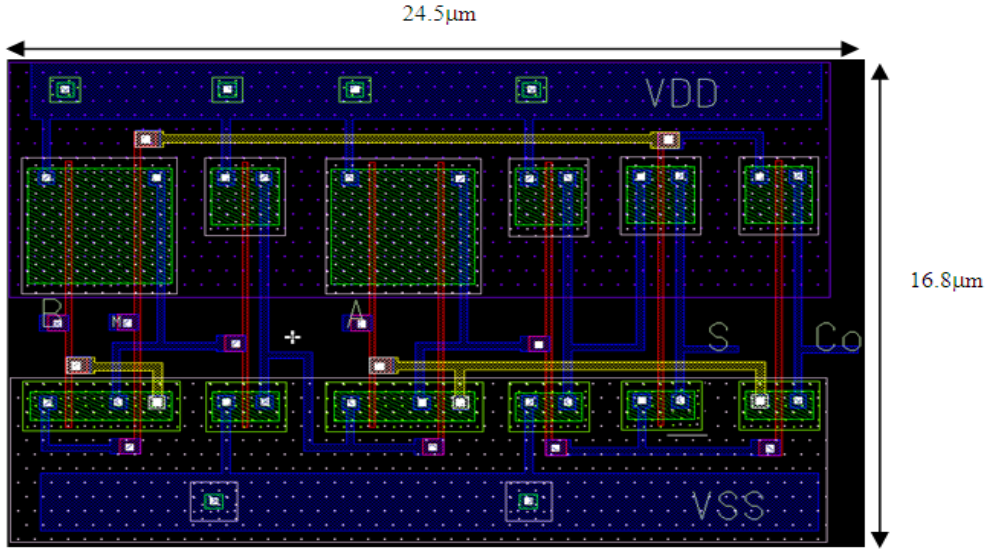


Fig. 13: Layout of the 1-bit proposed adder

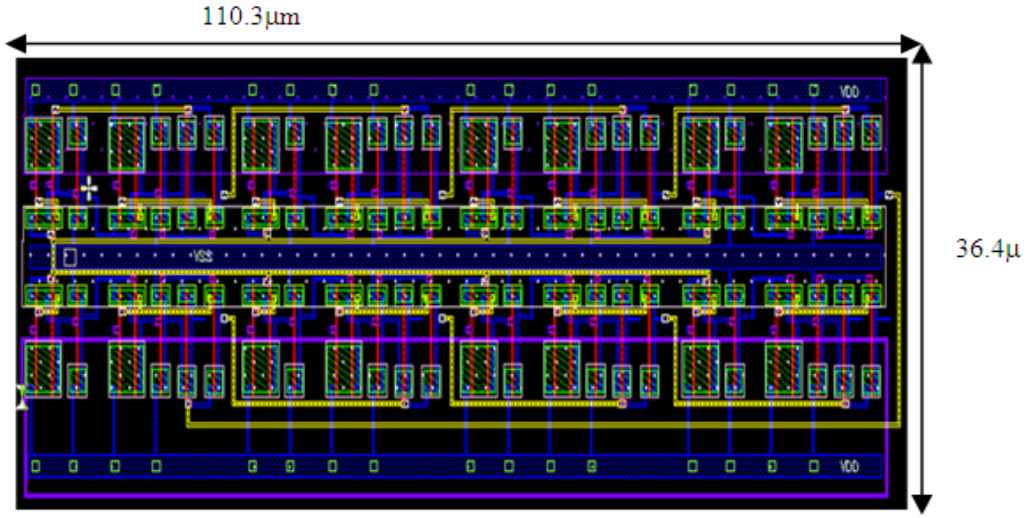


Fig. 14: Layout of 8-bit proposed adder

CONCLUSION

In this study, a new 2's complement adder realized by exiting XOR and new full adder structure is proposed. The proposed designs possess the advantages of less transistor counts compare with conventional designs. Different circuit logic style have been implemented, simulated, analyzed and compared at 3.3V supply voltage with temperature 27°C. The analysis and simulation results showed that a worst-case delay and total power consumption in this new design are better than the prior studies. The performance analysis of adder circuit has been presented for 1-bit, 4-bit and 8-bit. The layout is realized by CEDEC's Silterra 0.18 µm CMOS process technology with total area of 411.6 µm 2 and 4014.9 µm 2 for 1-bit and 8-bit respectively. The compact size of the proposed design with low power dissipation and low propagation delay is certainly plays a crucial role in building arithmetic circuits.

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