

Design of an 8-cell Dual Port SRAM in 0.18- μm CMOS Technology

Mohammad Mahdi Ariannejad, Mamun Bin IbneReaz, Md. Syedul Amin and F.H. Hashim

Department of Electrical, Electronic and Systems Engineering Universiti Kebangsaan
Malaysia, 43600 UKM Bangi, Selangor, Malaysia

Abstract: Low power and low area Static Random Access Memory (SRAM) is essential for System on Chip (SoC) technology. Dual-Port (DP) SRAM greatly reduces the power consumption by full current-mode techniques for read/write operation and the area by using Single-Port (SP) cell. An 8 bit DP-SRAM is proposed in this study. Negative bit-line technique during write has been utilized for write-assist solutions. Negative voltage is generated on-chip using capacitive coupling. The proposed circuit design topology does not affect the read operation for bit interleaved architectures enabling high-speed operation. Designed in 0.18- μm CMOS process, the area is only 1.2 times of the SP-SRAM and its power is 1.3 times of the SP-SRAM when the two ports simultaneously work at the same frequency. Simulation results and comparative study of the present scheme with state of-the art conventional schemes proposed in the literature for 45 nm CMOS technology show that the proposed scheme is superior in terms of process-variations impact, area overhead, timings and dynamic power consumption. The proposed negative bit-line technique can be used to improve the write ability of 6 T Single-Port (SP) as well as 8 T DP and other multiport SRAM cells.

Keywords: Demultiplexer, memory cell, negative bit-line, SRAM, tri-state buffer

INTRODUCTION

Portable computing and communication devices demand high-speed computation and complex functionality with low power consumption (Akter *et al.*, 2008a, b; Reaz *et al.*, 2007a, b; Marufuzzaman *et al.*, 2010; Reaz *et al.*, 2003; Reaz *et al.*, 2005; Kaur and Noor, 2012). The emerging market for portable SoC demand low power SRAM without paying the price of speed reduction. The main factor used for power reduction is the supply voltage reduction (Reaz *et al.*, 2006; Reaz and Wei, 2004; Mohd-Yasin *et al.*, 2004; Mogaki *et al.*, 2007). Two major design trends to reduce the supply voltage while keeping good speed performances. The 1st is to have a low Threshold Voltage (VT), to achieve the good speed and the second is to use a boosted word line scheme (decreasing the memory cell access time) (Elmasry, 2000). These techniques are costly in term of process and design.

High speed, low power and compatibility with standard technology SRAM are essential for System on Chip (SoC) technology. An 8 bit DP-SRAM is proposed in this study utilizing the Negative bit-line technique. In the design consideration, various types of designs are discussed. First a 6 T-SRAM (1 WR) and two types of 8 T-SRAM cell (2 WR 1 WIR) are discussed. Thereafter, the (1 W1 R) cell principle with

external unit is explained and SNM sensitivity and the write/read operations time of 1 WR 1 W1 R cell are compared. Then the methodology is followed by Result and Discussion section and finally the study is concluded.

DESIGN CONSIDERATION

A conventional SRAM cell consisting of six-transistors, two nMOS transistors as transfer devices, two pull-up pMOS transistors and two pull-down nMOS transistors is shown in Fig. 1, 2 and 3 (Elmasry, 2000). The single-port SRAM has one set of address and data interface. So, at the same time SRAM do either read-operation or write-operation, that is why its operation is often denoted as "1WR". However, Fig. 2 is two write-read (2WR) type of 8T-SRAM memory cell which has similar structure with the standard single-port SRAM. But it has two sets of data and address paths. So, this is a dual-port memory cell. Each address and data path can complete the write and read operation independently.

Figure 3 is also a DP storage cell, which still have 2 sets of address and data paths, but one of the ports do write operation only and the other do read operation only (1WIR). In these 2 types of 8T-SRAM, the 2WR type of memory cell can also operate as a 1WIR, but

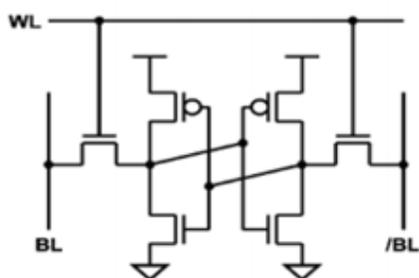


Fig. 1: 6T-SRAM (1WR)

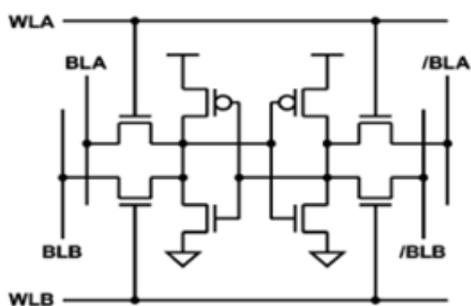


Fig. 2: 8T-sram (2WR)

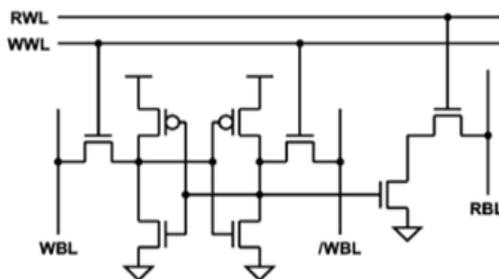


Fig. 3: 8T-SRAM (1W1R)

the 1W1R type of memory cell cannot operate as a 2WR cell. As such, the 2 WR cell has more access-flexibility than 1W1R cell. Required by many SoC designs, 1WR SRAM is mainly used to store instructions. Besides, memory cell can also be used in transfer registers and general purpose registers, where the memory with one write port and one read port is needed only. So, the structure showed in Fig. 3 is the best option and use\in the system proposed by Kai-ji *et al.* (2010) and Nii *et al.* (2009). As there are three kinds of DP SRAMs, we handle the conventional 8T SRAM, 10T SRAM with a single-end read port and 10T SRAM with differential read ports.

Soft errors and Single Event Upsets (SEU) are common problem in memory circuits. SEU occurs when a charged particle strikes a sensitive node and

flips the state of the SRAM cell from 0 to 1 and vice versa, causing a soft error. Current research suggests that the average rate of failure for complex chips may be in excess of four errors per year (Roche and Gasiot, 2005). There have been many solutions to increase the level of soft error protection of the SRAM cell. Protection method is an effective method which uses capacitors in SRAM cells to absorb the excessive charge (Artola *et al.*, 2011). Although they provide sufficient protection, they adversely affect the cell performance also.

The complementary data bits which are stored in a SRAM cell are latched by a pair of back-to-back inverters. Therefore, these data do not need to be refreshed. On the other hand, data that is stored in one transistor, one capacitor DRAM cell gets degraded over a period of time due to charge leakage. Therefore, for any high-speed operation, especially when the required memory density is low, SRAM memory is always the memory of choice. The advantage of using 2 DP arrays is that once the data is written into the memory, the data can be accessed from either port. For example, data that is written into the first array RAM-A in a first word line W1 can be accessed from either the left or right port of the array for a read operation. In order not to disturb the unselected cells, in each cycle only one word line of the dual-port array is activated.

The 10T SRAM with a single-end read port is the best as a dual-port SRAM in a 45-nm process technology. Although the conventional 8T SRAM has the least transistor count and is the most area efficient, the readout power becomes large and the cycle time increases due to the keeper circuits on the read bit lines. The 10T differential-port SRAM can operate fastest. In terms of the power efficiency, however, even if the sense point is set to 50 mV, most cells sink the bit line more than 50 mV, which leads to the power overhead. As a result, the 10T single-end SRAM always consumes the lowest readout power of the three.

METHODOLOGY

An 8 bit DP-SRAM is proposed in this study. Negative bit-line technique during write has been utilized for write-assist solutions. Negative voltage is generated on-chip using capacitive coupling. The proposed circuit design topology does not affect the read operation for bit interleaved architectures enabling high-speed operation. The schematic diagram of the proposed DP SRAM is shown in Fig. 4. This design consists of 8 inverting latches and 8 tri-state buffers and 2 De-multiplexer. It has separate control signals for

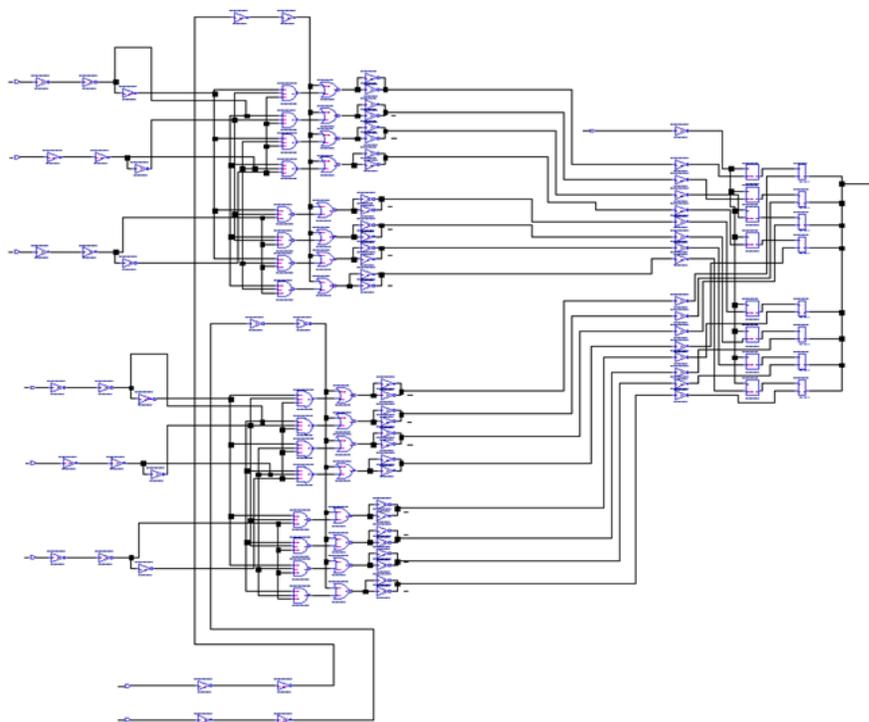


Fig. 4: The circuit diagram of the proposed 8-Cell SRAM

Table 1: Comparison of cell area and rectangle size between 6T, dual port 8T and logic ruled

90 nm LOP MOSFET (Low-Operating-Power)	SP: 6T-cell	DP: 8T-cell (this work)	DP: 8T-cell (logic-ruled)
Rectangle size (μm^2)	1.74×0.72	2.84×0.72	2.58×1.14
Cell area (μm^2)	1.2528	2.0448	2.9412
Ratio	1	1.63	2.35

read and write addresses. This allows for simultaneous read/write operations.

RESULTS AND DISCUSSION

In the 8T SRAM, an access time is a period from a time at which an RWL rises to $V_{DD}/2$ to a time at which an output of the sense amplifier is charged up to $V_{DD}/2$. In the 10T-S SRAM, an access time is a longer one: a periods from a time at which a read word line (RWL) rises to $V_{DD}/2$ to a time at which an output of the sense amplifier is charged up to $V_{DD}/2$, or a period from a time at which an RWL rises up to $V_{DD}/2$ to a time that an output of the sense amplifier is discharged down to $V_{DD}/2$.

In the 10T-D SRAM, an access time is a period from a time at which an RWL rises to $V_{DD}/2$ to a time at which a differential voltage between an RBL and /RBL is expanded to 50 mV, 100 mV or 200 mV. In all the SRAMs, the worst cell with the worst threshold-voltage variation determines the delay. In particular, in the 10T-D SRAM, even if the sense point is set to 50 mV, most cells sink the bit line more than

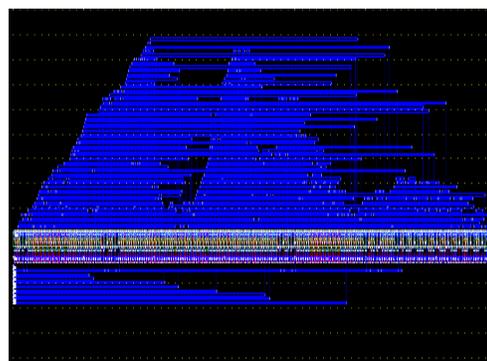


Fig. 5: A layout design of the 8-cell SRAM

50mV. A comparisons study of Cell area and Rectangle size between 6T and dual port 8T and logic ruled for 8T-cell is shown in Table 1. The proposed low voltage 8-cell SRAM layout is designed in CEDEC 0.18- μm CMOS process and shown in Fig. 5. The write and read time is a little longer than 6T-SRAM, 1W1R memory has significantly degrades the static noise margin than 6T-SRAM and the read-operation does not need the

pre-charge of the bit-line. 8T-SRAM can provide better stabilization, high speed and low power than 6T-SRAM.

CONCLUSION

A new CMOS buffer has been proposed which has no short-circuit power consumption. The output pull-up and pull-down transistors are driven by separate driving stages which ensure pull-up and pull-down transistors do not turn on simultaneously. The Dual port SRAM has ability to simultaneously read and write different memory cells at different addresses. The proposed negative bit-line technique can be used to improve the write ability of 6T Single-Port (SP) as well as 8T DP and other multiport SRAM cells.

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