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A Great Efficiency Full Adder Cell Based on Carbon Nano-Tube Technology

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Abstract: In this study, we present a very quick full adder cell that has high energy efficiency based on carbon nano-tube transistor technology This project and other circuits in this study were in different voltages and frequencies with HSPICE software .The results of show that the speed and efficiency of this circuit is obviously better than other circuits like: CMOS and CNFET. Also, this full adder that we present, make great ability to on outlet and it works properly in low voltages.

Keywords: CNFET, Full-Adder (FA), the diameter of nano-tube, transmission gate

INTRODUCTION

The difficulty of changing measure and physical limitation of silicon transistors , make designers to apply new Nano technology .one of the most hopeful and probable branches of Nano-technology is carbon nano-tube transistor . the usage of COMS transistors cause difficulties like high consumption of electrical current and increase of power consumption ; so, the carbon nano-tube transistors are going to be the alternative of silicon transistors. The general principle of operation and structure of carbon Nano-Tube transistors is similar to current transistors. If you continue using CMOS technology in design of electronic integrated circuits , it causes dimension reduction of COMS transistor based on more law that resulting to improve speed cast and power consumption; but the min aturization of transistors is going to finish , because the circuits are so compressed that the chips will be so hot and the high heat lead to increase the power consumption and decrease of general operation .In recent years, designers have been trying to design circuits based on carbon Nano-Tube transistors (Deng, 2007; Raychowdhury and Roy, 2004).

The summation is one of the main actions in mathematics and it is the base of many other mathematics actions like subtraction, multiplication and address operation. The full adder cell is main pat in complex arithmetic circuits and arithmetic processors and it is an important part of arithmetic and logic unit. The design of an adder with simple structure that has high speed and low power consumption can be very effective for simplifying the arithmetic algorithms and increase of computing system performance (Junming *et al*., 2001; Zimmermann and Fichtner, 1997; Chang *et al*., 2003). So, the improve of performance of this circuit will improve the performance of all parts of system (Zimmermann and Fichtner, 1997; Chang *et al*., 2003). Thereby many designers design different plans with different methods to improve the performance of all parts of system, in recent years.

In this study, we present a full adder cell based on carbon Nano-Tube transistors and then, we compare it with COMS and CNFET adder cell in different situations .Here, we explain about this adder briefly.

COMS adder circuit (Zimmermann and Fichtner, 1997) is made of 28 transistors and designers use COMS technology to make it. Bridge (FA24T) adder cell (Navi and Kavehei, 2008), has 24 transistors and it is design based on low power structure and high efficiency and fully symmetrical bridge. Adder circuits Hybrid-1(Chang *et al*., 2003), Hybrid-2 (Goel *et al*., 2006) are designed based on low power XOR/XNOR Circuit and respectively has 26 and 24 transistors. TG (Transmission Gate) FA cell (Weste and Eshraghian, 1993) has 18 transistors and it is designed based on transfer Function theory and XOR Gate. and CNFET-based FA cells including the CNT-FA-1 based on minority function with 8 transistors and 7 capacitors (Navi *et al*., 2009), CNT-FA-2 is based on majority-not, NAND and NOR functions which is composed of 12 transistors and 8 capacitors (Navi *et al*., 2010a) and the CNT-FA-3 based on minority function and utilizes 5 capacitors and 8 transistors (Navi *et al*., 2010b).

CARBON NANOTUBE TRANSISTOR

The basic idea of this carbon nano-tube was discovered by Igima on 44, by chance (Ijiima, 1991). It is a layer of granite that it is twisted and ruled with special angle. (Carbon nano-tube has interesting and

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special and rare characteristic but the characteristics which make this new arrangement of carbon atom to an important material in micro Electronic are:

- Transfering of Electrons Ballestic in length of tube.
- The carbon nano-tube can be conductor and semi-conductor by changing the angle of twisting on graphit layer. Carbon nano-tube characterize by chiral vector (C_h) and C_h calculated by nexus (Deng, 2007):

$$\vec{C}_h = n_1\vec{a}_1 + \vec{a}_2 n_2 \quad (1)$$

$\vec{\alpha_1}$ and $\vec{\alpha_1}$ are unit vectors of an organized network of carbon atoms and (n_1, n_2) are Integers that show the of a point and a paper and they define the caberality of tube and characterize the nano-tube . (The length of C_h tube calculates by (2) formula (Deng, 2007) :

$$C_h = a\sqrt{n_1^2 + n_2^2 + n_1 n_2} \quad (2)$$

The diameter of CNT calculates by (3) formula and usually it is about a few nano-meters:

$$D_{CNT} = \frac{C_h}{\pi} = \frac{a\sqrt{n_1^2 + n_2^2 + n_1 n_2}}{\pi} \approx 0.078\sqrt{n_1^2 + n_2^2 + n_1 n_2} \quad (3)$$

The relation of eve voltage to geometric shape of nano-tube to achievement of different eve voltages is based on nano-tube diameter eve in CNTFET and it is marked by (4) formula:

$$V_{th} = \frac{0.43}{D_{CNT}(nm)}V \quad (4)$$

The carbon nano-tube divide to different group based on n_1 and n_2 integers. (If $n_1 = n_2$ we call the carbon nano-tube, Armichair. (If $n_1 = 0$ and n2 = 0, we call it zigzag and in other situations we call it chiral (Raychowdhury and Roy, 2004; Bok Kim *et al*., 2009).

The first nano-tube transistor with SWNT , metal contact and golden or platinum source Drin made by tans, Dekker and Verschueren in 443 (Tans *et al*., 1998).

A carbon nano-tube transistor is similar to a MASOFT and it includes 3 parts: source, Drin and gate. It means the basic operation of field effect nano-tube transistors is similar to current silicon transistors (Deng, 2007). In which, we consider a nano-tube as a channel and put an Also, such channel should be controlled by gate electrode. These transistors turn off/on by gate, electro statically (Chen, 2004). We introduce 3 different type of carbon NLT here, in brief:

- **Schottky barrier CNFET (SB-CNFET):** IT works based on Schottky barrier. In this kind of transistor the touch points of Drin and source joins directly to the channel of nano-tube. The length and width of Schottky barrier and so the conduction of it characterize by gate voltage electrostatically. Two important factors or these kind of transistors are, at first, the energy of barrier in Schottky barrier has limitation on CNTFEL conduction in on mood. Second, these kind of transistors present the characteristic of strong that limit the use of these transistors in circuits with the current logic of CMOS.
- **MOSFET-like CNFETs (MOS-CNFETs):** There is impurity through the carbon nano-tube (This impurity is strongly similar to current MOSFET. (These transistors have unipolar behavior. these kinds of transistors because of their physical similarities to silicon technology, the Si-MOS circuits with MOS-CNFETs circuits.
- **Band-to-band tunneling CNFET (T-CNFET):** This kind of transistor shows the strong am bipolar characteristics and it applies for design of low power consumption because of it cuts the #cut off $ current very well (Raychowdhury and Roy, 2007; Paul *et al*., 2006) .

PROPOSED FULL ADDER CELL

The main idea of this design is taken from TGA FA cell in Weste and Eshraghian (1993). The recommended adder designed based on transferring function adder designed based on transferring function and XOR gate. This circuit showed in Fig. 1. The out lets of recommended circuit build in 3 stages. In X knot and first stage, we build $A \oplus B$ and in Y knot we build A □ B and at last in other stages we build SUM and C_{out} outlets. The Sum and C_{out} functions in this adder calculate based on (5) and (6) formula.

$$SUM = (A \square B)C_{in} + (A \oplus B)\overline{C_{in}} \quad (5)$$

$$C_{out} = (A \square B)A + (A \oplus B)C_{in} \quad (6)$$

When we replaced a gate with two CNFET transistors, it does not need to con duct C_{in} signal and the number of up adder transistors is be creased. we consider the diameter of transferring gate of replacing nano-tube transistors, so large that the eve voltage of through fare is nearly zero and so, we don't experience the voltage drop in circuit outlet and the knots of outlet in this circuit are in complete sway that this factor give a high assurance to the circuit and it cases reduction in leakage wasting power.

We use from a newer design of XOR to perform this circuit and we use is instead of XOR in this circuit.

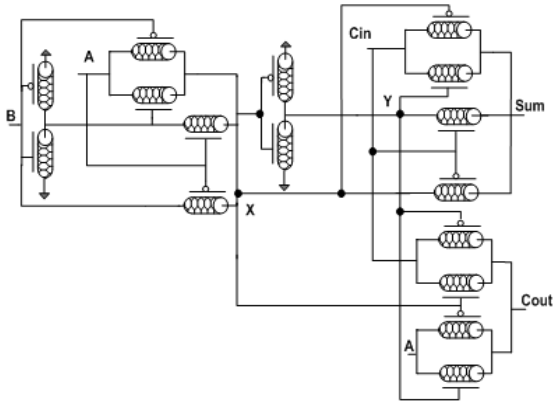

Fig. 1: The first draft of recommended full adder

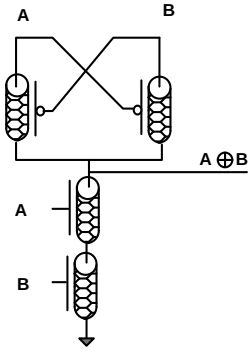

Fig. 2: The recommended XOR circuit

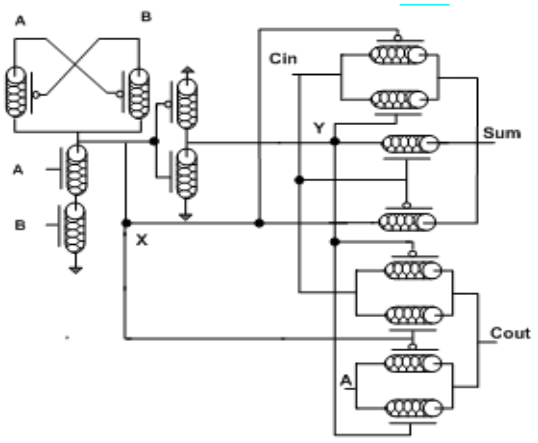

Fig. 3: The final model recommended full adder cell

Figure 2, the circuit of this XOR has2 less transistor than the XOR in this circuit that it had 6 transistors.

The first model of recommended adder cell (Fig. 3) We replaced transferring gate with current transistors and also, we used from a better structure of XOR function and finally, the increase of nano-tube diameter make it better than the former circuits in COMS technology all of above help us to achieve carbon nano-tube technology The results are, reduction in area of circuit, decrease of delay and therefore increase of efficiency Moreover, the let out signals in this circuit have complete sway and they performed just with 14 transistors.

The arc with largest average power and send data to that selected node in a unicast manner.

Table 1: Simulation results for the FA cells AT 0.65V and 0.5V supply voltage

Design	Delay ($*10^{-12}$ ec)	Power (10^{-7} W)	PDP (10^{-17} J)
0.5V			
CCMOS	451.07	2.1982	9.9155
CMOS-bridge	582.43	1.9915	11.599
Hybrid1	315.57	1.9788	6.2445
Hybrid2	323.47	2.1300	6.8902
TG	238.44	2.1641	5.1602
CNT-FA-1	101.37	3.7553	3.8067
CNT-FA-2	204.05	2.2528	4.5969
CNT-FA-3	64.228	3.1688	2.0353
Proposed design	55.121	2.8910	1.5935
0.65			
CMOS	129.40	4.0516	5.2429
MOS-bridge	195.05	3.6280	7.0767
Hybrid1	122.38	3.7031	4.5317
Hybrid2	117.20	3.9735	4.6336
TG	90.097	3.9022	3.5157
CNT-FA-1	45.044	6.0951	2.7455
CNT-FA-2	69.408	5.5519	3.8534
CNT-FA-3	41.342	5.4946	2.2716
Proposed design	37.134	5.3888	2.0010

SIMULATION AND COMPARING

Because ALL of the adder cells and the final model of proposed adder are simulated by HPSPICE software. To evaluate the proposed deigns, we simulated them using Synopsys HSPICE. 32nm CMOS technology has been used to simulate CMOS circuits and compact SPICE model which is proposed in Deng (2007) has been used to simulate CNFET-based circuits. This standard model has been used for unipolar MOSFET-like CNFET devices. The goal of this simulation is to increase the efficiency of all circuits by use of the minimal dimension for transistors. We perform all simulation on the same terms and room temperature. The operating frequencies are 250 MHz and 500 MHz. And power supplies were used 0.5 V and 0.65 V. The proposed designs optimized were for speed and power at 0.65 V and 250 MHZ.

Then we kept the circuit parameters constant and the simulation did in other terms.

To calculate the delay we have tested all possible input transitions (56 patterns) and then the delay has been measured for each transition. The maximum delay has been reported as the delay of each FA cell.

The average power consumption include: dynamic power consumption, short circuit, static and it measured by simulator. Because we want to make compromise between power and delay and also to general assessment of circuits efficiency, we calculated the multiply of Power in Delay (PDP).

The result of simulation in 250MHz frequency is in Table 1.

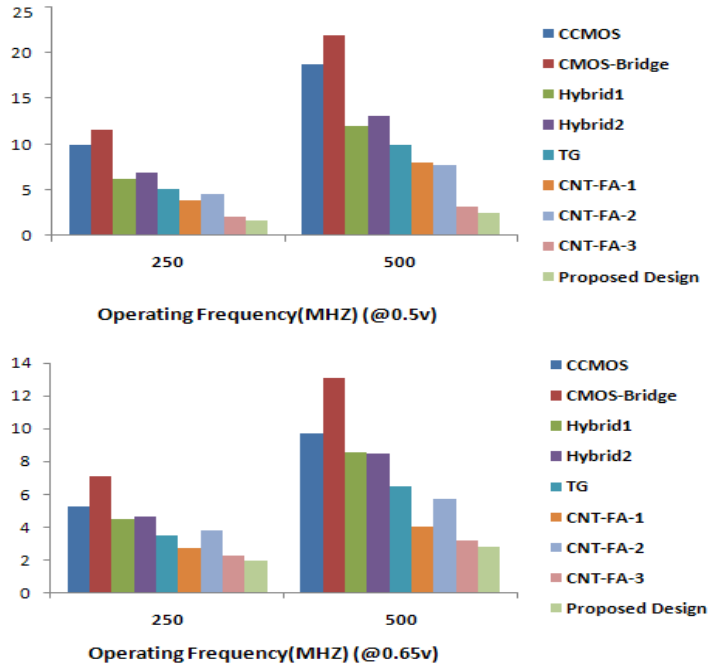

Fig. 4: PDP of the designs at different test conditions

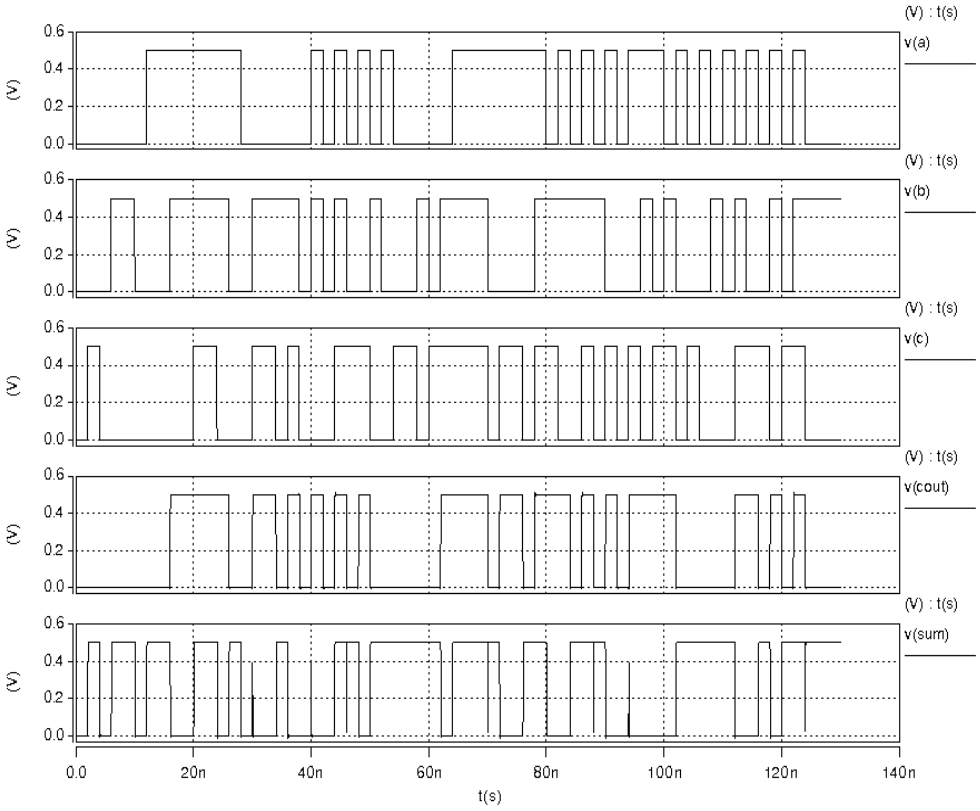

Fig. 5: Input and output waveforms of the proposed design (@ 250 MHz and 0.5V)

At 0.65 v supply voltage, the proposed design is Approximately 17. 3, 80.96, 69.65, 68.31, 58.78, 17.56, 46.6 and 10.1%, faster than CCMOS, Bridge-CMOS, Hybrid1, Hybrid2, TG, CNT-FA-1, CNT-FA-2 and CNT-FA-3, respectively. The PDP of the first proposed design is 61.83, 71.72, 55.84, 56.81, 43.08, 27.11,

47.07 and 11.91% better than CCMOS, Bridge-CMOS, Hybrid1, Hybrid2, TG, CNT-FA-1, CNT-FA-2 and CNT-FA-3 respectively.

Previous CNFET-based FA cells have more power consumption than CMOS FA cells but in our design reduced power consumption significantly. The PDP of the first proposed design is 96.4, 95.84, 94.64, 93.13, 95.11% and 91.38% better than CCMOS, Hybrid1, TG, CNT-FA-1, CNT-FA-2 and CNT-FA-3 respectively. The second design consumes less power and is more high-performance compared to the first proposed design. Finally, the results indicate that the third proposed cell consumes less power and has the best delay and PDP in comparison with the other cells mentioned in Table 1.

According to the Table 1, the delay and efficiency of proposed circuits better than the other adder circuits. The proposed circuit in all different voltages has the least delay and the best efficiency. As a result the proposed FA cells have the best PDP in different conditions.

Figure 4 shows PDP diagrams at 250 MHz and 500 MHz frequencies. It can be concluded from the charts that the PDP of the proposed designs are less than the previous designs.

Figure 5 shows the waveforms of the proposed design at 0.5 v supply voltage. This design performs very well at low supply voltages and high frequencies and has full swing outputs.

CONCLUSION

This study has proposed a novel high-speed and low-voltage CNFET-based Full Adder circuit based on carbon Nano-tube technology and transfer gate to achieve the least delay and the most efficiency .We did the simulation of above full adder cell in different term and compare it with silicon and carbon nano-tube technology of full adder circuits is better than other that circuits in delay and efficiency. The suitable capability in outlets and low power consumption in comparison of former CNFET adder circuits are the advantages of this circuit. All knots of this circuit are in complete sway voltage that it gives the circuit a high assurance.

REFERENCES

Bok Kim, Y., Y.B. Kim and F. Lombardi, 2009. Novel design methodology to optimize the speed and power of the CNTFET circuits. Proceeding of IEEE International Midwest Symposium on Circuits and Systems, pp: 1130-1133.

Chang, C.H., M. Zhang and J. Gu, 2003. A novel low power low voltage full adder cell. 3rd International Symposium on Image and Signal Processing and Analysis (ISPA), 1: 454-458.

Chen, Z., 2004. Nanotube for nanoelectronics. Enc. Nanosci. Nanotechnol., 7: 919-924.

Deng, J., 2007. Device modeling and circuit performance evaluation for nanoscale devices: Silicon technology beyond 45 nm node Ancarbon nanotube field effect transistors. Ph.D. Thesis, Stanford University.

Goel, S., A. Kumar and M.A. Bayoumi, 2006. Design of robust, energy-efficient full adders for deep-sub micrometer design using hybrid-CMOS logic style. IEEE T. VL. SI. Syst., 14(12): 1309-1321.

Ijiima, S., 1991. Helical microtubules of graphitic carbon. Nature, 354: 56-58.

Junming, L., S. Yan, L. Zhenghui and W. Ling, 2001. A novel 10-transistor low-power high-speed full Adder cell: Solid-State and integrated-circuit technology. Proceedings of 6th International Conference on IEEE, 2: 1155-1158.

Navi, K. and O. Kavehei, 2008. Low-power and high performance 1-Bit CMOS full Adder cell. J. Comput., 3(2).

Navi, K., A. Momeni, F. Sharifi and P. Keshavarzian, 2009. Two novel ultra high speed carbon nanotube full Adder cells. IEICE Electron., 6(19): 1395-1401.

Navi, K., M. Rashtian, A. Khatir, P. Keshavarzian and O. Hashemipour, 2010a. High speed capacitor-inverter based carbon nanotube full adder. Nanoscale Res. Lett., 5: 859-862.

Navi, K., R. Sharifi Rad, M.H. Moaiyeri, A. Momeni, 2010b. A low-voltage and energy-efficient full Adder cell based on carbon nanotube technology. Nanomicro Lett., 2(2): 114-120.

Paul, B.C., S. Fujita, M. Okajima and T. Lee, 2006. Modeling and analysis of circuit performance of ballistic CNFET. Matter. Res. Soc. Proc., 1018: 717-722.

Raychowdhury, A. and K. Roy, 2004. A novel multiple-valued logic design using ballistic carbon nanotube FETs. Proceedings of the 34th International Symposium on Multiple-Valued Logic, pp: 14-19.

Raychowdhury, A. and K. Roy, 2007. Carbon nanotube electronics: Design of high-performance and low-power digital circuits. IEEE T. Circuit. Syst., 54(11): 2391-2401.

Tans, S.J., R.M. Verschueren and C. Dekker, 1998. Room temperature transistor based on a single carbon nanotube. Nature, 393: 49-52.

Weste, N. and K. Eshraghian, 1993. Principles of CMOS VLSI Design: A System Perspective. AddisonWesley, Reading, MA.

Zimmermann, R. and W. Fichtner, 1997. Low-power logic styles: CMOS versus pass transistor logic. IEEE J. Solid-State Circuits, 32: 1079-1090.