Research Journal of Applied Sciences, Engineering and Technology 5(18): 4493-4498, 2013
ISSN: 2040-7459; e-ISSN: 2040-7467

Submitted: September 07, 2012 Accepted: October 25, 2012 Published: May 05, 2013

ARM Core Unit Design of a Remote Video Monitoring System

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Abstract: In this study, we have a analysis of the ARM core unit design of a remote video monitoring system. An important aspect of a remote video monitoring system is that the image information stored in the monitoring system is transmitted to a remote PC through the GSM/GPRS network. There into the application of the ARM core unit is one part of the design of the entire remote video monitoring system. An ARM core unit is designed based on ARM architecture and ARM chips. It includes hardware and software design. Practice shows high stability and reliability of the design.

Keywords: ARM, embedded system, JTAG, remote video monitoring system

INTRODUCTION

Remote monitoring system is the product of the combination of computer technology, communications technology and control technology. Computer hardware and software system which can achieve remote monitoring is called Remote Monitoring System. An important aspect in achieving a remote video monitoring system is the ARM core unit design (Peng, 2010). This design is based on ARM architecture and ARM chips. It meets the following specifications:

- The operating voltage is 5V; operating current is less than 200mA
- Have Universal Serial Interfaces; the number of interfaces is greater than 3
- Have RJ45 network interfaces
- Have a SD card interface
- Have USB interface terminals
- Be able to run the μC/OS-II operating system

THE SELECTION OF THE ARM MICROPROCESSOR

The microprocessor is the central part to achieve monitoring terminals. It is responsible for controlling and coordinating each module. Therefore, the selection of the microprocessor is crucial.

In this design, monitoring points of transformer system are scattered and conditions are poor, so it has strict requirements and restrictions on the equipment size and the power consumption. It even might not have reliable power. It requires using solar energy. Therefore a powerful embedded microprocessor which has small size, low power consumption and high reliability is selected (Zhou, 2003).

ARM7TDMI is most suitable for cost-sensitive products. It is a 32-bit embedded RISC processor which is currently used more widely. Considering the system performance, power consumption, price, difficulty of development, technical support and other factors we make sure that the ARM7TDMI applies to our development program.

The design is to develop a set of remote video monitoring system based on the embedded network communication technology. The following factors need to be considered in the selection process of the embedded processor (Wu, 2004; Wang, 2002): running speed, powerful interfaces, low power consumption and convenient debugging.

According to the actual need of the development platform, the product of NXP's LPC2378 chip is selected.

THE HARDWARE DESIGN OF THE SYSTEM

The hardware design part of the system is based on the LPC2378. It includes the power supply circuit design, the clock circuit design, the choice of the reset circuit, the extension of the serial interface and JTAG circuit design.

- **Overall system design:** The main block diagram of the overall design of the system is shown in Fig. 1. The CPU of the system uses NXP's LPC2378 chip. It is a microcontroller based on the ARM7TDMI-S CPU. It is a 144-pin package. Through the on-chip PLL it can achieve maximum CPU operating frequency to 60MHz. It has extremely low power consumption. GPIO that can be used is up to 76-112. It provides more than one serial interface in which there are two SPI interfaces. LPC2378 is the core of the system controller.
- **The power circuit design:** According to the need of the LPC2378 supply characteristics, the LM1117-3.3 is added in the power supply circuit. The LM1117 is a series of linear regulator LDO power chip. It can limit the current output to

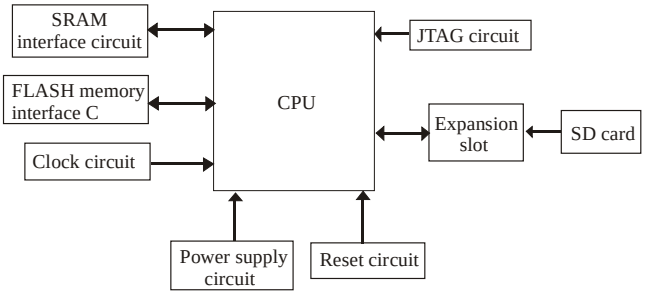

Fig. 1: The main structure diagram

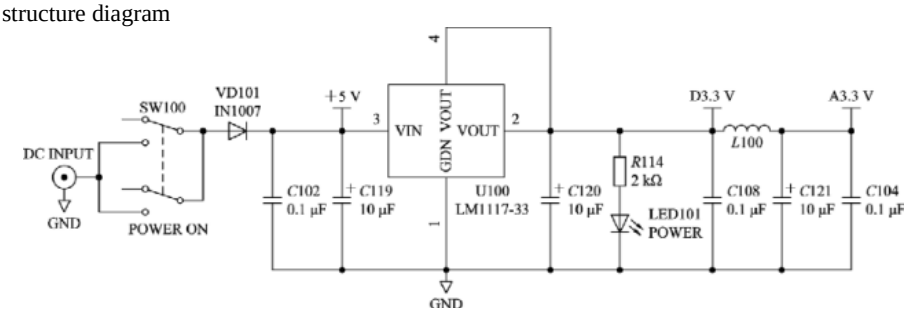

Fig. 2: The power supply circuit

- to 800 mA. In it there is a zener balance energy band. It can ensure that its output voltage error is within 1%.

5V power supply is in the LM1117. Adjusted 3.3V power supply directly drives the digital part of the board. On power a light-emitting diode lights. It shows that the 3.3V power supply which is connected to the circuit is effective. 0.1uF decoupling capacitor is connected between the power supply pin and ground in all valid devices. Digital power and analog voltage are separated by the inductance. The analog voltage section also sets the filter capacitor to absorb the high-frequency interference brought about by the digital power supply. The power supply circuit is shown in Fig. 2.

- **The clock circuit:** The operating frequency range of the integrated oscillator and external crystal in the LPC 2378 chip is from 1 to 30 MHz. The operating frequency range of the external oscillator is up to 50 MHz. In it a 12 MHz crystal is used. It can provide tens of MHz CPU operating frequency to the system. PLL settling time is 100 μs. The real-time clock uses a standard 32.768 kHz clock crystal. The clock circuit is shown in Fig. 3.
- **The reset circuit design:** The reset signal is used to start or restart the MPU/MCU, orders it to enter or return to a predictable cycle program and executes sequentially. Once the MPU/MCU is in an unknown state, for example, the program is "running out" or enters an infinite loop; the system needs to be reset. The reset circuit of the system is shown in Fig. 4. When in power +3.3V power supply charges the capacitor C215 through R200 and makes the RST signal temporarily at a low. With the C215 to be charged constantly the RST

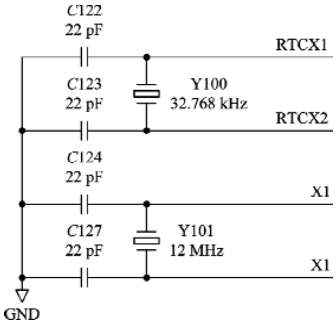

Fig. 3: The clock circuit

signal goes high after a certain time. Thus it forms a negative pulse to make the CPU reset.

In addition, by combining the reset circuit and ISP functions the circuit interface function of automatic program downloading is designed. The process of the automatic program downloading is as follows. The CPU reset is controlled by the DTR signal of the serial port. In the CPU reset period, the level of P2.10 is controlled by the RST signal of the serial port so as to control whether the CPU enters the ISP state. The DTR signal and the RST signal control the reset signal and P 2.10 through the transistor. As shown in Fig. 4, when the DTR or RST is high the transistor turns on. Thereby it controls the level of the RST and P 2.10. The jumper JP 200 makes automatic program downloading enabling control. If do not need the automatic downloading function we can remove the jumper in order to prevent the outside interference on the CPU.

- **The communication serial interface circuit:** The LPC 2378 has two asynchronous serial controllers

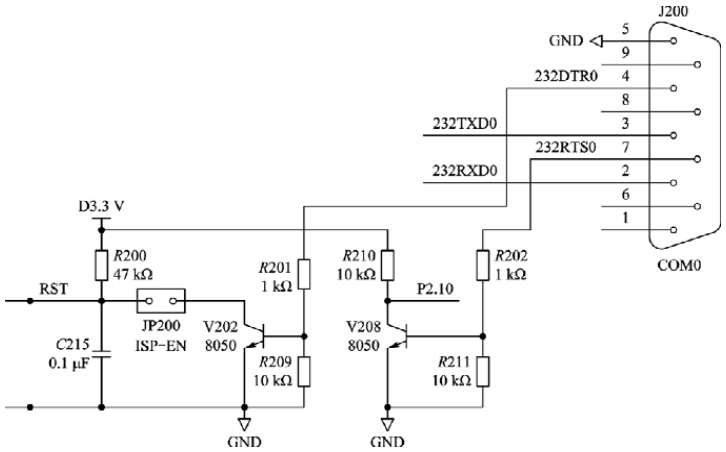

Fig. 4: The reset circuit

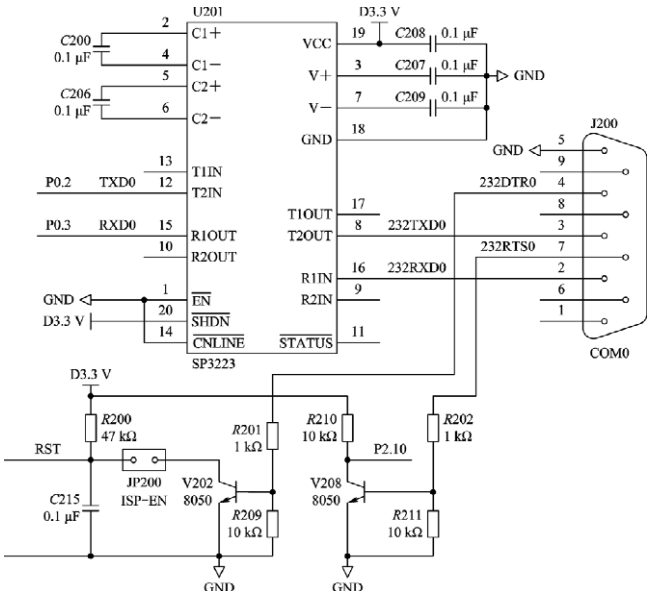

Fig. 5: The serial port 0 interface circuit

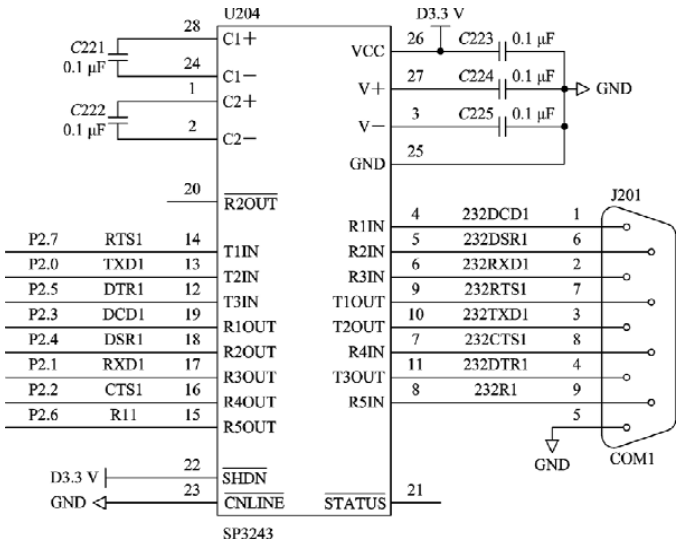

Fig. 6: The serial port 1 interface circuit

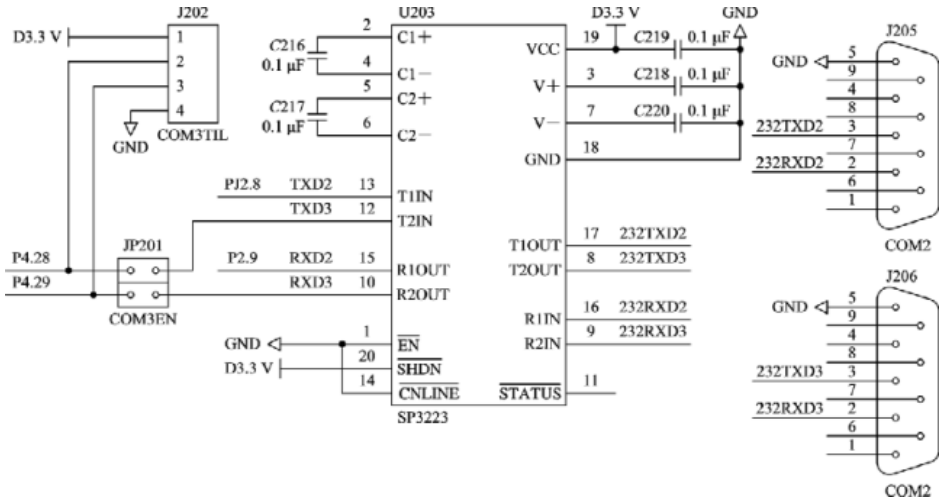

Fig. 7: The serial port 2 and 3 interface circuit

which are UART 0 and UART 1. The clock can be generated by the internal clock generator or provided by an external clock. Because the LPC 2378 is a 3.3V system it is completely different with the level signal that is defined by the RS-232 standard. Therefore, the communication between the two must go through the conversion of the signal level. The level conversion of the system uses the SP 3223E/3243E. It is a 3V operating voltage RS-232 converter chip. In addition the UART 1 of the LPC 23xx series of ARM7 microprocessors has the full MODEM interface. So the 8-way RS 232 converter chip SP3223E/3243E is used.

The design extends the four serial circuits. The serial port 0 is used for the ISP automatically downloading and VT 100 terminal debugging. The serial port 1 has a complete handshake, can be used for communication with MODEM and can extend the remote communication capability of the system. The serial port 2 uses a simple 3-wire way, shares an interface chip SP 3223 and can be used for the communication with the camera module. The serial port 3 can be used for the communication with the GPRS module. The four serial interface circuits are shown in Fig. 5 to 7.

- **The JTAG circuit design:** JTAG (Joint Test Action Group) is an international standard test protocol. It is mainly used for chip internal test, system simulation and debugging (Zhou, 2005; Wei, 2011). JTAG technology is an embedded debugging technique. Inside the chip it packages a special test circuit TAP (Test Access Port). It uses the dedicated JTAG test tools to test the internal nodes (Li and He, 2011; Ji, 2007). At present, the most complex devices support the JTAG protocol, such as the ARM, DSP, FPGA devices, etc. The standard JTAG interface is 4-wire: TMS, TCK, TDI, TDO. They are test mode select, test clock, test data input and test data output (Shi, 2008).

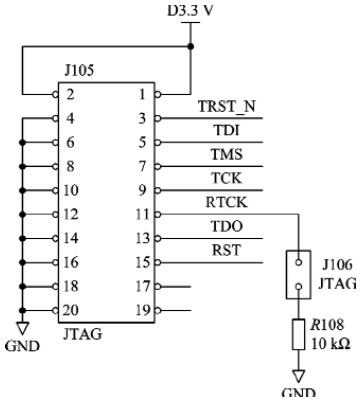

Fig. 8: The JTAG interface circuit

Through the JTAG interface all the internal parts of the chip can be accessed, so it is a simple and efficient means of developing and debugging embedded systems. At present there are two standards to connect the JTAG interface: 14 pin connector and 20 pin connector. This design uses a 20-pin JTAG interface. The system's JTAG interface circuit is shown in Fig 8.

- **The network communication circuit design:** The network portion connected to the CPU selects the chip STE 100 P. It is equivalent to the functions of the PHY. After that the network transformers are converted to the interface level and leads to the network interface. The network communication circuit is shown in Fig. 9.

THE SOFTWARE DESIGN OF THE SYSTEM

After the hardware platform and the LPC 2378 processor which is based on ARM7TDMI-S are analyzed, the μC/OS-II embedded operating system is

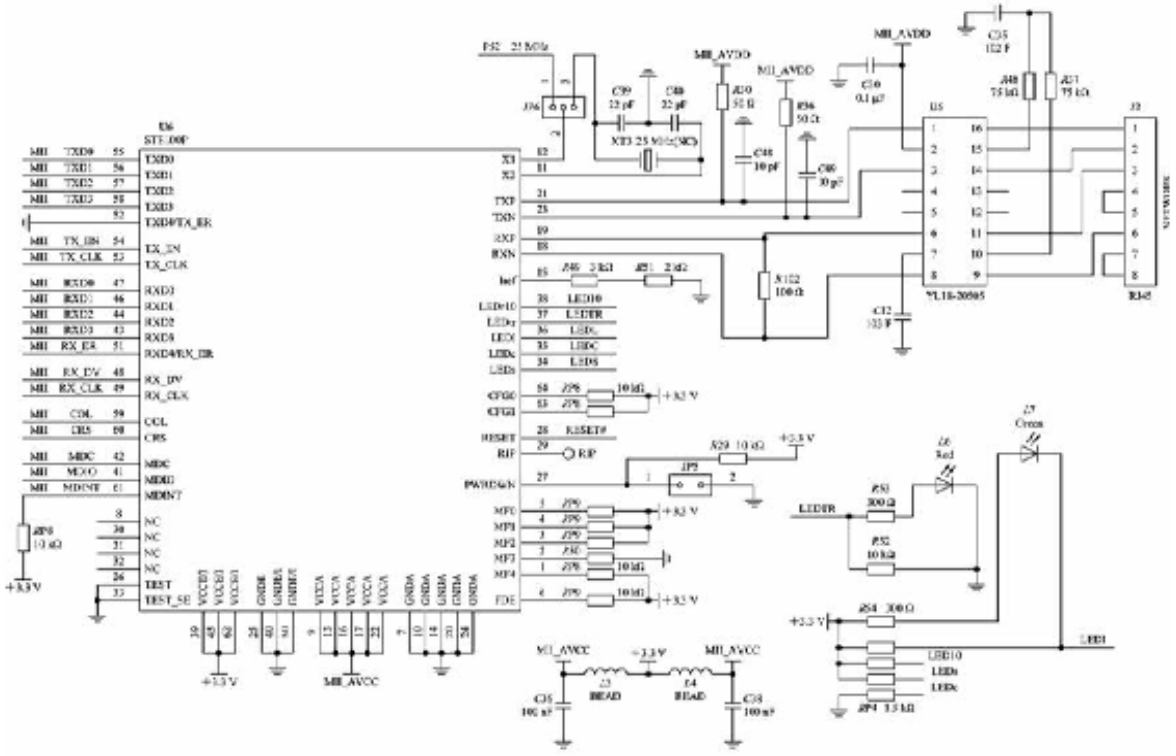

Fig. 9: The network communication circuit

chosen. It has a small kernel, is easy to cut and has good portability.

- **Conditions of transplanting µC/OS-ii and the main transplantation work:** The purpose of the transplantation of an embedded operating system is to make the operating system be able to run on a microprocessor or microcontroller. Most of the µC/OS-II codes are written in C language. But it still needs to use assembly language to write some codes associated with the processor. These processor-related codes are a prerequisite for running the real-time multitasking operating system and are also an important part of the embedded operating system migration.
  Transplantation of µC/OS-II in the LPC2378 builds embedded development platform of the entire system and on this platform we continue the development of the API interface. Finally, it is the preparation of the application software. The levels of development of the whole system have five which are underlying hardware design, transplanting the µC/ OS-II, configuring the µC/ OS-II, the API interface development and the application software design.

- **The startup code of the LPC23xx:** The startup code is a piece of code which is executed after the chip reset and before entering the main () function of C language. It is mainly to provide basic operating environment for running the C language program. It includes the exception vector, the CPU mode stack set, the interface between the IRQ and C language, initializing the system clock, the initialization memory acceleration module and the prohibition of related interrupt etc.
- **Transplantation of µC/OS-II:** Transplantation of µC/OS-II includes the following content: rewriting the OS_CPU.H file, rewriting the OS_CPU_A.S file and rewriting the OS_CPU_C.C file.
- **µC/OS-II transplantation test:** Testing a µC/OS-II real-time kernel is not complicated, that is to make the real-time kernel to run up in their own target board. In the beginning some simple tasks and clock interrupt tasks can be run. If debugging is successful applications can be added in the above. The general starting and running process of embedded systems is as follows:

- The system hardware initialization
- The operating system initialization
- Creating an operating system task
- Clock initialization of the operating system
- Starting the system hardware
- Starting multitasking of the operating system

After the above work is completed the CPU control is put to the operating system.

We can create three tasks. Task A is to make Led0 flash once every 1 second and the priority of the allocation is 10. Task B is that Uart0 is output to "Uart0 OK" every 2 sec and the priority of the allocation is 20. Task C is that Uart1 is output to "Uart1 OK" every 3 sec and the priority of the allocation is 30. Program running output is in line with the set value. And the above procedure is used to do 24 h of test for the stability of the operating system kernel. Test results prove the stability of the operation and the reliability of the transplantation.

CONCLUSION

In engineering applications, the ARM core unit design of the remote video monitoring system is strong project engineering. It has a very high demand to many aspects of engineering practice and is a very good reference for other types of engineering problems. The ARM core unit of the remote video monitoring system is designed in the study. It includes hardware and software. The design has a certain practical significance.

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