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Implementation of Camera Link Interface on Virtex-5 FPGA

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Abstract: Camera link interface is a standard interface commonly used in current industrial camera and image acquisition card and it is usually realized by special chips. The embedded image processing platform has the FPGA chips, if the camera link interface can be implemented on the FPGA chips, the circuit design will be simplified and the system integration can be improved.

Keywords: Camera link, channel link, frame grabber, FPGA

INTRODUCTION

In the current industrial applications, Camera Link interface is usually implemented by adopting the special-purpose chips, it needs at least four chips, a power supply and several resistance capacitances, it also needs circuit board area and cost. When the Camera Link data is transmitted to the FPGA, if the Camera Link interface is achieved by a small number of FPGA logic resources, then the system integration, reliability and flexibility can be improved and the system cost can reduced. If the interface can be realized on FPGA (Zhu *et al*., 2011), it can not only make image acquisition, but also can be used in two FPGA chips (Shu-Chang *et al*., 2011) which have no special high speed serial interface, to realize high speed data transmission with less amount of pins, it will has very realistic significance (Xie and Cheng-Jiang, 2010). To achieve this purpose, the Camera Link interface definition and the related resources of FPGA will be shown respectively as follow.

Camera Link interface is from Channel Link interface, before introducing Camera Link, LVDS and Channel Link will be introduced in detail.

LVDS is short for Low-voltage differential signaling, the Signal pendulum rate is 350 mv and the model is shown in Fig. 1:

LVDS signal voltage pendulum rate is very low; therefore rise or fall time is so short that it can achieve high speed. Driver changes single-ended task signal IN into Receiver. On one side of the Receiver have 100 Ω terminal resistances in parallel, Receiver takes a sample from voltage signal across the resistance voltage and it recovers as single-ended signal out.

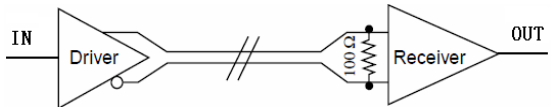

Fig. 1: LVDS model

Channel-Link by National Semiconductor whose physical layer is based on the LVDS and at first it is regarded as a solution in the flat display field, the technology soon developed as a common mode of data transmission. The model as shown in Fig. 2:

Sending end and receiving end all have 28 single end parallel data signal and 1 road single-ended clock signal, the clock signal is temporarily called adjoint clock. The serializer of sending end which is driven by clock signal makes 28 single-ended signals as 7:1 string change into 4 road single-ended serial data, then it gets through the 5 groups of LVDS signal Driver with 1 road adjoint clock to drives Receiver. Receiver reverts LVDS signal to 4 road single-ended serial data signals and 1 road adjoint clock. With adjoint clock driving, it deserializes 4 road serial data as 1:7 and then reverts to 28 parallel signals.

The relationship between adjoint clock and distribution of Channel Link interface parallel data in serial data stream is shown in Fig. 3. In adjoint distributed architecture based on agent will coexist in the domain of design robot. No matter what kind of clock period, every road string data stream transports 7-bit of 28-bit parallel. Serial data rate is about seven times of adjoint clock frequency, accurately deserializing the serializable data requires taking data

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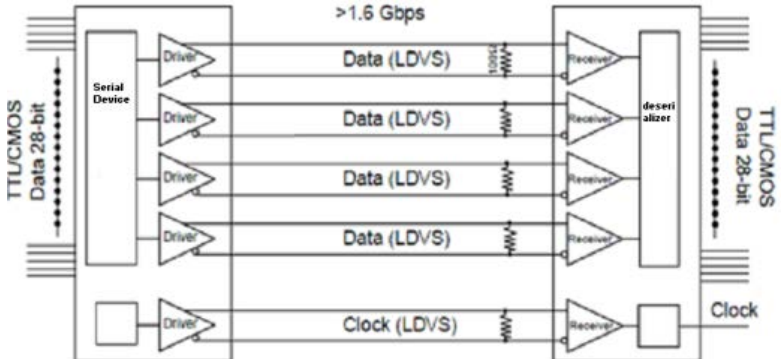

Fig. 2: Channel-Link model

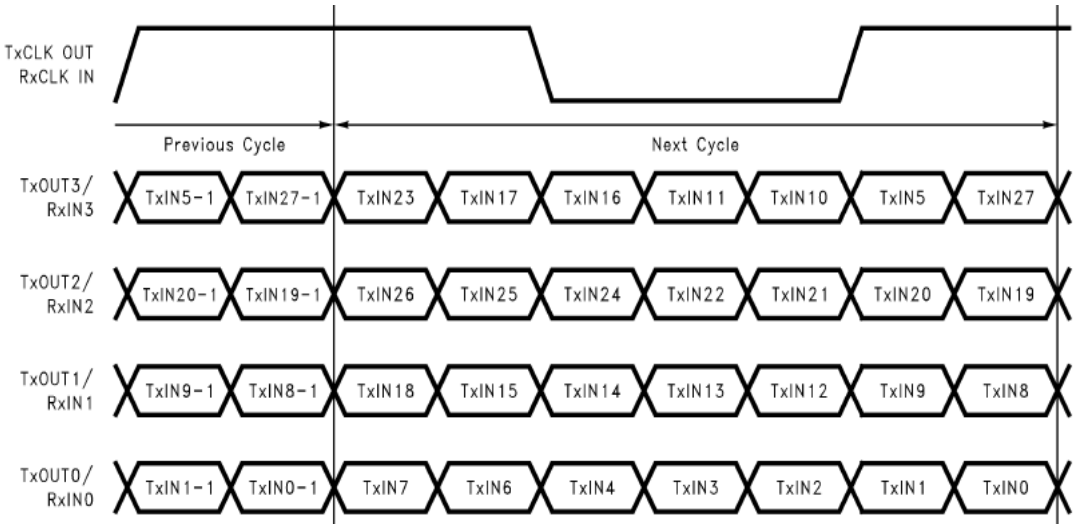

Fig. 3: Adjoint clock relation of channel link

sampling with seven times of adjoint clock frequency, sampling edge should aim at each data effective window center position of serial data flow, so as to ensure the highest accuracy, the interior of deserializer has phase lock loop PLL, the frequency produced by PLL clock is 7 times of adjoint clock frequency.

Camera Link interface composition:

Camera link interface has two ports: Camera and Frame Grabber (Xiaonan *et al*., 2010). The former is a camera end; the latter is image acquisition end. As shown in Fig. 4, Camera Link interface structure is: 1 to 3 Channel Link interfaces, the direction is from Camera to Frame Grabber, it is used for the image data transmission; a four channel-camera-control interface CC1 ~ CC4, the direction is from Frame Grabbe to Camera, it is usually used for Camera exposure trigger control (He *et al.*, 2009). A two channel asynchronous serial interface: SerTFG (Serial to Frame Grabber) and SerTC (Serial to Camera). Frame Grabber configures Camera through the SerTC, Camera sends register value to Frame Grabber through the SerTFG. All the interfaces are physically based on LVDS signal transmission. When the Channel Link number configuration of Camera Link interface is 1, 2 and 3, they are respectively called Base and Media and Full mode. Three kinds of model use the same set of camera control interface and serial communication interface.

Camera Link interface only has Channel Link which involves serial parallel conversion (Haitao *et al.*, 2007), any other interface is ordinary unidirectional connection, therefore the key to realize the Camera Link interface on FPGA is to realize the Channel Link. And many current high-end FPGA chips internal have deserializer element, it is very suitable to implement the applications such as Camera Link, Camera Link interface is implemented with few resource in FPGA in order to enhance hardware system integrated level and flexibility. In the following parts, the study ill represent

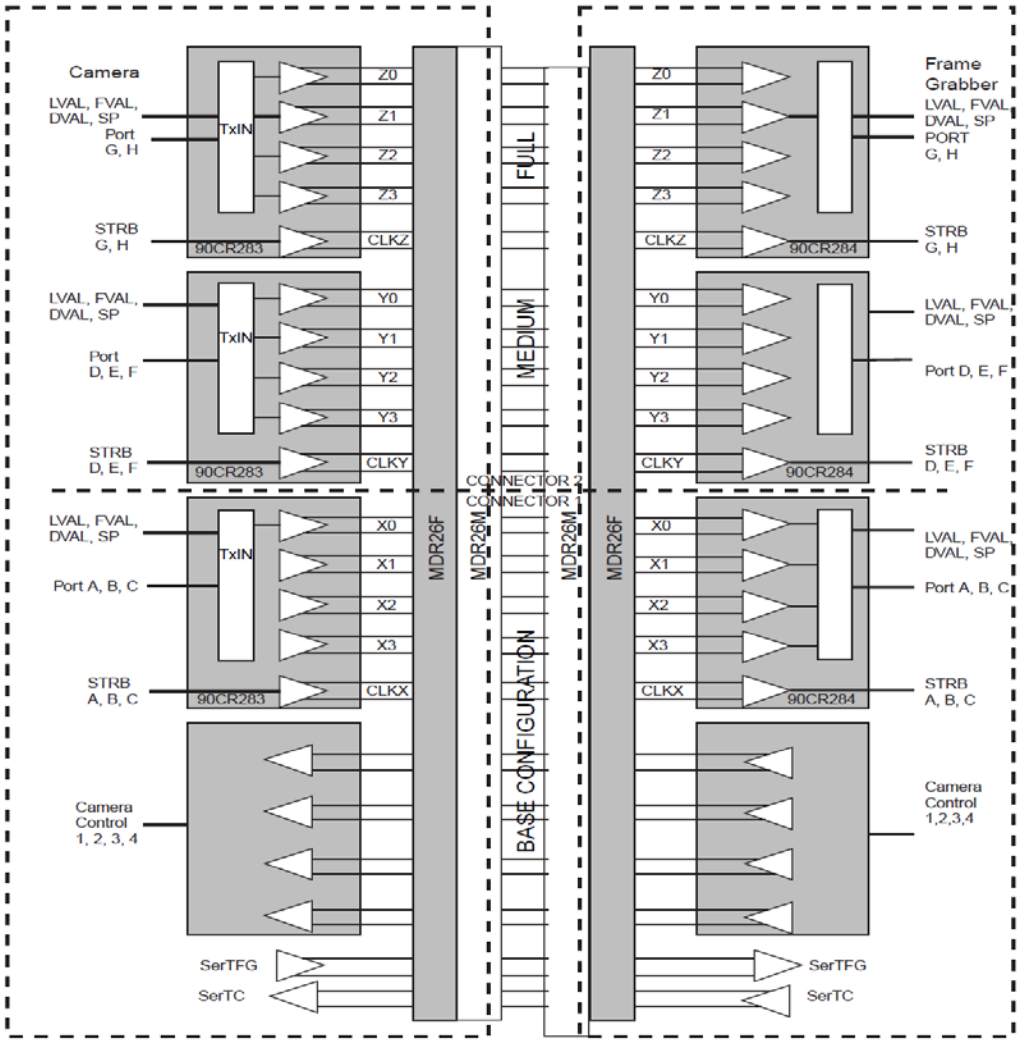

Fig. 4: Camera Link interface structure

how to implement Camera Link interface Frame Grabber end on Virtex-5 FPGA.

Virtex-5 FPGA: In Xilinx Company, to implement camera link interface frame grabber end on Virtex-5 FPGA (Wang and Wang, 2011) requires a PLL, IBUFDS/IBUFGDS, OBUFDS, ISERDES, IODELAY and IDELAYCTRL. In addition to PLL, the other parts are all belong to the Select IO.

Camera link interface implementation: Figure 5 shows the hardware design about implementation of Camera Link interface Frame Grabber end Base configuration.

Implementation: In Fig. 5, the dashed part is the deserializer design of Channel Link. The adjoint clock CLKX – P / CLKX - N and serial data signal RX0_P/RX0_N respectively converts to single end signal CLKX and RX0 through IBUFGDS and IBUFDS. The design idea is to use IODELAY adjust the serial data signal RX0 delay, in order to make RX0 data effective window center position take a sample for the sampling clock edge of alignment deserializer.

CLKX represents the input clock of PLL; the three out put way clock of PLL all pass global buffer processing. CLKOUT0 = 7*CLKX; CLKOUT1 = 200MHz; CLKOUT2 = CLKX. CLKOUT0 and CLKOUT2 keep edge alignment with CLKX. CLKOUT0 provides data sampling clock for two cascaded ISERDES port CLK. CLKOUT1 provides reference clock for IDELAYCTRL port REFCLK. CLKOUT2 provides control clock for ISERDES port CLKDIV and IODELAY port C and it also provides the data which latched ISERDES output for Fabric.

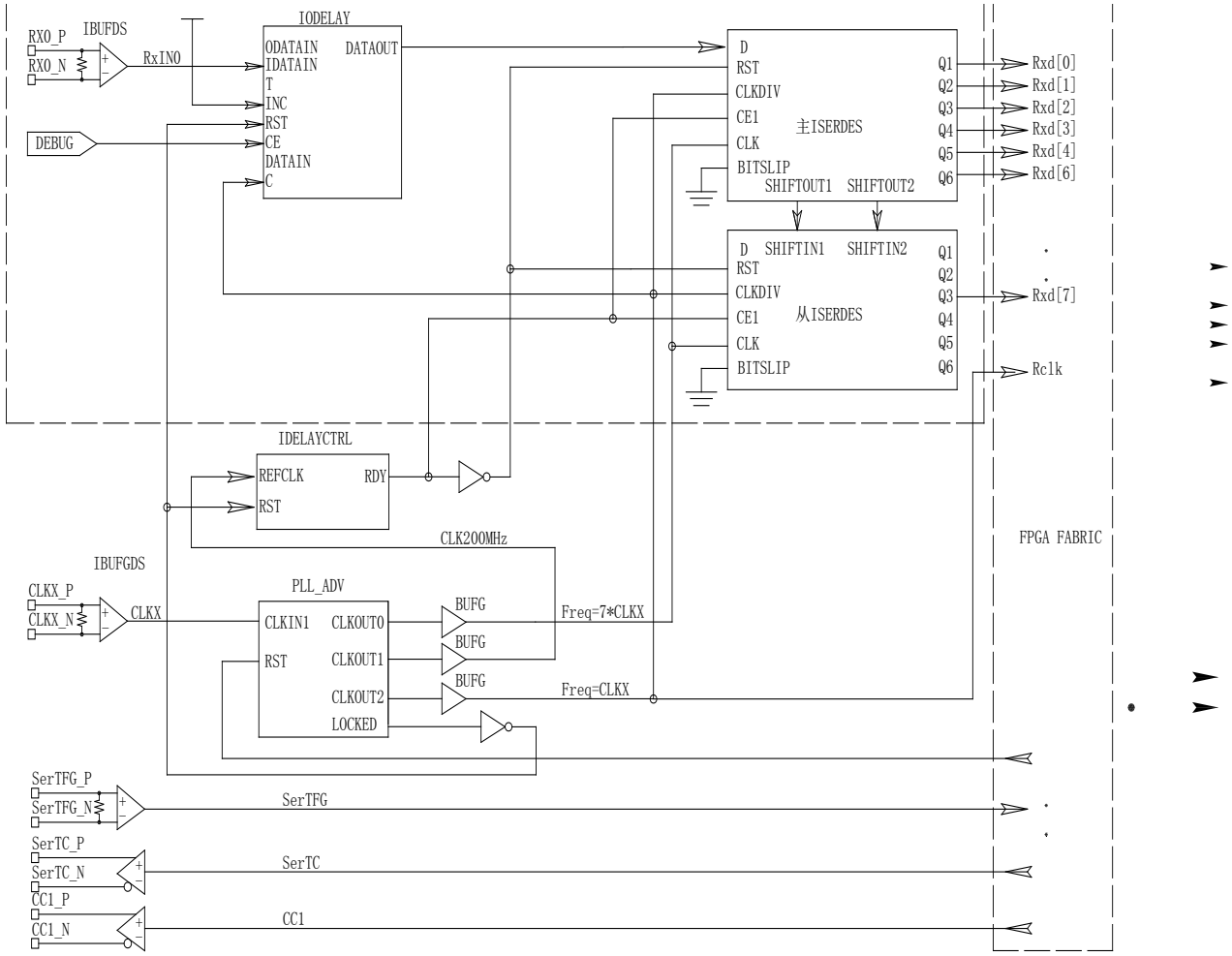

Fig. 5: Frame grabber end base configuration hardware

Reset signal is designed due to the principle direct correlation. The stability of PLL frequency is the foundation of the whole circuit operation, hence it's signal LOCKED is used to control IDELAYCTRL and IODELAY; The data which ISERDES receives is significant, only after calibrating IODELAY by IDELAYCTRL, therefore the reset signal of ISERDES is controlled by the signal RDY of IDELAYCTRL.

The configuration of IODELAY is input VARIABLE delay. RX0 as input signal source, goes from IODELAY delay to the data port D of the cascaded master ISERDES. IODELAY delay adjustment direction port INC joints high, control port C joints CLKOUT2, control clock port CE joints DEBUG signal。when CLKOUT2 is on the rising edge, each sampling that DEBUG is high, the delay increase a pat, when delay is 63 pat, if sampling that DEBUG is high, the delay back to 0 apt and rotate around. Through controlling the DEBUG signal to adjust the delay of RX0 signal, in order to meet the requirements. Initial delay is set to 0 beat.

Test: When commissioning, it needs building a debugging environment: Using a Camera end Camera Link interface to send specific Channel Link data; Connecting the camera end camera link interface to the Virtex-5 FPGA circuit with cable, Camera end serializer clock is 60 MHZ and it makes the parallel data serialized, which Channel Link sends to FPGA.

First debug serial channel 0 of Channel Link. In order to eliminate interference, the parallel transmission data of channel 0 is 1. According to the parallel data distribution, the Camera parallel data is: 28’b0000-0000-0000-0000-0000-0000-0001, the ISERDES output of corresponding channel 0 of FPGA should be 7 'b000-0001. After the FPGA configuration, the PLL should be reset, waiting for each element end reset and then adjust

IODELAY delay. The DEBUG is controlled in Fig. 5, the cycle of the positive impulse is in 1/2 ~ 1 CLKOUT2 width, IODELAY delay will increase 1 pat, when one pulse is coming. When the delay value is improper, the parallel data which deserialized from ISERDES is not equal to 7 'b000-0001, even sometimes data which contains two bits is equal to 1. To keep inputting pulse to DEBUG, when input N pulses , the data is 7 'b000-0001, continue to input pulse until the data is not equal to 7' b000-0001, at present the total number of input pulse is to M. The data effective window width of the channel ISERDES is M-N, the center position of window is (M +N-1)/2, three other channel window center position are measured in turn based on this method.

When Control signals, serial signal test, FPGA Fabric drives CC1 ~ CC4, SerTC, Camera end and the corresponding signal is received, Camera end drives SerTFG, FPGA Fabric end and the corresponding signal is received, the two kinds of interface are finish debugged.

After debugging, in the program the IODELAY delay configuration is fixed, the value is the integer part of (M + N-1)/2. Hence, Camera Link interface is implemented on Virtex-5 FPGA. The actual test of the design is divided into two stages. At first ,testing error rate, The Camera end output data is divided into three sections: 0~7, 8~15, 16~28, the repetitive data with 0~255 circulation is input into each section with 60 MHz, if the receiving data of Camera Link is flawed, it will emit trigger signal. After several hours testing, data has been normal and it doesn't happen to trigger signal. Then the design will be integrated into the FPGA complete design, to realize the image normal collection in the actual equipment.

CONCLUSION

Debugging results show that the principle of implementing camera link interface design on FPGA is feasible, the design has passed the error rate test and it can be applied in practice. After the application, the hardware circuit design can be simplified. As a tool of platform, this design can be directly transplanted between the Virtex-5 FPGA chips.

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