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Interference Rejection in UWB LNA using Front-End Triode MOSFET

H. Rezaei, E. Abiri, H. Shahraki and M.R. Salehi
Department of Electrical and Electronics Engineering, Shiraz University of Technology, Shiraz, Iran

Abstract: In this study, an Ultra Wide Band Low Noise Amplifier (UWB LNA) with new input stage for interference rejection is presented. In this scheme, a common gate front end MOS device in triode mode is used to reject in-band and out-band interferences. Furthermore, advantage of weak inversion mode of MOS device is used. While this stage has no DC power consumption, it is possible to easily reject in band and out band interferences with 12.5 and 9.2 dB, respectively. In order to increase power gain of the circuit two stages are added as an amplifier to the circuit. Also, in order to improve the Noise Figure (NF) and bandwidth of the circuit, the advantages of thermal noise cancellation technique in the second stage and the series-peaking method in the output buffer are used. The circuit is design in 0.18 μm technology. Simulation results show peak gain of 17.6 dB in the low band (3.1-4.75 GHz) and 15.6 dB in the high band (6.1-10.6 GHz). Minimum NF in mentioned frequency band is 3 and 2.3 dB, respectively. Hence, this circuit rejects in band and out band interferences 15.6 and 11.5 dB, respectively, while UWB LNA consumes 16 mW DC power from 1.8 V. The s_{11} is less than -9.6 dB over entire bandwidth since worst value of IIP3 over entire bandwidth is -14 dBm which occurs at 10.6 GHz.

Keywords: Interference rejection, Low Noise Amplifier (LNA), Ultra Wideband (UWB)

INTRODUCTION

Ultra wide band standard was proposed by federal communication committee (FCC, 2002) in frequency range of 3.1-10.6 GHz. Due to the wide frequency band, UWB systems are capable of increasing the transmission rate up to 450 Mbps. Therefore, UWB systems are widely used for numerous applications in the form of WPAN and short- range wireless communications (Safarian and Heydari, 2008; Nikookar and Prasad, 2009). However, the performance of these systems can be vitiated by the presence of interferer sources which can seriously affect UWB receivers. Currently, there are two major categories of signals mainly caused by WLAN systems which work in UWB frequency range. These signals work under IEEE 802.11a standard and IEEE 802.11 b/g standard. These kinds of interferences are called in-band and out-band interferences, due to occupying the frequency band of 5-6 GHz and 2.4-2.48 GHz, respectively. The high power interference signal caused by these systems may lead the UWB LNA receivers to saturation and consequently degrading the sensitivity of the system. Thus, removing this type of interference is considered as a crucial issue in designing RF transceivers. As it can be observed in Fig. 1, the optimum region for UWB LNA systems is in the range of 3.1-4.75 GHz and 6.1-10.6 GHz.

Recently, many UWB LNA have been proposed to improve the system performance of UWB transceiver.

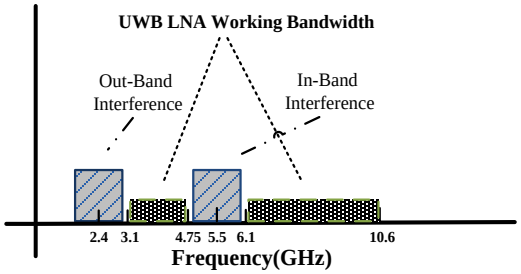
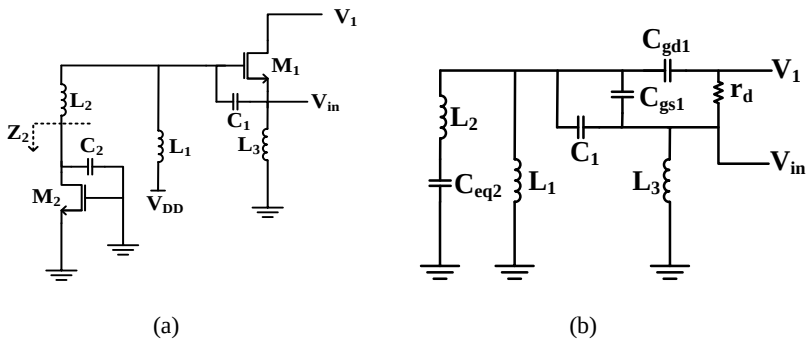


Fig. 1: Spectrum of UWB system with interferences

Gm-boosting (Li, 2004) and thermal noise cancellation for decreasing the noise figure (Bruccoleri *et al*., 2004), Distributed Amplifiers (DA) to achieve flat gain and wide bandwidth (Guan and Nguyen, 2006), bridged-shunt-series peaking technique for increasing the bandwidth and improving the matching in the output (Shekhar *et al.*, 2006). These generic methods improve the system performance, this is while and they are not capable of interference rejection. Hence, various methods have been proposed for interference rejection which most of them have been designed by using notch filters (Gao *et al.*, 2007; Reja *et al.*, 2011; Park *et al.*, 2010; Jui-Yi and Hwann-Kaeo, 2011; Liang *et al.*, 2010). These filters are able to be tuned over the rejected frequency. However, due to using an additional circuit for rejecting the considered frequency, these

Corresponding Author: H. Rezaei, Department of Electrical and Electronics Engineering, Shiraz University of Technology, Shiraz, Iran



(a) (b)

Fig. 2: (a) Schematic of proposed interference rejection circuit, (b) Equivalent circuit of proposed input stage

filters will cause an increase in power consumption and noise figure. In this study, the interferer signals in the input stage will be rejected in such a way that there will be no increase in the power consumption, no effect on noise figure. Also, powerful tuning over the considered frequency will be preserved. Here, advantages of weak inversion and triode working mode of MOS device will be used. The proposed input stage can be used in the form of common gate and common source. Since CG LNA, has better input reflection coefficient (Li, 2004), the proposed input stage has been used in this form. All simulations have been done by use of agilent ADS 2008A.

CIRCUIT DESIGN

The architecture of 3 stages LNA will be described in this section. Initially proposed input stage, CS LNA and output buffer with noise analysis will be described with more details.

Input stage: The proposed input stage is shown in Fig. 2a. In this circuit, inputs MOS device in triode mode (M_1) with L_1 and C_1 are used to reject out-band interference. This is while, combination of L_2 with C_2 and drain-gate capacitance of M_2 in weak inversion mode are used to reject in-band interference. Whereas M_1 is biased in triode region with $I_{d, M1} \approx 0$, power consumption of input stage is zero; also, drain-gate capacitance of M_2 causes mostly powerful in-band interference rejection. By using mentioned mode biases, g_{m1} and g_{m2} in Fig. 2a can be neglected. Hence, equivalent circuit of input stage can be considered as it shown in Fig. 2b.

In order to find rejected frequencies, input admittance of circuit can be calculated as (1), where $C' = C_{gs1}+C_1$, $C_{eq1} = C'+C_{gd1}$, $C_{eq2} = C_{gd2}+C_2$ and also $L_{eq1} = L_1+L_2$. Generally, it is difficult to find the exact rejected frequency from (1) because of the many circuit components. But, it is possible to simplify the equation through some approximations. Therefore, if $L_{eq1} \approx L_2$ is assumed, then, input admittance can be estimated as (2).

Equation (2) has two poles in its denominator which can be considered as two rejected frequencies. These frequencies are given by (3) and (4):

$$Y_{in} = L_3 S + \frac{r_d C' C_{eq2} C_{gd1} L_2 S^5 + C_{eq1} C_{eq2} L_1 L_2 S^4 + r_d C' \left(C_{gd1} L_1 + C_{eq2} L_{eq1}\right) S^3 + \left(C_{eq1} L_1 + C_{eq2} L_{eq1}\right) S^2 + r_d C' S + 1}{r_d \left(C_{eq1} C_{eq2} L_1 L_2 S^4 + \left(C_{eq1} L_1 + C_{eq2} L_{eq1}\right) S^2 + 1\right)} \quad (1)$$

$$Y_{in} = L_3 S + \frac{r_d C' C_{eq2} C_{gd1} L_2 S^5 + C_{eq1} C_{eq2} L_1 L_2 S^4 + r_d C' \left(C_{gd1} L_1 + C_{eq2} L_{eq1}\right) S^3 + \left(C_{eq1} L_1 + C_{eq2} L_{eq1}\right) S^2 + r_d C' S + 1}{r_d \left(C_{eq1} L_1 S^2 + 1\right)\left(C_{eq2} L_2 S^2 + 1\right)} \quad (2)$$

$$f_1 = \frac{1}{2\pi\sqrt{C_{eq1} L_1}} \quad (3)$$

$$f_2 = \frac{1}{2\pi\sqrt{C_{eq2} L_2}} \quad (4)$$

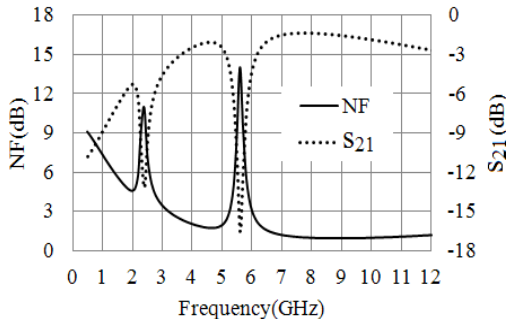


Fig. 3: The noise figure and s_{21} of proposed front end stage

Hence, we can reject out-band and in-band interferences by tuning f_1 and f_2 on 2.4 and 5.6 GHz, respectively. In this study, components values of front end LNA are C_1 = 684fF, C_2 = 143fF, W_1/L = 100 µm/0.18 µm, W_2/L = 100 µm/0.18 µm, L_1 = 4 nH with R_S = 4.2Ω, L_2 = 2.65 nH with R_S = 2.8Ω, L_3 = 1.7 nH with R_S = 6Ω which are fixed for the design in the following discussion. Simulated NF and gain of front end LNA are shown in Fig. 3. Consequently, the proposed CG-input stage rejects in band and out band interference 12.5 and 9.2 dB, respectively.

CS LNA with thermal noise cancelation technique: In the proposed front end LNA, M_1 provides no power gain due to bias in triode mode. Therefore, as shown in Fig. 4, two stages (M_3 and M_5) are added to the circuit in order to amplify the received signal. Furthermore, thermal noise cancelation technique is used to decrease noise figure of the circuit. This is done by means of M_4 which provide extra pass for signal pass from input to the output. The concept of noise cancellation can be extended as Bruccoleri *et al*. (2004). Also, M_5 forms output buffer based on series-peaking technique (Shekhar *et al.*, 2006; Hong and Gui-Can, 2008). Hence, through this technique, maximum Bandwidth Extension Ratio (BWER) can be obtained.

As shown in this figure, M_3 and M_4 make two signal paths from M_1 in this technique. C_Y and C_X are input parasitic capacitances of M_3 and M_4 at nodes Y and X, respectively. Since, noise current of M_1 ($I_{n,M1}$) flow out of node Y and into node X, therefore two obtained voltage noises are of different phases. These signals are collected with each other at node Z and cancel the noise contribution of M_1.

After cancelling the noise of M_1, the main sources of noise are M_3, M_4 and M_5. If input matching condition, $Y_{in} = 1/R_S$, is assumed, the noise factors contributed can be derived as:

$$F_{M3} = \frac{\gamma}{\alpha} \times \frac{g_{m3}}{\left[H(S)g_{m3} + g_{m4}\right]^2} \times \frac{4}{R_S} \tag{5}$$

$$F_{M4} == \frac{\gamma}{\alpha} \times \frac{g_{m4}}{\left[H(S)g_{m3} + g_{m4}\right]^2} \times \frac{4}{R_S} \tag{6}$$

$$F_{M5} = \frac{\gamma}{\alpha} \times \frac{S^2 C_{gs5}^2}{g_{m5}\left[H(S)g_{m3} + g_{m4}\right]^2} \times \frac{4}{R_S} \tag{7}$$

where,

$$H(S) = \frac{S^2 Z_1 r_d C' C_{gd1} + S Z_1 \left(C_{gd1} + C'\right) + 1}{S^2 Z_1 r_d \left(C' C'' + C_{gd1} C_{gs3}\right) + S\left(Z_1 \left(C' + C_{gd1}\right) + r_d C''\right) + 1} \tag{8}$$

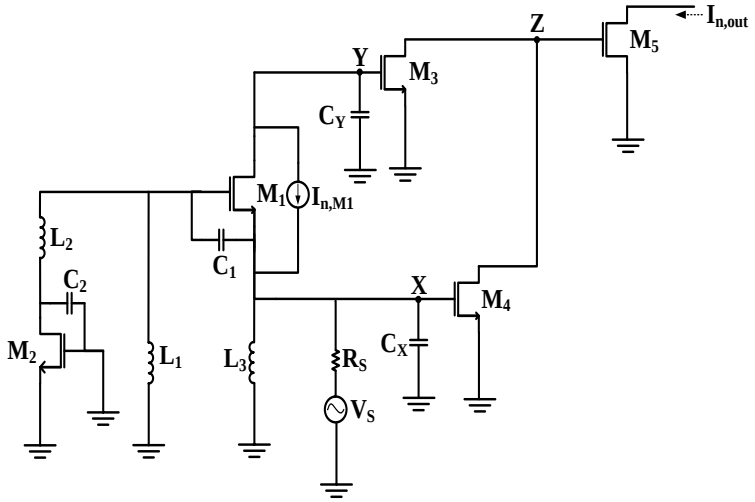


Fig. 4: Schematic of noise cancelation technique

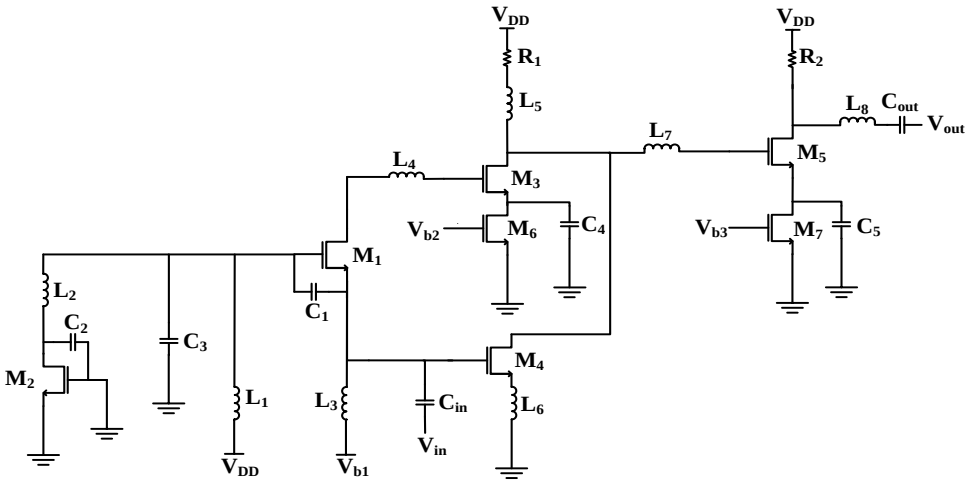


Fig. 5: Proposed UWB LNA

and γ is a noise parameter, $\alpha = g_m/g_{d0}$ at which g_{d0} is the channel conductance for V_{DS} = 0, also, $C'' = C_{gs3}+C_{gd1}$ and $Z_1 = L_1$ S $\left\|\left(L_2S + \frac{1}{C_{eq\,2}S}\right)\right.$.

Thus, total noise factor *F* can be approximately as:

$$F = 1 + F_{M3} + F_{M4} + F_{M5} = 1 + \frac{\gamma}{\alpha} \times \frac{4}{R_S} \times \frac{g_{m3} + g_{m4} + S^2 C_{gs5}^2 g_{m5}^{-1}}{\left[H(S) g_{m3} + g_{m4}\right]^2} \quad (9)$$

Considering (9), it is obvious that while g_{m3} and g_{m4} are optimized to cancel NF of M_1, total noise factor can be decreased. Furthermore, I_{M5} can be design to be as lower as possible to decrease total DC power consumption of the circuit. Hence $I_{d, M3}$ = 2.3 mA, $I_{d, M4}$ = 4 mA and $I_{d, M5}$ = 2.6 mA are selected.

Figure 5 shows proposed UWB LNA in which C_3 is added to improve input matching at low frequencies. On the other hand, in order to improve input matching of the circuit in low-band frequency $C_3 \approx 1/\omega_L R$ has been used. Here, ω_L is the lower cut-off frequency and *R* (50Ω) is the characteristic impedance at both ports. Resonating L_4 and L_7 with input parasitic capacitance of M_3 and M_5, respectively, improves input matching and gain at high frequencies. Also, bandwidth extension of LNA can be obtained via using inductance L_5 without any high Q requirements (Mohan *et al.*, 2000). Inductance L_8 forms the most powerful technique at the output which is called the series-peaking technique (Hong and Gui-Can, 2008). Hence, through this technique, maximum BWER can be obtained. Also, M_6 and M_7 with gate bias provide DC current path of M_3 and M_5, respectively. Furthermore, C_4 and C_5 provide the ac ground of circuit over working frequency bands.

Table 1: Circuit parameters of proposed UWB LNA

Element	Value	Element	Value
C_3	521 *fF*	V_{b2}	0.75 V
R_1	114.2 Ω	V_{b3}	0.64 V
R_2	152 Ω	L_4	1.9*nH* with R_s = 3.8Ω
W_3/L	100 *μm*/0.18 *μm*	L_5	2.6*nH* with R_s = 5.2Ω
W_4/L	100 *μm*/0.18 *μm*	L_6	0.5*nH* with R_s = 2.0Ω
W_5/L	100 *μm*/0.18 *μm*	L_7	0.8*nH* with R_s = 1.6Ω
V_{b1}	0.66V	L_8	0.85*nH* with R_s = 2Ω

SIMULATION RESULT

The simulation is carried out using agilent ADS 2008A software with TSMC 0.18 μm CMOS technology. First, second and third stage as an output buffer draw 8.9 mA from 1.8 V power supply. Consequently, total power consumption is 16 mW. The components values of front end LNA are the same as what we mentioned in input stage section. But, other circuit elements are chosen in order to optimize simulation results of proposed LNA. Table 1 summarizes other circuit elements of the UWB LNA. All inductors are spiral inductors on silicon with low required quality factor because of the use of large series resistances.

Figure 6a shows s_{21} of circuit which is 16.85 dB with ±0.75 dB fluctuation over 3.1-4.75 GHz and 15.15 dB with ±0.45 dB fluctuation over 6.1-10.6 GHz. Furthermore, gain of proposed LNA varies from highest amount of 17.6 dB in low frequency band to lowest amount of 14.7 dB in high frequency band which shows ±1.45 dB fluctuation over 3.1-10.6 GHz. Meanwhile, the gain of this circuit is 6.1 and 2.0 dB at 2.4 GHz and 5.6 GHz, respectively. Consequently, the LNA is able to reject in-band and out-band interferences at least with 15.2 dB and 11.5 dB, respectively, compare to

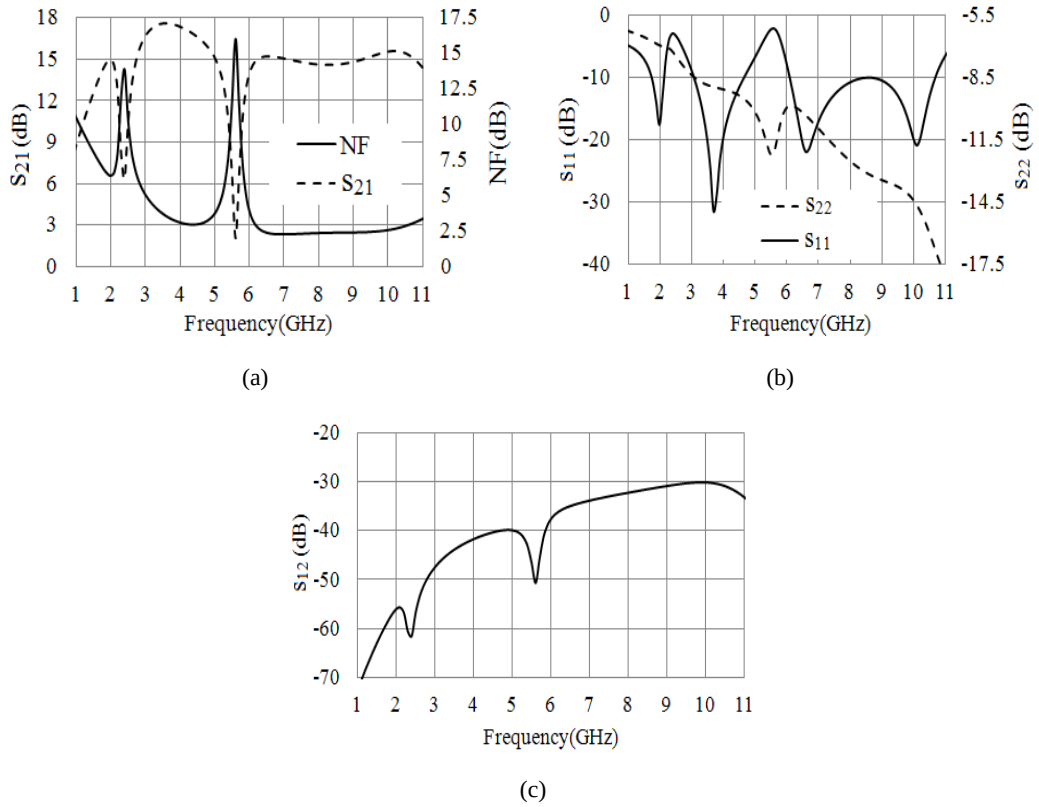


Fig. 6: (a) The NF and the gain, (b) The input and output reflection coefficient, (c) The reverse isulation (s_{12})

Table 2: Comparison between the proposed UWB LNA with other conventional techniques

	Result								
Ref.	BW (GHz)	$s_{21,MAX}$ (dB)(ave.)	In. Re. (dB)@(GHz)	NF_{min} (dB)(ave.)	s_{11} (dB)	P (mW)	IIP3 (dBm)	CMOS Tech.	Interference rejection
Gao *et al.* (2007)	3-10	20.3	19.6@5 GHz 12.8@2.4 GHz	4	<-10	24	-14.3 @7GHz	0.18 µm	Notch filter
Reja *et al.* (2011)	2-11	(16.5)	44.8@5.81 GHz	2.2	<-12	16.5	NA	90 nm	Tunable active inductors
Park *et al.* (2010)	3.1-10.6	13.2	8.2@5.2 GHz	4.5	<-9.5	23	-1.4	0.18 µm	Tunable notch filter
Lin and Chiou (2011)	1.2-9.5	14.7	35.7@5.8 GHz	5.3	<-10	16	-2.5	0.18 µm	Notch filter
Liang *et al.* (2010)	3-4.8	15	45@5.2 GHz 48@2.4 GHz	3.5	<-10	5*	NA	0.18 µm	Notch filter (active inductor)
This work	3.1-4.75 6.1-10.6	17.6 (17.1) 15.6 (15)	8.3@2.4 GHz 15.2@5.6 GHz	2.96 (3.45) 2.28 (2.48)	<-9.7	16	-10 @7 GHz	0.18 µm	Front end triode MOSFET

*: Only core LNA

maximum power gain. Also, this figure shows the simulated noise figure of LNA. Noise figure of proposed LNA varies from 2.96 to 4.7 dB in low frequency band and from 2.28 to 3.2 dB in high frequency band.

Figure 6b shows variation of input reflection coefficient. The worst value of s_{11} in the proposed LNA is -9.6 dB which occurred in 4.75 GHz. This is while input reflection coefficient has a better value over the rest of the frequency bands in both low and high band and is less than -10 dB. This figure also shows s_{22} of proposed UWB LNA. The worst amount of s_{22} is -8.52 dB which occurred at 3.1 GHz. As frequency increases, s_{22} in proposed LNA becomes better to the best values of -16.46 dB.

Figure 6c shows reverse isolation s_{12} of the proposed LNA which is less than -30 dB over the mentioned frequency bands. Another parameter which

should be considered is group delay since a large amount of it may distort the signal phase. In this circuit, variation of group delay ranges from 129.3 to 182 ps in low frequency band and from 73.65 to 176.1 ps in high frequency band which is acceptable. The stability factor of the proposed circuit over its working bandwidths is larger than 2.6, so proposed UWB LNA is always stable. By applying two tones test with 1 MHz spacing over UWB working frequency band, the simulated IIP3 for the LNA ranges from -10 to -14 dBm and from -11 to -13 dBm in low and high frequency band, respectively. Table 2 summarizes the performance of recently reported UWB LNA with interference rejection using CMOS technology.

CONCLUSION

In this study, a new technique for interference rejection in input stage of UWB LNA is proposed. Consequently, confident rejection of in-band and out-band interference is achieved. Whereas advantages of triode and weak inversion mode of MOSFET are used, robustness tuning and no DC power consumption are obtained by this technique. Therefore, a UWB LNA with this technique in its first stage is designed. Benefits of CS LNA as an amplifier with thermal noise cancelation technique are used in the second stage of UWB LNA. Finally, output buffer is implemented with series-peaking technique to extend the bandwidth of proposed UWB LNA.

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