

Mitigating Balanced and Unbalanced Voltage Sag Via Shunt-Connected Voltage Source Converter (VSC) by using Double Vector Controller

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Abstract: This study presents a shunt-Connected Voltage Source Converter (VSC) to mitigate balanced and unbalanced voltage sag and regulate the grid voltage at a fixed level by inserting required reactive power at the Point of Common Coupling (PCC). Moreover, an inner Vector Current-Controller (VCC) and outer voltage controller (VVC) are applied together to calculate the current references for the VCC. Furthermore, an inductor/capacitor/inductor (LCL) filter is replaced with the simple L-filter in between the VSC and the network and it is constructed to reduce the voltage sag. Likewise, to make up for the unbalanced dips, the positive and negative sequence components related to the grid voltage should be managed distinctly. The positive and negative sequence components related to the grid voltage should be managed distinctly. This is achieved through the application of two independent controllers for the two sequences with an identical cascade structure which has been explicated above. Simulation results designate proper functioning of the control system which has been proposed.

Keywords: Power quality, reactive power controller, voltage and current controller, voltage sag mitigation, voltage source converter

INTRODUCTION

In the recent decades, power quality problems especially voltage sag and harmonic distortion are known as one of the most significant topics among power system engineers (Hingorani, 1995; Di Perna *et al.*, 2003; Woodley *et al.*, 1999; Jung *et al.*, 2002). Therefore, the occurrence of these power quality events especially for those industries which are associated with information technology systems can be very harmful. Recently, state-of-the-art power electronic based compensators called 'Custom Power Devices (CPD)' have been developed to mitigate the negative effects of power quality problems (Hingorani, 1995). The Series-connected Voltage Source Convertors (VSC), also called Static Series Compensator (SSC) or Dynamic Voltage Restorer (DVR), can be categorized as a type of CPDs. These devices can be connected in series with the distribution feeder at the upstream side of the sensitive loads to effectively mitigate or eliminate the effects of voltage sag, voltage imbalance and other types of power quality events (Hingorani, 1995). Nevertheless, high investment and maintenance costs and complex structure are the main limitations to of Series-connected VSCs (Newman and Holmes, 2002). The Distribution Static Synchronous Compensator (D-STATCOM) is a type of shunt-connected CPDs which is mostly based on VSC and connected in parallel with sensitive loads in distribution networks to protect sensitive loads against voltage sag, voltage variation and current harmonic distortion (Choma and Etezadi-

Amoli, 2002; Escobar *et al.*, 2000). The voltage sag compensation strategy in D-STATCOM is based on the reactive power injection at the connection point for moderate voltage sag, while active power injection is mandatory to mitigate deep voltage sags (Bollen, 1999; Wang *et al.*, 1998). Therefore, a precise control strategy is necessary to improve the dynamic performances of D-STATCOMs. Such controllers should be able to accurately control the voltage or current feedback loop and the switching pattern of the inverters. Based controllers in D-STATCOM controllers can be mainly divided into voltage control and current control, which voltage control mode is mainly common in Voltage control mode, the output AC voltage should track the created reference voltage in DC quantities. Depending on the required control parameters, this procedure can be implemented using (Clarke and park transformed) d-q reference to extract active-reactive power and direct-quadratic voltage components as the transformation values and multiplying these values in the AC instantaneous voltage (Svensson and Lindgren, 1998). The main limitation of this technique is the high sensitivity of the transformed values to the imbalance voltage conditions, which make the control procedure more complex. In comparison, the current control methods such as hysteresis and average current controllers are less complex and faster than voltage control methods.

In this study, an improved control method based on voltage and current regulation is proposed and using Double Vector Control (DVC) because it has two

vector-control loops. One of the loops is taken into consideration to regulate current while the other loop regulates voltage at (PCC). Vector Current Control (VCC) is applied for compensator current regulation (Hingorani, 1995) and Vector Voltage Controller (VVC) works as outer control loop, which tracks the reference bus voltage to realize the voltage sag mitigation. In the simulation program PSCAD/EMTDC all the simulations are carried out and the relevant performance is manifested.

CONFIGURATION OF D-STATCOM WITH DUAL VECTOR CONTROLLER (DVC)

DVC is mainly a type of cascade controller designed to control the required injected current. DVC consists of two vector controllers namely Vector Current Controller (VCC) and Vector Voltage Controller (VVC).

Vector current controller: The Vector Current Controller (VCC) can be considered as a useful tool which makes the compensator current to track the reference current. Considering the schematic diagram of the shunt-connected VSC shown in Fig. 1 and applying Kirchhoff's voltage law to the VSC output filter by using Clark and Park transformation under the fixed two-coordinate $\alpha\beta$ frame, the voltage and current at the Point of Common Coupling (PCC) can be obtained as:

$$u_{(t)}^{(\alpha\beta)} - L_r \frac{d}{dt} i_r^{(\alpha\beta)} - R_r i_r^{(\alpha\beta)} = e_g^{(\alpha\beta)} \tag{1}$$

$$\frac{d}{dt} i_r^{(\alpha\beta)} = \frac{1}{L_r} u_{(t)}^{(\alpha\beta)} - \frac{R_r}{L_r} i_r^{(\alpha\beta)} - \frac{1}{L_r} e_g^{(\alpha\beta)} \tag{2}$$

where, R_r and L_r are resistance and reactance of the filter and u, e_g and i_r are the VSC output voltage, PCC voltage and injected current at the PCC, respectively.

By applying the Synchronous Reference Frame (SRF), i.e., dq-coordinate system and Phase-Locked Loop (PLL) in the VCC, the active and reactive current can be separately controlled. Therefore, Eq. (1) can be

rewritten as Harnefors and Nee, 2000; Wang *et al.*, 1998):

$$u^{(dq)*}(k) = u_{ff}^{(dq)}(k) + k_{pcc} \mathcal{E}_i^{(dq)}(k) + \sum_{n=1}^k k_{i,cc} \mathcal{E}_i^{(dq)}(n-1) \tag{3}$$

where, $u_{ff}^{(dq)}$ and $\mathcal{E}_i^{(dq)}$ are the feed-forward term and current error at each sample k , respectively and:

$$u_{ff}^{(dq)}(k) = e_g^{(dq)}(k) + R_r i_r^{(dq)}(k) + j \frac{\omega L_r}{2} [i_r^{(dq)}(k) + i_r^{(dq)*}(k)] \tag{4}$$

$$\mathcal{E}_i^{(dq)}(k) = i_r^{(dq)*}(k) - i_r^{(dq)}(k) \tag{5}$$

The proportional gain, $k_{p,cc}$ and the integral gain, $k_{i,cc}$ to attain the deadbeat response can also be defined as $L_r/T_s + R_r/2$ and $K_{p,cc} T_s/T_{i,cc}$, respectively,

where,

$T_{i,cc}$ = The integrator time constant is set to L_r/R_r

Both active and reactive currents are controlled independently with high bandwidth, even in over modulation region using the voltage limitation and Minimum Amplitude Error (MAE) tactics (Ottersten and Svensson, 2002; Svensson and Lindgren, 1998). The output voltage of VCC can be expressed in terms of SRF by substituting (4) and (5) in (1) as:

$$u_d^* = e_g^d(k) + R_r i_r^d - \frac{\omega L_r}{2} (i_r^q(k) + i_r^q) + k_{p,cc} (i_r^d - i_r^d)(k) + \sum_{n=1}^k k_{i,cc} (i_r^d - i_r^d)(k-1) \tag{6}$$

$$u_q^* = e_g^q(k) + R_r i_r^q - \frac{\omega L_r}{2} (i_r^d(k) + i_r^d) + k_{p,cc} (i_r^q - i_r^q)(k) + \sum_{n=1}^k k_{i,cc} (i_r^q - i_r^q)(k-1) \tag{7}$$

Vector Voltage-Control (VVC): The main task of the VVC is to maintain and stabilize the PCC voltage at its

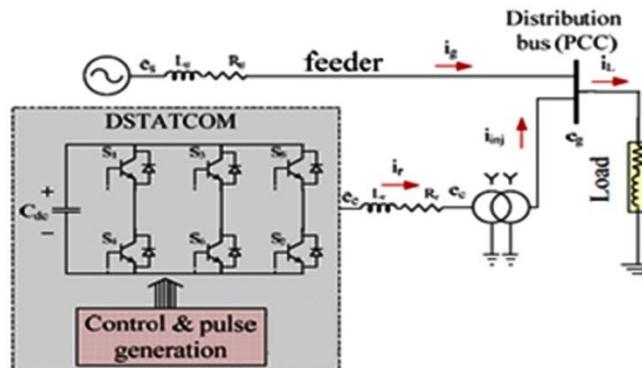


Fig. 1: Single-line diagram of system with shunt-connected VSC and L-filter

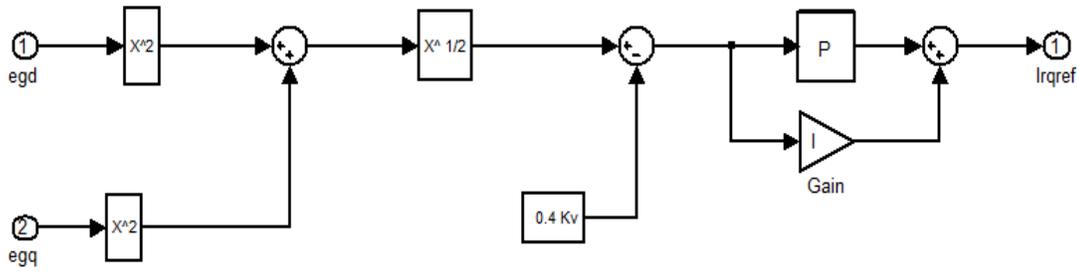


Fig. 2: Block scheme of the i_{rq}^* with its relevant process

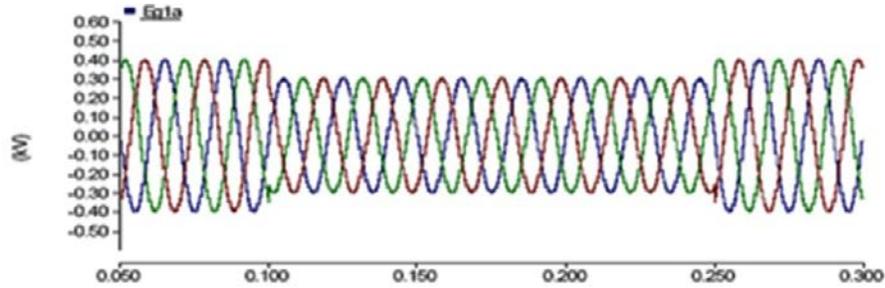


Fig. 3: Grid voltages during 25% voltage sag. Without VSC

rated value. In the presence of an injection transformer with winding ratio of 1:1 and assuming a negligible voltage drop at the transformer reactor, the PCC voltage can be considered balanced and equal to the filter capacitor voltage e_c Fig. 6. Hence, the voltage at PCC can be controlled and kept constant. Considering Fig. 1, the injected current into the grid can be obtained as:

$$i_r^{(dq^*)}(k) = i_{inj}^{(dq^*)}(k) + j \frac{\omega C}{2} [e_c^{(dq^*)}(k) + e_c^{(dq)}(k) + k_{p,vc} \varepsilon_e(k) + \sum_{n=1}^k k_{i,vc} \varepsilon_e(n-1)] \quad (8)$$

where, $\varepsilon_e(k)$ is the voltage error at sample k , is given by:

$$\varepsilon_e(k) = e_c^{(dq)^*}(k) - e_c^{(dq)}(k)$$

Therefore,

$$i_r^{d^*} = i_{inj}^d - \frac{\omega C}{2} (e_c^q - e_c^d) + k_{p,vc} (e_c^{d^*} - e_c^d) + \sum_{n=1}^k k_{i,vc} (e_c^{d^*} - e_c^d) \quad (9)$$

$$i_r^{q^*} = i_{inj}^q + \frac{\omega C}{2} (e_c^{d^*} + e_c^d) + k_{p,vc} (e_c^{q^*} - e_c^q) + \sum_{n=1}^k k_{i,vc} (e_c^{q^*} - e_c^q) \quad (10)$$

where,

$K_{p,vc}$ = The proportional gain

$K_{i,vc}$ = The integral gain

If the integrator time constant is equal to 30 ms and setting of the current and voltage controller are respectively 70% and 25% of deadbeat (Bongiorno *et al.*, 2005, Petersson *et al.*, 2005).

AC-voltage controller: The amplitude of the PCC voltage can be controlled by injecting reactive power and also the voltage e_g can be change by using the network impedance (Woodley *et al.*, 1999). Figure 2 shows the complete block scheme of the Vector Current-Controller (VCC) with its relevant process. The voltage magnitude error is transmitted to the ac-voltage controller, formed by a PI-regulator. In case of the steady-state q-voltage of $e_g^{(dq)}$ will be zero. $i_r^{q^*}$ is the output reference reactive current, which is fed to the VCC and $i_r^{d^*}$ is the reference active current which is acquired from a slow dc-link voltage controller that compensates for VSC losses. The capacitive reactive power injected into the network by the VSC, has been represented as a below:

$$Q = e_{gq} i_{rd} - e_{gd} i_{rq} = -e_{gd} \quad (11)$$

In view of the fact that e_{gq} is zero, when the voltage of grid is too low, capacitive reactive power has been injected and the current i_{rq} will be positive. Discrete time amplitude of the PI-regulator is given by:

Table 1: Control parameters gride prameter

Grid voltage	E	400 V	1 pu
Grid Current	I	40 A	1pu
Grid frequency	f	50 HZ	
Grid inductance	L_g	2.1 mH	0.114 pu
Grid resistance	R_g	0.05 Ω	0.0087 pu
Load resistance	R_l	10 Ω	1.73 pu
Load inductance	L_l	23.9 mH	1.3 pu
DC-link voltage	u_{dc}	600 V	1.5 pu
Filter resistance	R_r	24.8 m Ω	0.0043 pu
Filter inductance	L_r	2 mH	0.109 pu

Table 2: System parameter

Current controller parameters		
Proportional gain	$K_{P,cc}$	7.01(70% dead beat)
Integrator gain	$K_{i,cc}$	0
AC- voltage controller parameters		
Proportional gain	$K_{P,Q}$	0.97
Integrator time constant	$T_{i,Q}$	0.01
PLL-band with	α_{PLL}	30 rad/s

Table 3: Injection transform parameters

Rated power	S_{TR}	10 KVA	1.08 pu
Short-circuit power	E_{TR}	230 V	1 pu
Short-circuit voltage	P_{cc}	141 W	0.015 pu
Leakage inductance	V_{cc}	5.3 V	0.023 pu
Series resistance	L_{λ}	0.31 mH	0.018 pu
	R_{λ}	74.59 mΩ	0.014

$$i_{r,q}^*(k) = -k_{pQ} [\sqrt{e_g^{d*2} + e_g^{q*2}}(k) - \sqrt{e_g^{d*2} + e_g^{q*2}}(k-1)] - \sum_{n=1}^k k_{TQ} [\sqrt{e_g^{d*2} + e_g^{q*2}}(n-1) - \sqrt{e_g^{d*2} + e_g^{q*2}}(n-2)] \quad (12)$$

$$i_{r,q}^* = (-k_{pQ} - \frac{1}{S} T_{iQ}) (-0.4 + \sqrt{e_g^{d*2} + e_g^{q*2}}) \quad (13)$$

where, K_{PQ} and T_{iQ} are the proportional and integral gain of the regulator, respectively.

Performance description: Tables 1 and 2 are the controller and system parameters respectively (Woodley *et al.*, 1999). And by using PSCAD/EMTDC, simulation, control system has been investigated and tested. Figure 3 has represented the voltage at the PCC when the VSC in idle mode. As illustrated, the voltage of PCC is under the influence of a 25% voltage dip and 9° phase-angle jump. Figure 4 displayed the VSC injected a high reactive current (close to 200A.....) during voltage sag to make voltage at the PCC constant 400V (Fig. 5). According to the simulation result it is possible to compensate voltage sag with investigated controller and by changing L-filter with LCL-filter, VSC will managed the amount of reactive power needed.

System performance by applying lcl-filter and active damping: In above section the VCC described under stiff grid voltage, impedance of the grid is approximately equal to zero. If the PCC voltage stiff is not enough, e_g with the same dynamics of the injection current will changed, leading to the stability problem described above. It will be essential to overcome these problems to shown the dynamic of the grid voltage at PCC. Consequently, it should be modified configuration for the SVC by adding a capacitor ($C = 60\mu F$) (Fig. 6). Parameters for the injection transformer are shown in Table 3.

SIMULATION ANALYSIS

The control system, which has been offered, has been examined under similar voltage dip shown in

Fig. 3. The oscillations are visibly discernible in Fig. 7. Inserting a resistor as a damping term in series ($R_d = 0.5\Omega$) with the filter capacitor will lead to the prevention of this phenomenon. Nonetheless, the feed-forward term in Eq. (4) is depicted below and Fig. 8 demonstrates that the PCC voltage is adjusted to the preferred value which approximates 0.01 pu oscillations and can be observed in dq-voltage (Petersson *et al.*, 2005, Le, 1989):

$$u_{ff}^{(dq)}(k) = e_{-g}^{(dq)}(k) + (R_r - R_d) i_{-r}^{(dq)}(k) + j \frac{\omega L_r}{2} [i_{-r}^{(dq)}(k) + i_{-r}^{(dq)*}(k)] \quad (14)$$

Dynamic operation during unbalanced voltage sag:

The proposed control strategy by Simulation results has clarified that it is only appropriate for mitigation of balanced voltage sag as you can see in Fig. 8, owing to the presence of the negative-sequence in the measured quantities and to gain better cope with unbalance voltage dips should modify the configuration of the system separate to the control positive and negative-sequence of the injected current. Modifications of the negative-sequence components of the injected current will be illuminated in above section.

Double vector controller (dvc): To improve the unbalance disturbance compensation two separate controls, Synchronous Reference Frame (SRF_s) can be used (Petersson *et al.*, 2005, Sensarma *et al.*, 2001), where the positive and negative (SRF) are synchronized to positive and negative sequence component of the network voltage. The results can explain by the block scheme of Dual Vector Controller (DVC) (Woodley *et al.*, 1999). By Sequence Separation Method (SSM) can described sequence components of current injection, voltage of capacitor and filter current (Woodley *et al.*, 1999, Jung *et al.*, 2002). Equations (3 and 13) are the same for the positive sequence of VCC and VVC, respectively. To compensate for the unbalanced disturbance of the voltage, a control method is required to produce the source reference currents of D-STATCOM in the case the network voltage is unbalanced. These reference currents enter the vector controller based on which convertor voltage are made in phases a, b and c. The general trend is illustrated in Fig. 9.

In the Double Vector Controller (DVC) (Woodley *et al.*, 1999), two identical vector control blocks exist which are different only in the sign of couple factors between the d and q axes (Hingorani, 1995). The aim is to detach the positive and negative components of voltage and current in the event of the unbalanced voltage. Four signals change into subsequence components. Descriptions of these signals are provided in Fig. 10 and 11.

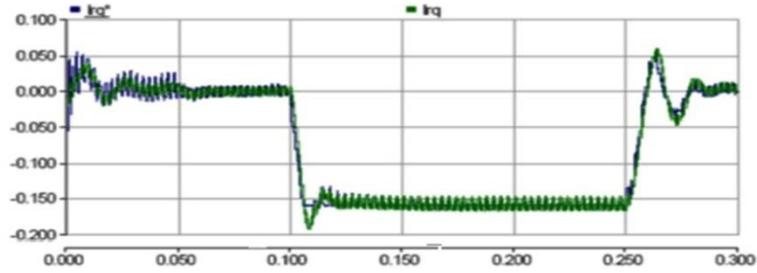


Fig. 4: Injected current of d- and q-component as a result of 25% voltage sag

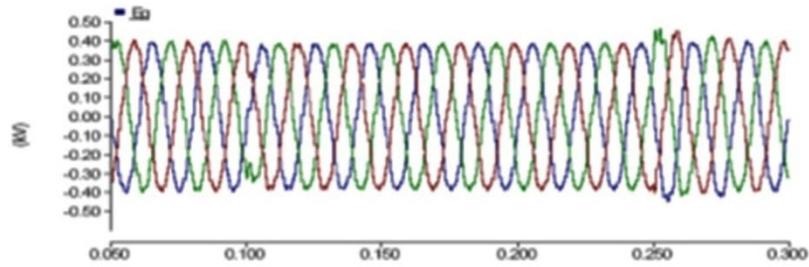


Fig. 5: Three-phase grid voltages compensated at PCC.VSC and L- filter are used

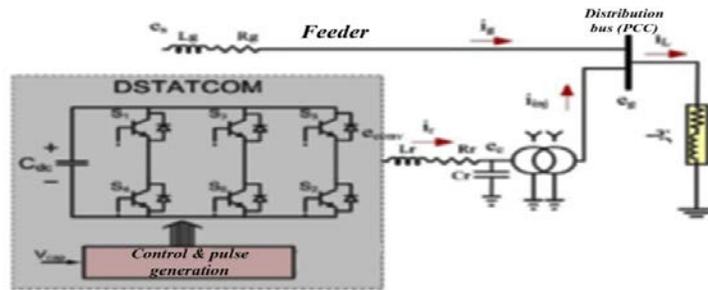


Fig. 6: Schematic related to the system with shunt-connected VSC and LCL-output filter.

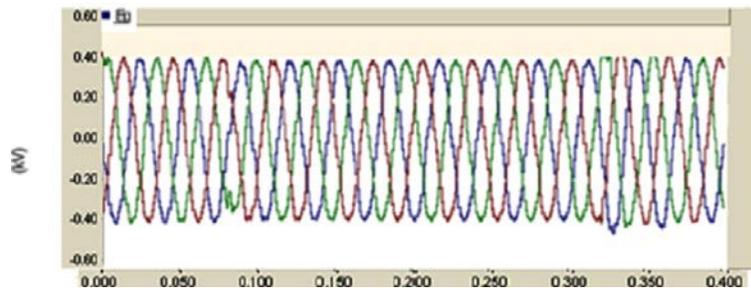


Fig. 7: The three-phase grid voltages of the PCC during the voltage sag .VSC in idle mode

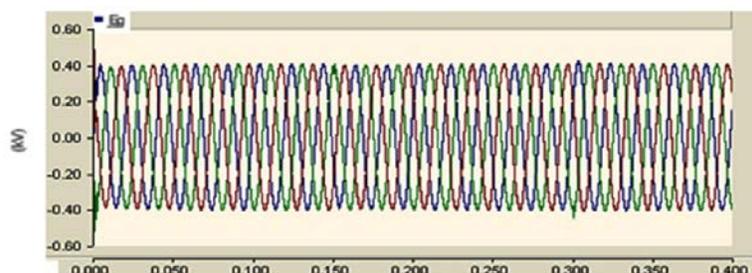


Fig. 8: Three-phase grid voltages of PCC. By applying VSC, LCL-filter and active damping

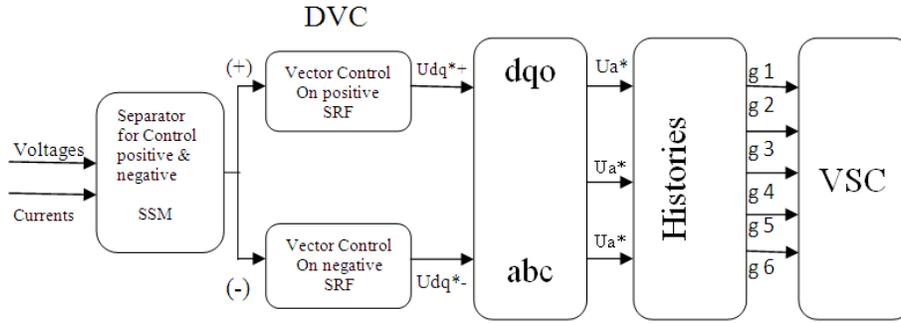


Fig. 9: Schematic of system (DVC) based on double synchronous reference frames

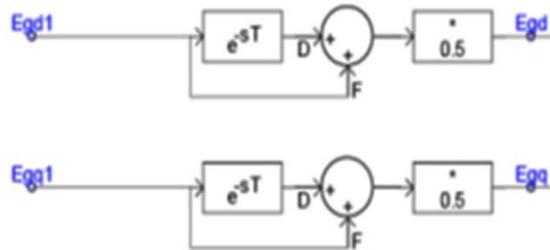


Fig. 10: Descriptions of these signals

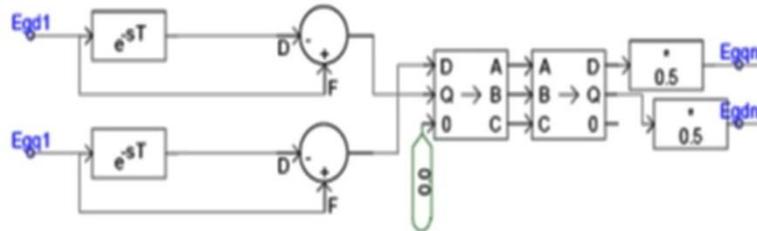


Fig. 11: Descriptions of these signals

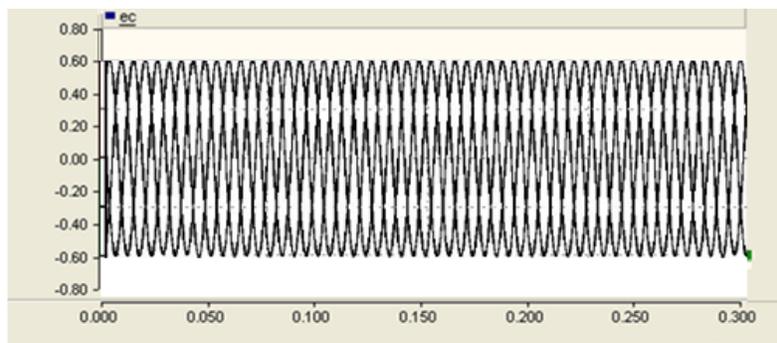


Fig. 12: Three-phase wave forms at PCC

E_g = Network voltage at PCC point
 E_c = Capacitor voltage of compensator filter
 I_r = Current of VSC convertor
 I_{inj} = Injected current to the network

$$x_d^+ = 0.5(e_d(t) + e_d(t - 0.005)) \quad (15)$$

$$x_q^+ = 0.5(e_q(t) + e_q(t - 0.005)) \quad (16)$$

$$x_d^- = 0.5(e_d(t) + e_d(t - 0.005)) \quad (17)$$

$$x_q^- = 0.5(e_q(t) + e_q(t - 0.005)) \quad (18)$$

Implementing of these four signals is shown by Eq. (16, 17), (18, 19) and Fig. 10, 11:

To compare the performance of the cascade controller that we presented in the previous section with DVC under the same unbalance voltage sag, illustrated in Fig. 7, for three-phase waveforms and by using Dual Vector Controller, it will be successful mitigation of the voltage sag and it is evidently visible in Fig. 12.

CONCLUSION

This study describes how to use VSC to mitigate voltage dip. Moreover, it discusses and shows that VSC can control and maintain the amplitude of the network's voltage with compensating voltage dip by injecting reactive power. Nevertheless, this kind of control system is completely sensitive to the parameters variations of the system. To gain at the high operation and more robust controller and structure of shunt connection, with simpler L-filter and LCL-filter has been analyzed. Investigation reveals that by selecting a cascade controller, with VVC and VCC a more powerful controller can be reached. Result of the control system has been obtained in the positive and negative SRF, in order to separate control components of positive and negative-sequence of the network voltage. Simulation results maintain that with the proposed control method, we can achieve high dynamic performance by using DVC.

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