Research Article
Energy Efficient Multiplexer and De-multiplexer Using FINFET Technology

[1]R. Arunya, [2]S. Ranjith, [1]P. Umarani, [3]A. Ramya and [1]T. Ravi
[1]Faculty of Electrical and Electronics Engineering, Sathyabama University,
[2]Department of Electronics and Communication Engineering, Jeppiaar Engineering College, Chennai,
[3]Department of Electronics and Communication Engineering, Anna University, Pandurati,
Tamil Nadu, India

Abstract: This study entirely focused on low power by reducing the switching activities and implemented with the device called FIN Field Effect Transistor. Low power has emerged as a principal theme in today's world of electronics industries. The invention of the first Integrated Circuitsb (IC) three decades ago, VLSI designers have been looking for methods to speed up digital circuits and to reduce the area for of digital system. However, the evolution of portable system and advanced DSB (Deep Sub-micron) fabrication technologies has brought power dissipation as another critical design factor. Several techniques to reduce the dynamic power have been developed, of which clock gating is predominant. The proposed DLFF use new clock gating techniques that reduce power dissipation deactivating the clock signals, which consumes less power than the existing DLFF. Here in this study we design an 8×1 multiplexer, 16×1 and 1×8, 1×16 demultiplexer using 3 bit synchronous counter output as selection lines for this multiplexer and de-multiplexer in MOSFET and FINFET technology.

Keywords: Clock gating, DLDFF, FINFET, sequential circuits

INTRODUCTION

The advantage of utilizing a combination of low-power components in conjunction with low-power design techniques is more valuable now than ever before. Requirements for lower power consumption continue to increase significantly as components become battery-powered, smaller and require more functionality. In the past the major concerns for the VLSI designers was area, performance and cost. Power consideration was the secondary concerned. Now a day's power is the primary concerned due to the remarkable growth and success in the field of personal computing devices and wireless communication system which demand high speed computation and complex functionality with low power consumption. The motivations for reducing power consumption differ application to application. In the class of micro-powered battery operated portable applications such as cell phones, the goal is to keep the battery lifetime and weight reasonable and packaging cost low (Nogawa and Ohtomo, 1998). Therefore much work focused on the low power design to reduce power consumption. Flip-Flops are the basic elements for storing information and they are the fundamental building blocks for sequential circuit. In sequential circuits clock is the control signal which is used for synchronization of data to functional elements. In Flip-Flops switching

activity as a primary power management concern. The basic low-power design techniques, such as clock gating for reducing dynamic power, or multiple voltage thresholds (multi-Vt) to decrease leakage current, are well-established and supported by existing tools (Young-Won *et al.*, 2009). Low power consumption is generally achieved only by careful hand crafted design. Power consumption in CMOS circuits can be divided in two components: Static dissipation, which is due to leakage current. Leakage current is a small current that flows through the transistor even when the transistor is off and there is no switching activity. Dynamic dissipation, which is due to charging and discharging of load capacitances and short circuit currents while both pMOs and nMOS networks are partially on. Dynamic power can be expressed as $P_{dyn} = 1/2\ \alpha\ cfv2\ dd$ (Ranjith, 2014). Internal clock gating technique is the most popular method for power reduction of clock signal. In Data transition look ahead D flip flop the gating function is derived within the flip flop without any external control signal. This technique used in many sequential circuits for reducing power. Proposed Data transition look ahead flip flop which consumes less power and area when compared with existing data transition look ahead flip flop, since flip flop finds most of application in counter here much work focused an synchronous counter is designed by using existing DL-DFF and proposed DLDFF. Then by using counter the

multiplexer and demultiplexer was designed by using FINFET technology (Labaey and Pedram, 1996).

MATERIALS AND METHODS

FINFET technology: As manometer process technologies have advanced, chip density and operating frequency have increased, making power consumption in battery-operated portable devices a major concern. Even for non portable devices, power consumption is important because of the increased packaging and cooling costs as well as potential reliability problems. Thus, the main design goal for VLSI (Very-Large-Scale Integration) designers is to meet performance requirements within a power budget. Therefore, power efficiency has assumed increased importance. FinFETs (fin-type field-effect transistors), an emerging transistor technology that is likely to supplement or supplant bulk CMOS (Complementary Metal-Oxide-Semiconductor) at 22-nm and beyond, offer interesting delay-power tradeoffs. The steady miniaturization of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) with each new generation of CMOS technology has provided us with improved circuit performance and cost per function over several decades. However, continued transistor scaling will not be straightforward in the sub-22 nm regime because of fundamental material and process technology limits. The main challenges in this regime are twofold:

- Minimization of leakage current (subthrehsold þ gate leakage)
- Reduction in the device-to-device variability to increase yield

FinFETs have been proposed as a promising alternative for addressing the challenges posed by continued scaling. Fabrication of FinFETs is compatible with that of conventional CMOS, thus making possible very rapid deployment to manufacturing.

An important FinFET characteristic is threshold Voltage (Vth) controllability. The Vth at each gate of a FinFET can be controlled through the application of a voltage at the other gate. Because the Vth governs both transistor power consumption and delay, Vth controllability is a powerful tool for circuit optimization traditionally, in multiple supply voltage circuits, power is saved through the use of a lower supply voltage on off-critical paths. For instance, a conventional dual supply Voltage (Vdd) circuit may use the nominal high-performance Vdd for the technology process at hand and, on off-critical paths, a lower Vdd, which is typically 60-70% in magnitude compared to the higher Vdd. Advantage of FinFET's double-gate structure to further optimize power and performance.

Data-transition look-ahead D FLIP-FLOP (DL-DFF): The internal clock gating technique is appropriate for flip flops with low switching rate in the input data. DLDFF is one kind of flip-flop which has its own internal clocking system. In case of provision of the external clock leads to normal switching which will lead to unwanted power loss, but in DLDFF the clock will be generated only during the data transition so that the large amount of power is reduced (Nogawa and Ohtomo, 1998). The main feature of this flip-flop family is a mechanism for predictive turn off the internal clock when input and output data are equal. Since there exists an overhead associated with local clock gating, the use of these flip-flops is justified for low switching activities of the input data (Yeap, 2009). The Data-Transition Look-Ahead D Flip-Flop is a positive edge triggered, non inverting flip-flop. The output of the data-transition look-ahead, (DL), circuit is an XNOR function of D and Q. When D = Q, the DL circuit output is 0 and the internal clock is deactivated (Nogawa and Ohtomo, 1998). When D and Q are different the DL circuit output is 1 and the clock Control circuit activates the internal clock signals shown in Fig. 1.

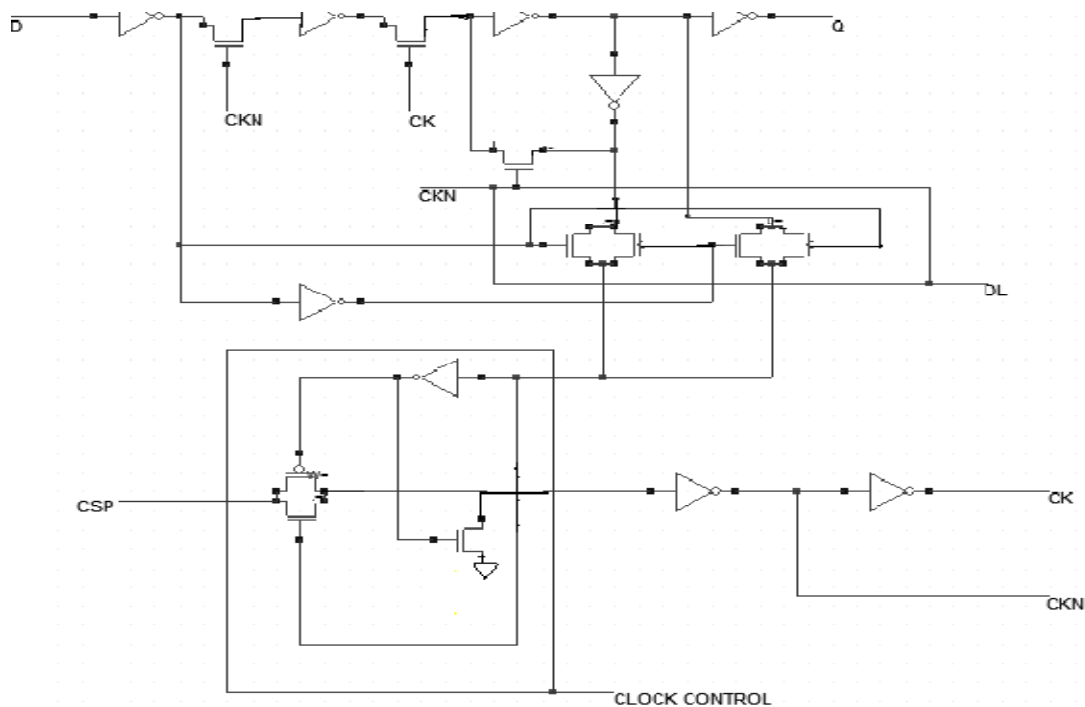
Fig. 1: Existing data transition look ahead D flip flop

Fig. 2: Proposed data transition look ahead flip flop

The Pulse Generator (PG) circuit generates a short pulse, CKI, at every rising edge of the external clock, CP. CKI then triggers the flip-flop if D ≠ Q. If there was no pulse generator, this flip-flop could be triggered by data instead of the clock. For example, if D ≠ Q and the rising edge of CKI arrives, then the clock pulse, CK, is generated and Q changes. However, if D changes again while the clock is still high and becomes different from Q, then another pulse of internal clock, CK, would be generated and the flip-flop would be actually triggered by Data (Stojanovic and Oklobdzija, 1999). The transmission gate in the existing Data transition look ahead D flip flop consumes more area and power. In order to reduce the power and area, the transmission gate is replaced by NMOS pass transistor, because in transmission gate there is no threshold loss, but the pass transistor followed by inverter will produce exact logic, that is without any threshold loss. In order to reduce power and less area we replaced the transmission gate in to pass transistor which is shown in Fig. 2. When compare to the existing DLDFF the proposed DLDFF consumes less power and less area.

Synchronous counter using proposed DLDFF: Counter are available in two categories: asynchronous and synchronous counters. In an asynchronous counter, a flip flop output transition serves as a source for triggering other flip flop. In other words, the clock input of some or all flip flops are triggered, not by the common clock pulses, but rather by the transition that occurs in other flip-flops outputs in synchronous counter, the clock inputs of all flip flops receive the common clock. There are different type of synchronous counter they are Binary Counters, Up-Down Binary Counter and BCD Counter, Binary counter with Parallel Load, Ring and Johnson counters. They are used to generate time signals necessary for digital operations. The synchronous counter is similar to a ripple counter with two exceptions: The clock pulses are applied to each FF and additional gates are added to ensure that the FFs toggle in the proper sequence. The advantage of synchronous counter over asynchronous counter is that, Since all inputs are synchronized with a common clock, no interrupts can occur in the middle of a state transition in synchronous counters, all flip-flops change simultaneously and in asynchronous counters, the propagation delay of the flip-flops add up to produce the overall delay. Although synchronous counters usually have more combinational logic, the propagation delay through these gates is small compared to the propagation delay through many stages of flip-flops. The conventional 3 bit synchronous counter shown in Fig. 3, in which the output of the combinational logic is given as input to the flip flop and triggering operation of the FF is monitored by a global clock. The inputs to the FF from the combinational logic block are unconditionally captured at every triggering edge of CLK, regardless of the previous value of the FF to advance system states (Young-Won *et al.*, 2009). This architecture evaluates the new data values at every clock cycle and its output is given to its associated Flip Flops (FFs) at every triggering edge of the clock. The simplified functions of 3 bit synchronous counter are given by expression as:
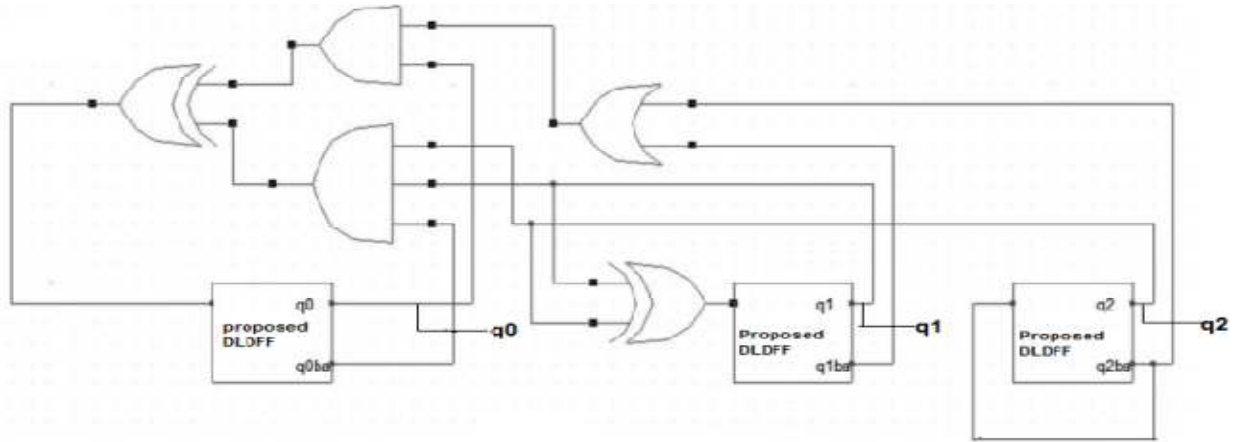
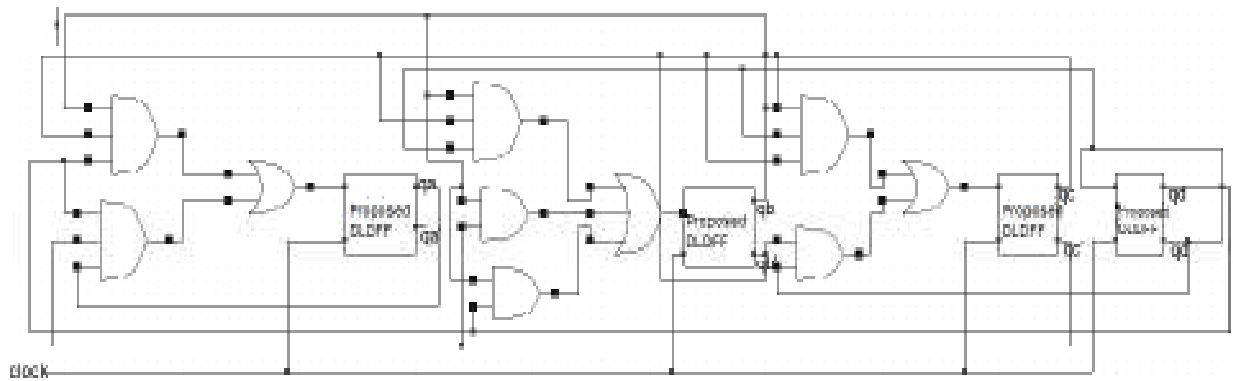Fig. 3: Three bit synchronous counters using proposed data transition look ahead D flip flop

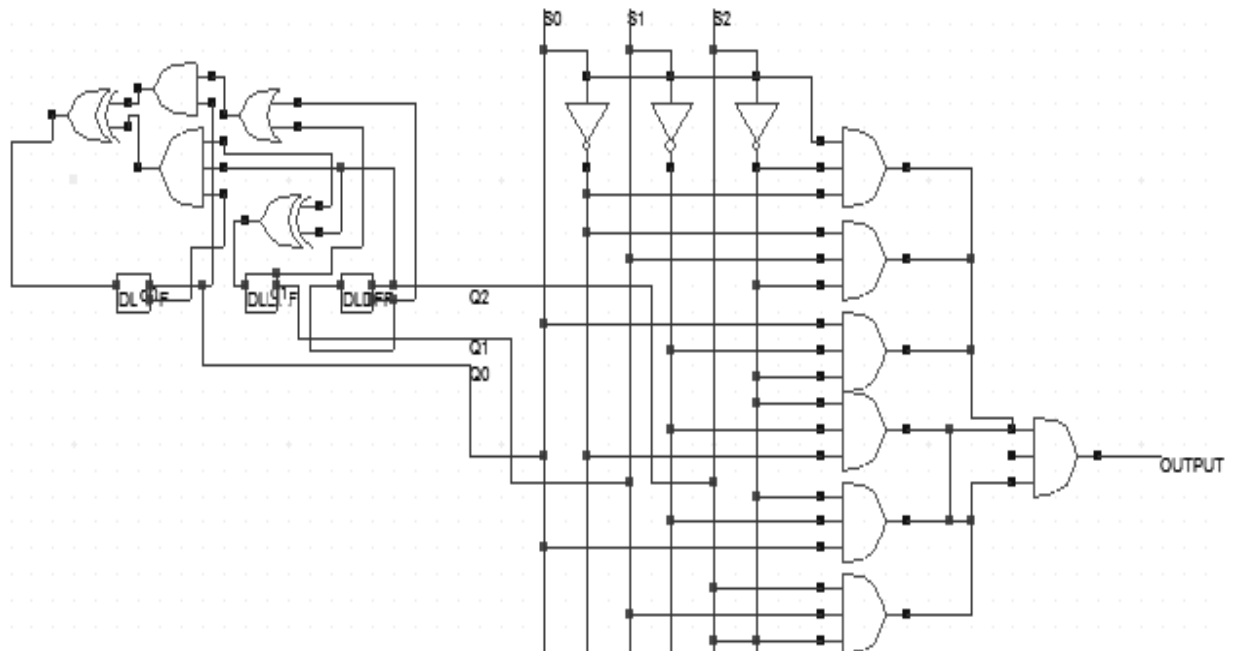Fig. 4: Decade synchronous counter using proposed DLDFF

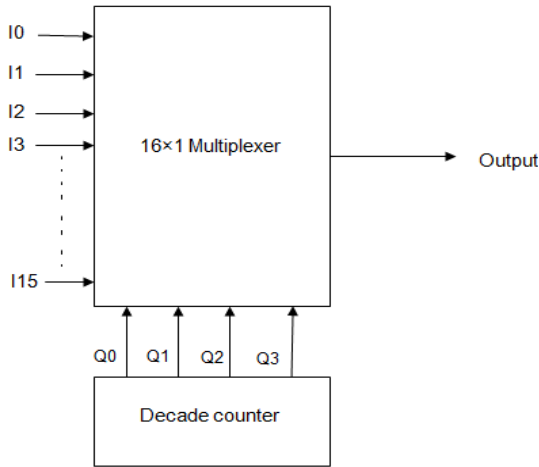Fig. 5: 8×1 multiplexer using 3 bit synchronous counter

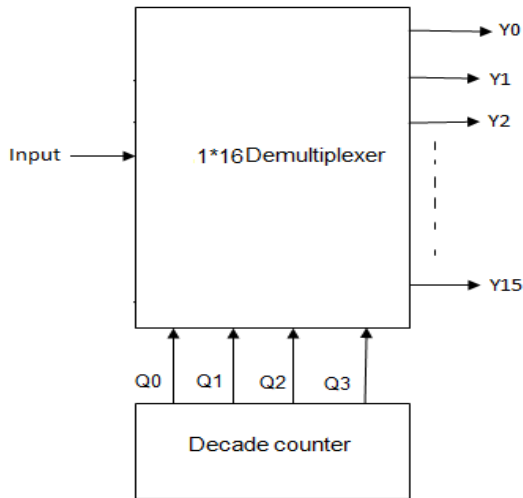Fig. 6: 16×1 multiplexer using decade synchronous counter

Fig. 7: 1×16 demultiplexer using decade synchronous counter

Q0 = DA = A'BC + AB' + AC', Q1 = DB = BC, Q2 = DC = C'

In this decade counter using proposed data transition look ahead flip flop shown in Fig. 4. Consumes low power when compared with existing counters using data transition look ahead D flip flop. A decade counter or BCD counter counts in binary-coded decimal from 0000 to 1001 and back to 0000 (Stan *et al.*, 1998). Because of the return to 0 after a count of 9, a decade counter does not have a regular pattern, unlike a straight binary count. The circuit can easily be drawn with four DLD flip flops, seven and gates and three or gate. Synchronous decade counter can be cascaded to form a counter for decimal numbers of any length. The simplified functions of decade counter are given by expression as:

DA = QB QC QD + QA Q'C Q'D

DB = Q'B QC QD + QB Q'C + QB Q'D

DC = QC Q'D + Q'A Q'C QD

DD = Q'D

The circuit can easily be drawn with four DLD flip flops, seven and gates and three or gate. Synchronous decade counter can be cascaded to form a counter for decimal numbers of any length.

Multiplexer and de-multiplexer using synchronous counter: There are many applications for counters in digital system. As multiplexer find significant application in the field of communication. Here in this study a multiplexer shown in Fig. 5 and 6 and demultiplexer shown in Fig. 7 are designed by using counter output as selection for multiplexer and demultiplexer. Multiplexers also are used in building digital semiconductors such as Central Processing Units (CPUs) and graphics controllers. At the receiving end of the data link a complementary demultiplexer is normally required to break single data stream back down into the original stream. Often, a multiplexer and demultiplexer are combined together into a single piece of equipment, which is usually referred to simply as a "multiplexer". Both pieces of equipment are needed at both ends of a transmission link because most communication systems transmit in both directions. Here in demultiplexer the input is single input but at the output side we will get number of signals. At the receiving end, a demultiplexer, or demux, chooses the correct destination from the many possible destinations by applying the same principle in reverse.

Synchronous counter using proposed data transition look ahead D flip flop is used to design 16×1 multiplexer shown in Fig. 6. Here in this multiplexer there are sixteen inputs and single output. In this decade counter count will start from "0000 to 1001". The 16×1 multiplexer uses four selection lines for the output selection. Since it is decade counter the output of counter gives Q0, Q1, Q2 and Q3.

De-multiplexer there will be only one input and N no of the output N represent the selection lines that are 2n. Since it's a decade counter it can count from "0000 to 1001". So here only nine outputs are observed. Here the 1×16 de-multiplexer shown in Fig. 7 needs four selection lines. These are the some of the applications of counters, since both multiplexer and demultiplexer finds an extensive application in the field of communications such as in telephony, video processing, digital processing etc. With this three bit synchronous counter and synchronous decade counter multiplexer and Demultiplexer are designed efficiently. By using the proposed data transition look ahead flip flop in these counters the power consumption of multiplexer and demultiplexer is reduced when compared to the counters designed using existing data transition look ahead flip flop.
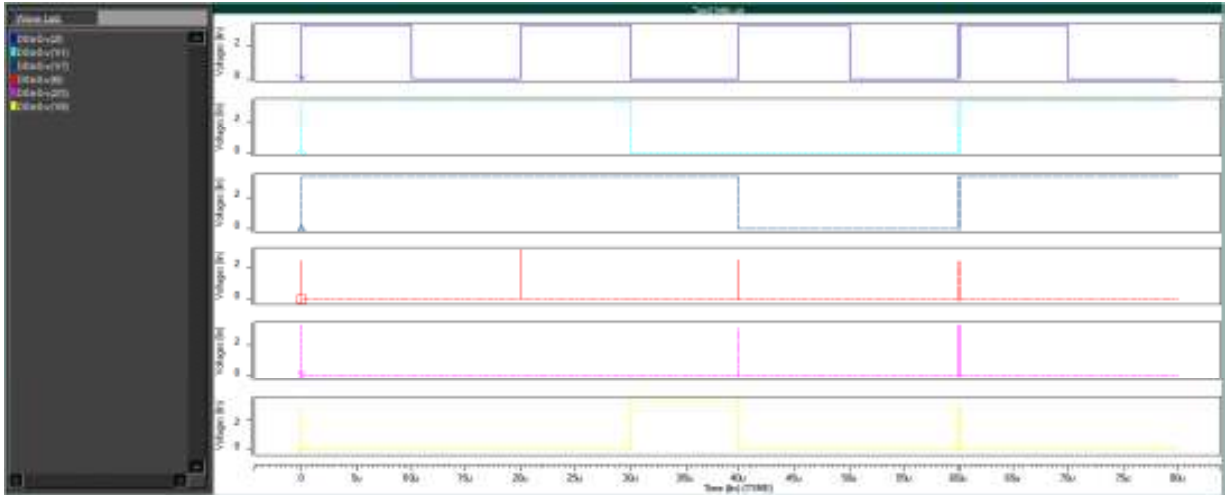
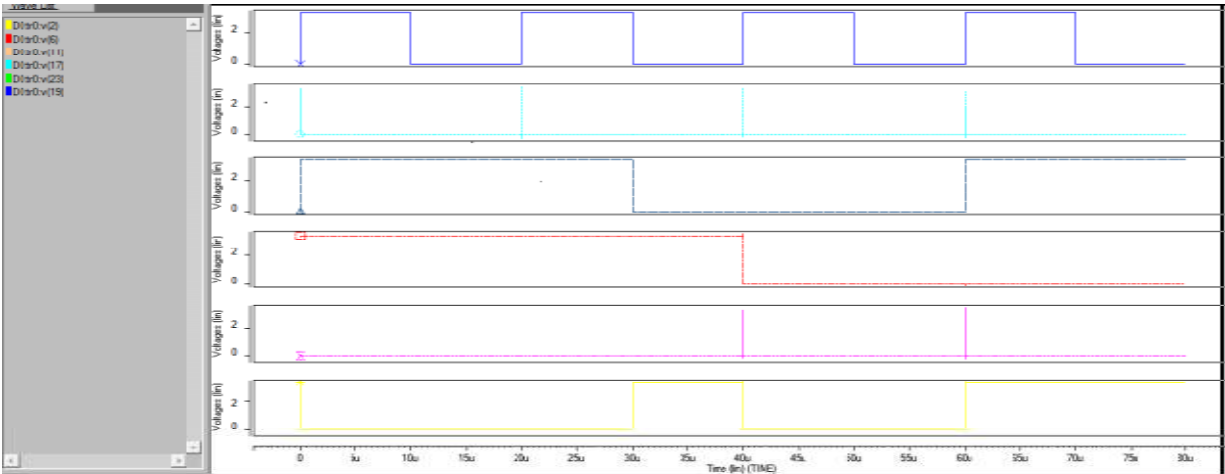Fig. 8: Output waveform of existing DLDFF
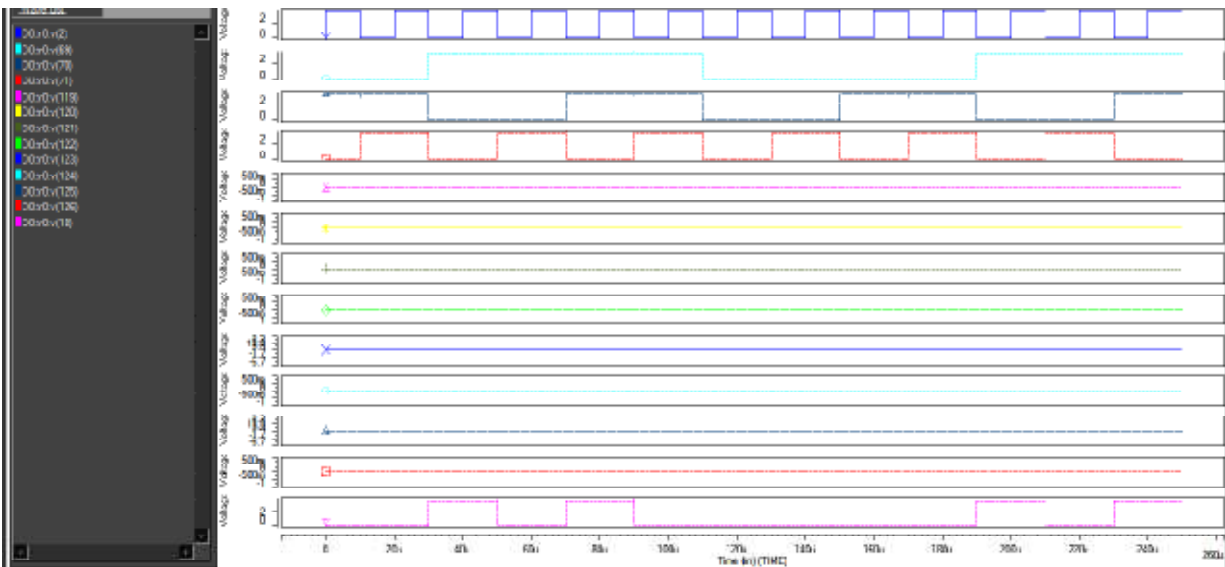

Fig. 9: Output waveform of modified DLDFF

Fig. 10: Output waveform of 8×1 multiplexer using existing counter
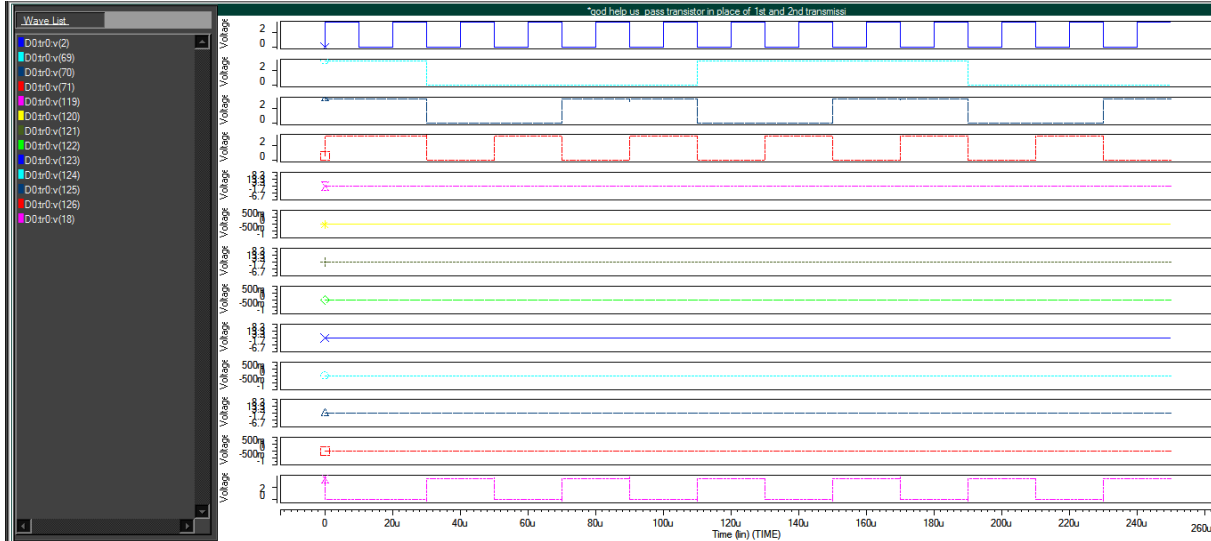
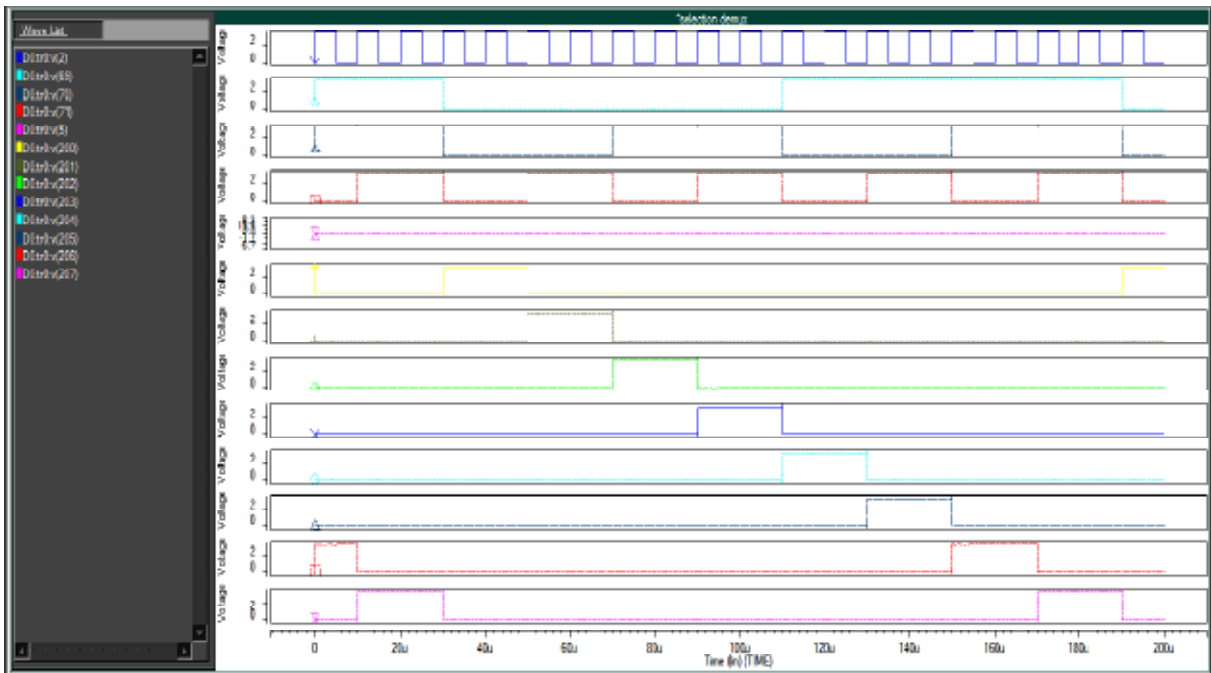Fig. 11: Output waveform of 8×1 multiplexer using proposed counter

Fig. 12: Output waveform of 1×8 demultiplexer using proposed counter

Table 1: Power analysis of DLDFF

Flip-flops	Number of transistors	Power consumption in MOSFET	Power consumption in FINFET
Existing DLDFF	50	2.814E-07	9.646e-09
Proposed DLDFF	47	2.297E-07	9.533e-09

RESULTS AND DISCUSSION

In this study the simulation output has been views has been given. The design is simulated by using the simulation tool "HSPICE". The technology used is MOSFET and FINFET. Operating voltage is 0.9 v and operating frequency is 5 kHz. The simulation results Simulation wave form of existing DLDFF shown in Fig. 8, Simulation waveform of modified DLDFF shown in Fig. 9. Simulation waveform of 8×1 multiplexer using existing counter shown in Fig. 10, Simulation waveform of 8×1 multiplexer using proposed counter shown in Fig. 11. Simulation waveform of 1×8 demultiplexer using proposed counter shown in Fig. 12, Simulation waveform of 16×1 multiplexer using existing decade counter shown in Fig. 13, Simulation waveform of 1×16 demultiplexer using
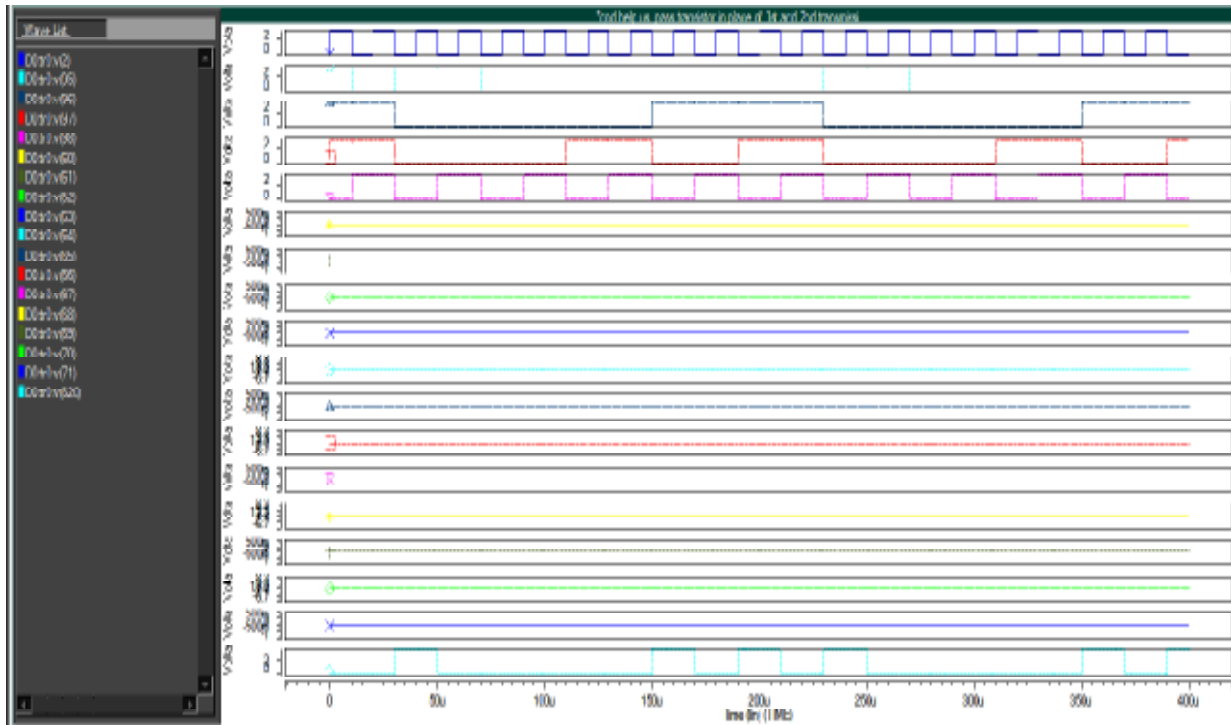
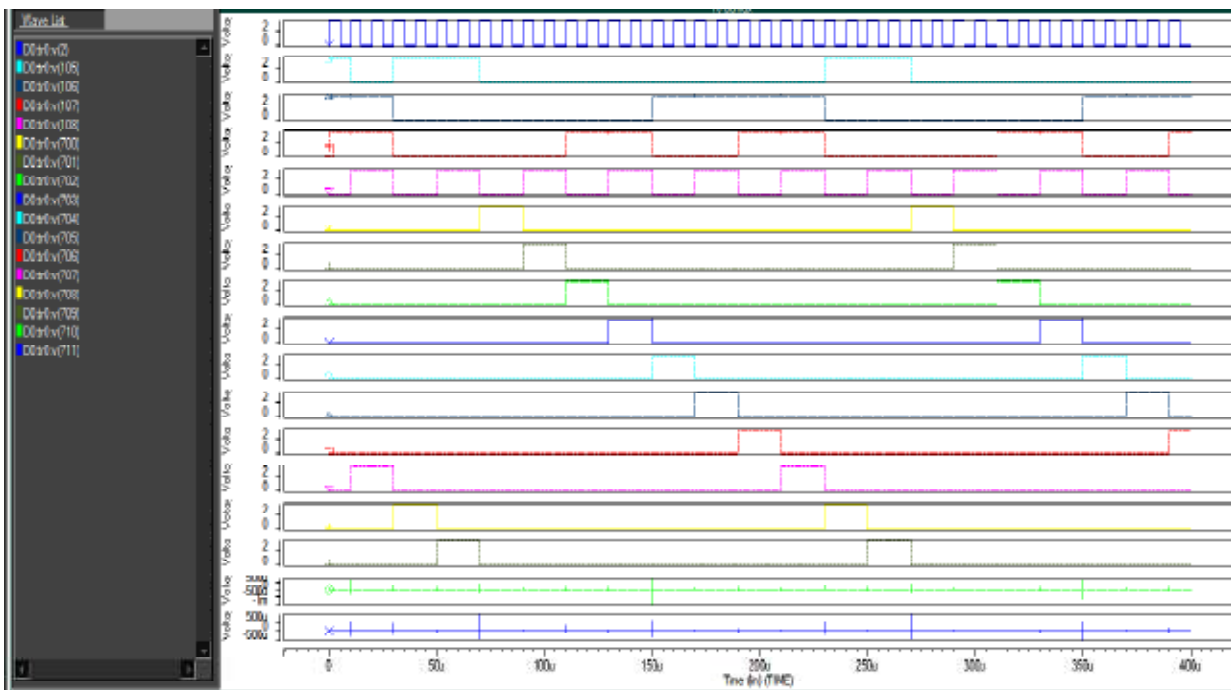Fig. 13: Output waveform of 16×1 multiplexer using existing decade counter

Fig. 14: Output waveform of 1×16 demultiplexer using proposed decade counter

proposed decade counter shown in Fig. 14. The Power and transistor count of existing and proposed DLDFF has been compared in Table 1. The power comparison of all the designs carried out in this study has been compared with MOSFET and FINFEET technology.

Performance analysis: In Table 1 and 2 the performance analysis of flip flop and synchronous counters, mux, demux were simulated by using 32 nm MOSFET and FI NFET technology using HSPICE TOOL. And there results were compared.

Table 2: Power analysis of MOSFET and FINFET based design

Technique	Type of technique	Power consumption in MOSFET		Power consumption in FINFET	
		Existing	Proposed	Existing	Proposed
Counters	3 bit synchronous counters DLDFF	9.014E-07	8.961E-07	3.299E-07	3.068E-07
	Decade counter DLDFF	1.483E-06	1.373E-06	9.202E-07	7.802E-07
Multiplexer	8×1 multiplexer using 3 bit synchronous counter	9.202E-07	9.118E-07	3.186E-07	2.965E-07
	8×1 multiplexer using 3 bit decade counter	1.334E-06	1.221E-06	9.723E-07	9.587E-07
	16×1 multiplexer using decade counter	1.126E-06	1.024E-06	9.442E-07	9.196E-07
	16×1 multiplexer using synchronous counter	1.026E-06	9.871E-07	9.168E-07	8.691E-07
Demultiplexer	1×8 demultiplexer using 3 bit synchronous counter	1.295E-06	1.115E-06	9.3015E-07	9.193E-07
	1×8 demultiplexer using 3 bit decade counter	1.635E-06	1.598E-06	9.853E-07	9.672E-07
	1×16 demultiplexer using decade counter	1.830E-06	1.715E-06	1.036E-06	9.975E-07
	1×16 demultiplexer using synchronous counter	1.906E-06	1.792E-06	1.322E-06	1.184E-06

CONCLUSION

In this study, 8×1, 16×1 multiplexer and 1×8, 1×16 de-multiplexer are designed and selection line of this Mux and Demux is provided by auto generating circuit called synchronous counter using proposed DLDFF. The transmission gate in the existing Data transition look ahead D flip flop consumes more area and power. In order to reduce the power and area, the transmission gate is replaced by NMOS pass transistor, because in transmission gate there is no threshold loss, but the pass transistor followed by inverter will produce exact logic, that is without any threshold loss. In order to reduce power and less area were placed the transmission gate in to pass transistor. When compare to the existing DLDFF the proposed DLDFF consumes less power and less area. So that with the proposed DLDFF the Mux, Demux and Counters are designed and also area of both existing and proposed methods are compared. The simulation result has been done using HSPICE software using 32 nm MOSFET and FINFET technology.

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