Research Article

Area and Energy Efficient Intelligent Level Shifter

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Abstract: The level shifters play a crucial role in multi supply systems and it is the effective way to reduce the power consumption at system level. The level shifters are the interfacing circuits, used to interface multi supply voltage modules. The design and analysis of competent level shifter is described in this study, with a lower energy and delay constraints. It is a novel architecture with multiplexer based circuit to perform both levels-up and levels-down operations. Proposed level shifter circuit has designed and analyzed using 90 nm CMOS process technology. This proposed level shifter can be operated at different supply voltages from 0.3 to 0.5V of VDDL and 0.9 to 1.1V of VDDH. The experimental and simulation results exhibits that the proposed circuit is having levels-up and levels-down average power is 17.57 nW and delay is 1.49 ns at a simulated frequency of 1 MHz. The level shifter has designed and simulated with different load and operating conditions. The proposed competent level shifter circuit is suitable for low power and high speed applications.

Keywords: Area efficient, delay, level shifter, low power, multi VDD systems, VLSI

INTRODUCTION

To reduce the power consumption at system level Dynamic Voltage Scaling (DVS) is the preferable technique (Usami and Horowitz, 1995), due to the quadratic relationship between the supply voltage and power, the reduction in supply voltage is a very effective technique to decrease the power consumption. However, there will be a bit delay overhead may results from the circuit. This is the technique used in advanced digital processing equipments for the reduction of energy consumption and it has extended to the sub threshold regime (Alioto, 2012). The low power consumption at sub threshold operation, facilitate the development of miniature bio medical sensors, devices and bio medical equipments (Zhang *et al.*, 2013). To facilitate DVS, the system can be grouped as critical path group and non-critical path group. All critical path groups are operated with higher Voltage (VDDH) and non-critical path groups are operated with lower supply Voltage (VDDL) to achieve the better power and speed constraints. By this the power consumption at system level improves without degrading in the performance. Level shifter is required at the interface because, the output from a low voltage cluster cannot be connected directly to a PMOS transistor of a high voltage cluster, since the PMOS transistor will not become perfectly OFF (MP2) and would be partially ON due to low voltage cluster output produces the LOW voltage and it leads to short circuit power consumption between
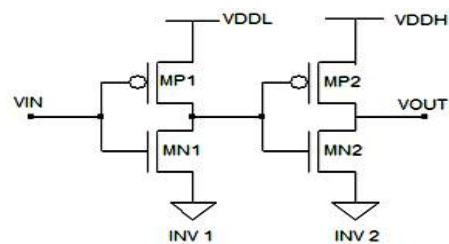

Fig. 1: Need of level shifter

VDDH and GND due to partially ON NMOS and PMOS transistors as shown in the Fig. 1.

To overcome this worst situation level shifters are the interfacing circuits, being used to interface non-critical groups and critical groups. These level shifters are the voltage converters will convert, an output from a low VDD cluster is to drive the input to a high VDDH cluster and will convert high VDD cluster to drive the input to a low VDD cluster. The main challenge in DVS Scheme is to design an efficient Level shifter with lower power and delay. In other words, the level shifter must be a capable circuit to perform level shifting with a minimal power consumption and delay. The remaining paper has arranged as follows, Review on existing level shifters, proposed energy efficient intelligent level shifter, simulation outcomes and comparisons with other circuits and conclusion.

The traditional level shifter and LS proposed by Srinivasulu *et al.* (2014) are the Differential Cascode

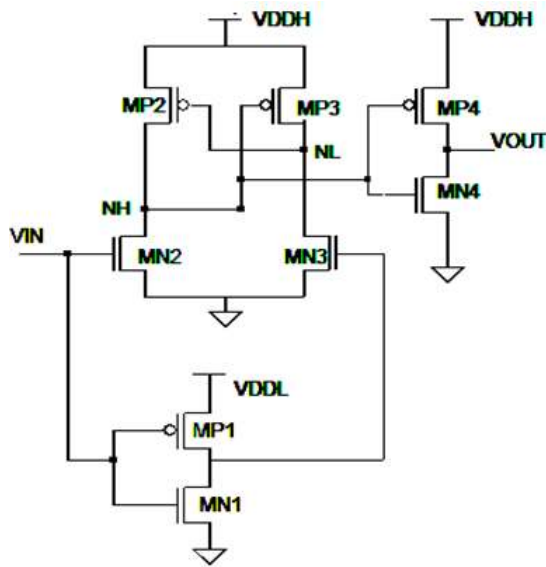**Corresponding Author:** Srinivasulu Gundala, Department of ECE, SITAMS, Chittoor, India

Fig. 2: Traditional DCVS level shifter

Voltage Switch (DCVS) logic is shown in the Fig. 2. Assuming, when VIN is logic '1', MN3 turns OFF and MN2 turns ON. Due to the feedback action of cross coupled PMOS MP2 and MP3, node NH is pulled down to VSS, node NL goes to VDDH, MN4 will become OFF and MP4 turns ON and VOUT node will be charged to VDDH, hence VOUT results as logic '1'. The DCVSL level shifter is a ratioed circuit there is a contention problem between pull up and pull down, will leads to increase in power consumption and delay. As a consequence pull up network impedance and pull down network impedances need to be balanced.

For practical purposes, a CMOS logic circuit with mixed gates operating on a lower supply voltage VDDL and on a higher supply voltage VDDH may be preferred. However, any gate operating on VDDH and connected after the gate operating on VDDL generates a short-circuit current.

A solution presented by Wooters *et al*. (2010) have constructed with two parts. The primary part is a DCVSL circuit with NMOS ON diode at top and the secondary part is a customary Differential Cascade Voltage Switch circuit to attain the power rail swing. It can avoid in-between power rails; unfortunately it is very poor in speed constraint.

Another technique invented and developed by Romli *et al*. (2012) has designed a level shifter for the reduction of the dynamic power (P_D) by optimizing the widths and lengths of the MOSFETs. It may reduce the dynamic power but there will be poor performance at leakage power and delay.

The design invented by Chen *et al*. (2006) performs level shifting at sub threshold voltage, with a realistic pull down size and its drawback is ON reference circuit path of current limiter, hence it may have high static power consumption.
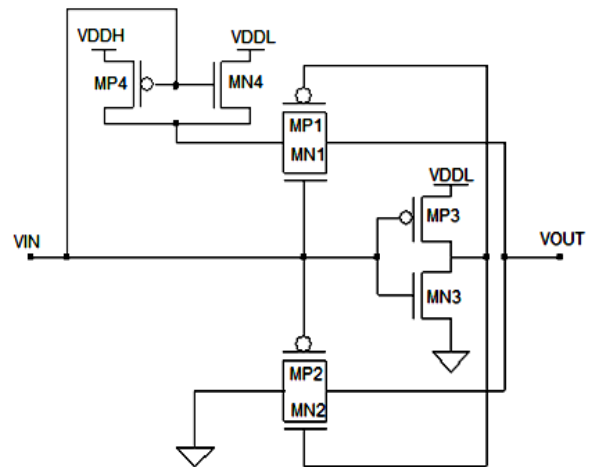

Fig. 3: Proposed high speed EELS

The novel design, designed and developed by Yuji and Kuroki (2012) performs level up shift and any errors in the logic signals, but requires more no. of transistor and area occupying is more.

MATERIALS AND METHODS

Generally to perform level up shift level shifters are used and to perform level down shift, extra inverters are needed and it requires extra circuitry also to select required type of shift operation. The proposed is a novel level shifter shown in the Fig. 3 performs both level up and level down shifts just based on VIN and no extra circuitry is needed. The level shifter comprises with two parts, one is to select type of level shifting operation, and another one is actual level shifter. The type of level shift selector comprises with MP4 and MN4 with VIN as SEL (select) input. When VIN is lower voltage the design will act as a level up shifter and when VIN is higher voltage the design will act as a level down shifter, here the type of shift selection takes place just based on VIN without human interpretation, hence it is named as Intelligent Level Shifter (ILS).

The circuit has designed to perform level up shift from 0.4 to 1 V and level down shift from 1 to 0.4 V, therefore the VDDL and VDDH voltages has taken 0.4 and 1 V respectively. The transistors MP4 and MN4 act as a 2X1 multiplexer. When VIN is 0.4 V the PMOS transistor MP4 becomes ON, i.e., VDDH is selected at the same time inverter output is logic '0', upper transmission gate (MP1 and MN1) becomes ON, hence VOUT will become equal to VDDH. When VIN is 1V the NMOS transistor MN4 becomes ON, i.e., VDDL is selected at the same time inverter output is logic '0', upper transmission gate (MP1 and MN1) becomes ON, hence VOUT will become equal to VDDL. When VIN is logic '0' the PMOS transistor MP4 becomes ON, i.e., VDDH is selected at the same time inverter output is logic '1', lower transmission gate (MP2 and MN2)
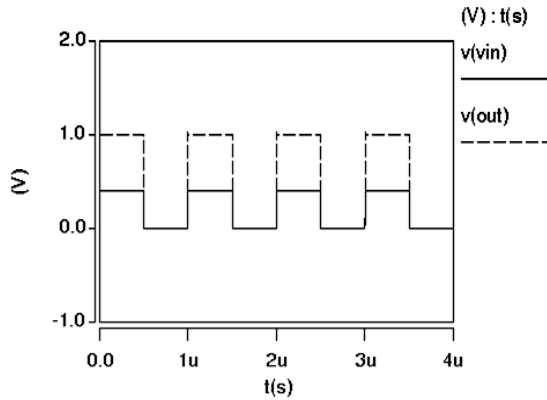
(a)
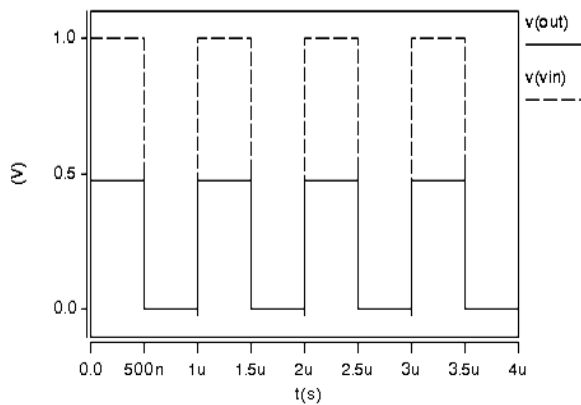
(b)

Fig. 4: Wave form of, (a) level up shift, (b) level down shift

becomes ON, hence VOUT will become equal to VSS, i.e., logic '0'.

RESULTS AND DISCUSSION

The Area and Energy Efficient ILS is modelled and simulated using Synopsys spice tools and characteristics of the design has analyzed at the operating temperature of 27°C, at frequencies of 100, 500 KHz and 1 MHz with a varying load conditions by taking different analysis like parametric analysis, power and delay analysis, load analysis and comparative analysis, illustrated in the Fig. 4 to 8.

Waveforms of the area and energy efficient ILS: It can be viewed in the wave forms that the design has produced stable output refer Fig. 4a is the level up waveform and Fig. 4b is the level down waveform, at the operated frequency 1 MHz.

Parametric analysis: As a parametric analysis the design has simulated for different VDDL and VDDH values and analyzed for both level up and level down
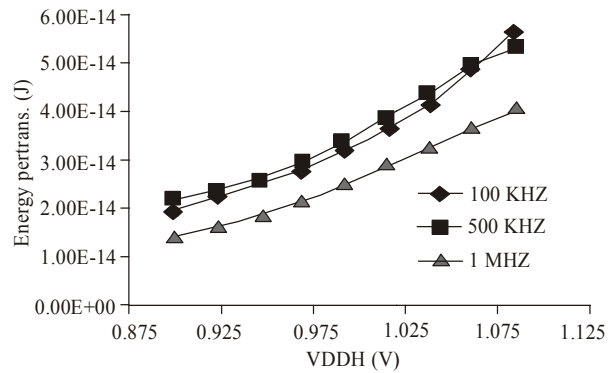

Fig. 5: Energy per trans. of area and energy efficient ILS as a function of VDDH
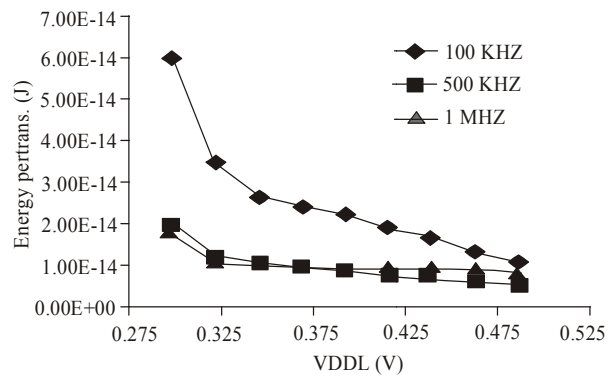

Fig. 6: Energy per transition of area and energy efficient ILS as a function of VDDL
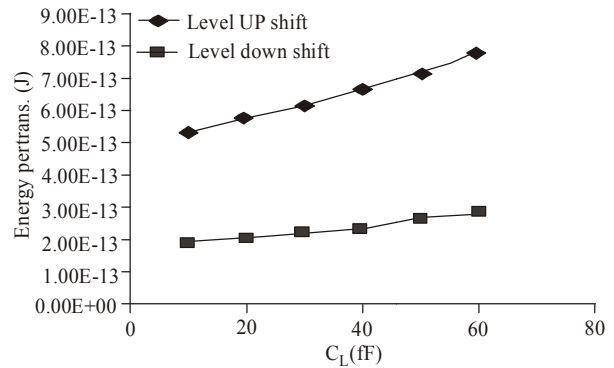

Fig. 7: Energy per trans. of area and energy efficient ILS as a function of CL

shifts. While level up shift the VIN is varied from 0.3 to 0.5 V in a steps of 0.1 V at a constant of VDDH 1 V. While level down shift the VIN is varied from 0.9 to 1.1 V in a steps of 0.1 V at a constant of VDDL 0.4 V.

In both cases energy and area ILS has produced stable output and its energies per transitions are shown in the Fig. 5 and 6 at 1 MHz operated frequencies.

Load analysis: The load analysis of the energy and area efficient ILS is performed to determine the capability of the design when loading effect occurs. The

Table 1: Comparison between various level shifters

Work/Ref.	Type of shift	Tech. (nm)	Frequency (Hz)	VDDL (V)	VDDH (V)	Power (nW)	Delay (nsec)
Wooters *et al.* (2010)	Level up	130	1M	0.188	1.2	-	57.90
Romli *et al.* (2012)	Level up	180	1K	0.400	3.0	Pa = 1.49	15.65
Chen *et al.* (2006)	Level up	130	50K	0.100	1.2	Ps = 8.00	50.00
Yuji and Kuroki (2012)	Level up	350	10K	0.230	3.0	Pa = 58.00	100.00
Lutkemeier and Ruckert (2010)	Level up	90	1M	0.200	1.0	Ps = 6.60	18.40
Lanuzza *et al.* (2012)	Level up	90	1M	0.180	1.0	Ps = 6.40	22.00
Luo *et al.* (2014)	Level up and down	65	20K	0.400	1.2	Ps= 15.00	15.00
Proposed	Level up	90	1M	0.400	1.0	Pa = 25.34	0.19
	Level down	90	1M	0.400	1.0	Pa = 9.80	2.80

Ref.: Yuji and Kuroki (2012) performs level up as well as logic error corrections; Pa: Average power or active power; Ps: Static power; Proposed design performs level-up and level-down shifts
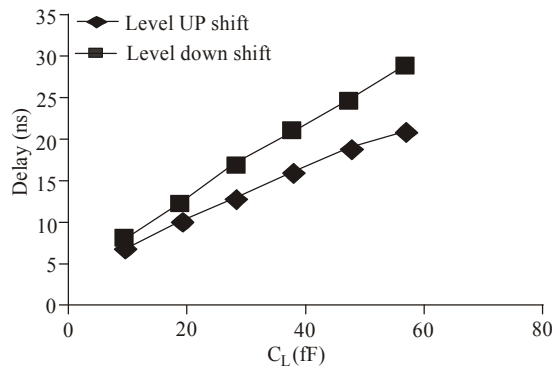

Fig. 8: Delay of area and energy efficient ILS as a function of CL

energy and area efficient ILS can be used to interface in any part of the target circuit. Thus is it important to analyse ILS operates under varying loading conditions, taken from 10 to 60 fF in steps of 10 fF varying load at 1 MHz frequency. The experimental results shown in the Fig. 7 and 8, demonstrates that the circuit consumes almost same power and delay at different loading conditions.

Comparative analysis with other designs: Table 1 shows the comparison between various level shifters. The level shifter circuit design in Wooters *et al.* (2010) performs level up shift only and it has a propagation delay of 57.9 nsec at 130 nm CMOS technology. The circuit design in Romli *et al.* (2012) also performs the level-up shift only and it has an ave. power of 1.49 nW with the delay of 15 nsec at 180 nm at the signal frequency of 1 KHz. The level converter design in Chen *et al.* (2006) performs level up shift and it has the static power of 8 nW with a delay of 50 nsec at the operated frequency of 50 KHz and simulated at 130 nm CMOS technology and having the provision to shift from 0.1 to 1.2 V. The design in Yuji and Kuroki (2012) performs level up shift and it has incurred the active power 58 nW and delay 100 nsec at 350 nm CMOS technology at a frequency of 10 KHz. The level shifter circuits in Lutkemeier and Ruckert (2010) and Lanuzza *et al.* (2012) perform level up shifts and it has almost same static Power approximately 6.5 nW and delay 20 nsec at 90 nm CMOS technology operated at 1 MHz. The

above designs are sufficient to perform level-up shift, and to perform level-down shift the design modifications like VDDs or circuit topologies need to be changed or additional circuits need to perform only for level down shifts. The novel level shifter Luo *et al.* (2014) design performs level-up shift and level-down shift 0.4 to 1.2 and 1.2 to 0.4 V, respectively have utilized 2×1 Mux with automatic selection of type of shift.

The proposed energy and area efficient ILS performs both level-up and level-down shifts and has average level-up and level-down active power is only 17.57 nW at a frequency of 1 MHz and average delay of level-up and level-down shift is only 1.49 nsec and it is low compared to the other designs.

CONCLUSION

The designed, energy and area efficient ILS circuit have utilized only 8 numbers of transistors to carry out both level-up and level-down operations and it is comparably low compared with other designs, hence it is area efficient. From the Fig. 5 and 6 it can be observed that it has consumed level-up and level-down average energy per transition at 1 MHz is 1.50E-14J and it is low compared with other designs, hence it is said to be as energy efficient design. The proposed energy and area efficient ILS offers a very low delay, average level-up and level-down delay is 1.495 nsec. The waveform of proposed design shows that the level shifter can able to shift from 0.3-0.5 V to 1 V and 0.9-1.1 V to 0.4V. By taking Multi Vt devices there can be further improvement we can show on Energy, Delay and Power consumptions.

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