

Research Article

Hybrid Controller for Three Level Shunt Active Power Filter to Reduce Supply Current Harmonics for Power Quality Improvement

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Abstract: Shunt Active Power Filter (SAPF) of electric power has become a grown-up technology for mitigating supply current harmonics and compensation of reactive power in the grid. In this study, a combined Proportional Integral (PI) and Fuzzy Logic Controller (FLC) are proposed to extract required reference current of the SAPF for balanced, unbalanced with static and dynamic conditions. The DC bus voltage of three level diode clamped multilevel PWM inverter functioning as a SAPF is maintained at stable value by regulating the current error using the conjunction of PI and FLC algorithm. Switching pulses for the multilevel inverter are generated from the sampled reference phase voltage magnitudes as in the case of conventional space vector PWM. The implementation of PI and FLC algorithm is executed using MATLAB fuzzy logic tool box. The simulation results shows that, the proposed model provides with low harmonic content in supply side and necessary reactive power is supplied to the Point of Common Coupling (PCC) thereby power factor of the system is improved in both static and dynamic conditions.

Keywords: Active power filter, fuzzy logic, harmonics, power factor, proportional integral, reactive power

INTRODUCTION

In recent decades, a lot of research is being carried out about mitigation of harmonic distortion for power quality improvement. The current drawn from the nonlinear loads such as power electronic converters, variable frequency converters, electronic chokes, SMPS, UPS etc., is not linear with grid supply voltage. This load is said to be nonlinear and naturally it is composed of odd order currents, which are stated as multiples of the fundamental frequency. These nonlinear loads generate the harmonics (Bhim *et al.*, 1999) and reactive power in the utility system and results in poor power factor (Akagi *et al.*, 2007) and distort supply current and voltage waveform at the load end (Abdelmadjid *et al.*, 2007). The harmonic current cannot deliver to active power and need to be reduced to improve the power quality. Traditionally, passive filters have been used to mitigate the supply current harmonics and power factor improvement. Passive harmonic filters can be designed as single-tuned elements that provide a low impedance path to harmonic currents at a particular frequency. This passive filter has several disadvantages such as it resonates with the supply impedance, large in size and it is limited with few harmonics. The various methods of Static VAR Compensators (SVCs) are proposed to solve the power quality issues (Luis *et al.*, 2005); but some SVCs have disadvantage such as it create lower-order harmonics themselves and response time too long

for fast-fluctuating loads (Karuppanan and Mahapatra, 2010b). Currently, active power filters have been deliberate widely for the harmonic and reactive power compensation. The active power filter can be connected in series for harmonic voltage compensation and it is connected in parallel for the compensation of harmonic current. The common SAPF is used with two level voltage source inverter (Bhattacharya *et al.*, 1998), but these are limited for low power applications and power handling capabilities (Routimo *et al.*, 2007). For high power applications three level multilevel inverters are proposed for active power filters (Vodyakho *et al.*, 2008a). The advantages of these inverters are less switching losses (Vodyakho *et al.*, 2008b), harmonics are less on the ac side, lower voltage stress on power devices (Bhim *et al.*, 1998). The SAPF with three phase three level inverter using conventional Space Vector Pulse Width Modulation (Salim *et al.*, 2011) and PI controller is used to extract reference current and experimental model is presented to validate the simulation results (Elango and Manikandan, 2014). In Karuppanan and Mahapatra (2010a), presents PI, PID and FLC are used to extract reference current for the SAPF with current controlled two level voltage source inverter. Hysteresis current controller is used to generate the switching pulses for the inverter.

In this study depicts feasibility of PI combined with FLC based SAPF to compensate the reactive power and harmonic mitigation in supply side due to nonlinear loads for balanced, unbalanced supply

voltage with static and dynamic load conditions. The performance of the SAPF is depends on two important control strategies such as reference current extraction and generation of PWM for three level inverter. The advantage of FLCs over the other controllers is that it does not involve precise mathematical model and it is more robust than conventional controllers (Singh *et al.*, 2007). The combination of PI and FLC estimates reference current I_{max} which is multiplied with unit currents to produce the required reference currents. Switching pulses for the three level inverter are generated from the sampled reference phase voltage magnitudes as in the case of conventional space vector PWM.

METHODOLOGY

Shunt active power filter: Shunt Active Power Filters are used to compensate supply current harmonics by injecting equal and opposite harmonic compensating current in to the point of common coupling. In this scheme the SAPF serves as a current source injecting the harmonic components generated by the non linear load but phase shifted by 180°. As a result, harmonic currents contained in the load current are cancelled by the effect of the active filter and the source current remains sinusoidal and in phase with the respective phase to neutral voltage (Rashid, 2001). Further, with a suitable control scheme, the shunt active power filter can also supply required reactive power into the load and thereby power factor of the system is improved. The compensation characteristic of SAPF is shown in Fig. 1.

Principle of compensation: The instantaneous current and the source voltage are expressed as follows:

$$i_s(t) = i_L(t) - i_c(t) \quad (1)$$

$$v_s(t) = V_m \sin \omega t \quad (2)$$

If a nonlinear load is applied, then the load current becomes nonlinear and is expressed using Fourier series as follows:

$$i_L(t) = I_1 \sin(\omega t + \phi_1) + \sum_{n=2}^{\infty} I_n \sin(n\omega t + \phi_n) \quad (3)$$

The instantaneous load power is then given by:

$$p_L(t) = v_s(t)i_L(t) \quad (4)$$

Which is then rewritten as follows:

$$p_L(t) = V_m \sin \omega t \{I_1 \sin(\omega t + \phi_1) + \sum_{n=2}^{\infty} I_n \sin(n\omega t + \phi_n)\} \quad (5)$$

The Eq. (5) is expressed as follows:

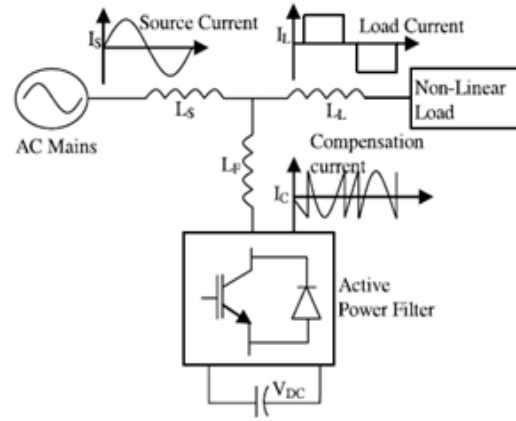


Fig. 1: Compensation characteristics of SAPF

$$p_L(t) = V_m I_1 \sin^2 \omega t \cos \phi_1 + V_m I_1 \sin \omega t \cos \omega t \sin \phi_1 + V_m \sin \omega t \sum_{n=2}^{\infty} I_n \sin(n\omega t + \phi_n) \quad (6)$$

Now, $p_L(t)$ can be expressed as:

$$p_L(t) = p_f(t) + p_r(t) + p_h(t) \quad (7)$$

where,

$$p_f(t) = V_m I_1 \sin^2 \omega t \cos \phi_1 = v_s(t)i_s(t) \quad (8)$$

with,

$$i_s(t) = \frac{p_f(t)}{v_s(t)} = I_1 \sin \omega t \cos \phi_1 = I_{sm} \sin \omega t = I_{max} \sin \omega t \quad (9)$$

$$\text{where, } I_{sm} = I_1 \cos \phi_1 \quad (10)$$

The three phase source currents after compensation is:

$$i_{sa}^*(t) = I_{max} \sin \omega t \quad (11)$$

$$i_{sb}^*(t) = I_{max} (\sin \omega t - 120) \quad (12)$$

$$i_{sc}^*(t) = I_{max} (\sin \omega t + 120) \quad (13)$$

This maximum value of $i_{sa}^*(t)$, $i_{sb}^*(t)$ and $i_{sc}^*(t)$ of the reference currents I_{max} is predicted by varying DC bus capacitor voltage using the conjunction of PI and FLC.

Role of the DC capacitor: The DC side capacitor provides to maintain a constant DC voltage with a low ripple in steady state and it serves as an energy storage element to supply the real power difference between load and source during the transient period. In steady state the real power supplied by the source is equal to the real power demand of the load. In case any change in load conditions, the real power demand in load side changes (Shailendra and Agarwal, 2003). The difference in real power between source and load is

Table 1: Switching states of one leg of inverter

Output voltage	Switching states			
	S11	S21	S31	S41
Vd	ON	ON	OFF	OFF
Vd/2	OFF	ON	ON	OFF
0	OFF	OFF	ON	ON

compensated by DC capacitor. If the DC capacitor voltage is attained the reference voltage, the real power supplied by the source is equal to load demand. The real and reactive power injection results in the ripple voltage of the capacitor which introduces finite delay.

Three level diode clamped multilevel inverter: The most commonly used multilevel topology is the diode clamped inverter, in which the diode is used as

clamping device to clamp the DC bus voltage to achieve the steps in output voltage. A three level inverter is usually preferred for high power applications. It has the advantages that the blocking voltage of each switching device is one-half of the dc link voltage and the harmonics contents output voltage is far less than those of two-level inverters at the same switching frequency. It is also known as a “neutral clamped” inverter, consists of two capacitors are connected in series and center point uses as the neutral. Each phase leg of the three level inverter has two pairs of switching devices are in series. The center of each device pair is clamped to the neutral through clamping diodes. Table 1 gives the switching states for one leg of multilevel inverter to obtain the output voltages. The simulation diagram of three level diode clamped inverter as shown in Fig. 2.

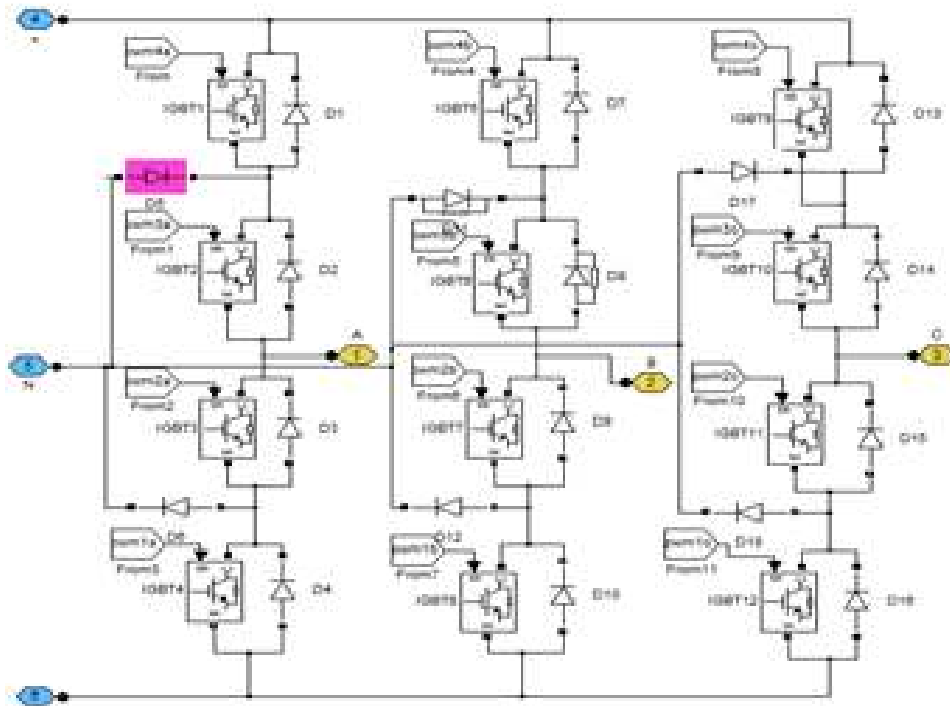


Fig. 2: Three level diode clamped inverter

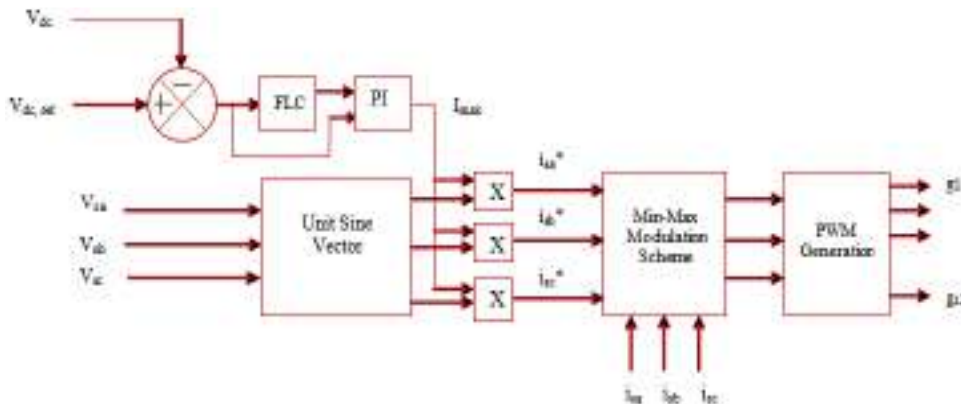


Fig. 3: Block diagram of reference current generation

Proposed block diagram: The actual capacitor voltage is compared with the reference DC voltage to produce the error signal and it feeds to generate the maximum current through conjunction of PI and FLC technique and these can be multiplied with unit sine vector signals to produce the reference currents (i_{sa}^* , i_{sb}^* , i_{sc}^*) for the SAPF system operation. The proposed reference current generation is shown in Fig. 3. The required PWM pulses are generated using Min-Max modulation scheme by comparing the actual supply current and reference current and it is feed into the three level inverter.

Fuzzy logic controller: Fuzzy logic is a form of many-valued logic; it deals with approximate value rather than fixed and accurate. This logic is inferred from the

fuzzy set theory in 1965 by zadeh. In this concept the transition is between membership and non-membership function and boundaries of fuzzy sets are vague. The fuzzy control system does not need an exact mathematical model, can work with vague inputs, can handle non-linearity and are more robust than conventional controllers. To execute the fuzzy logic control of SAPF in closed loop, the DC link capacitor voltage is sensed and compared with reference DC voltage. This error signal is given to the low pass filter through the limiter which allows fundamental components only. The error signal $e(n)$ and change of error signal $ce(n)$ are used as inputs for fuzzy controller as shown in Fig. 4. FLC output is given to PI controller to estimate the maximum reference currents I_{max} .

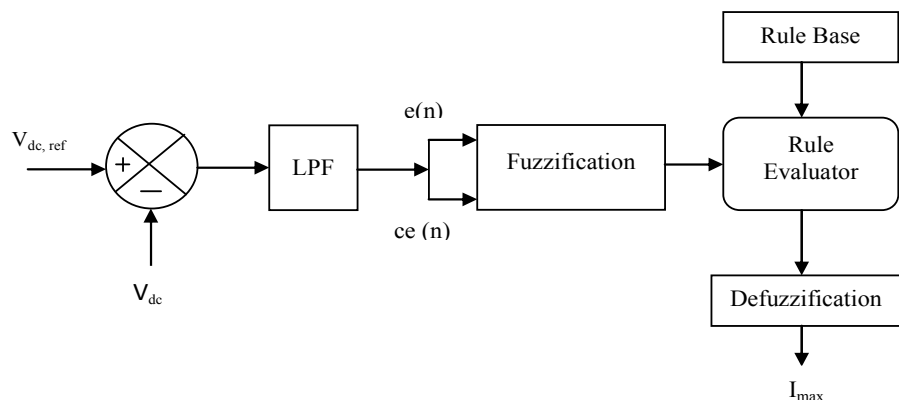
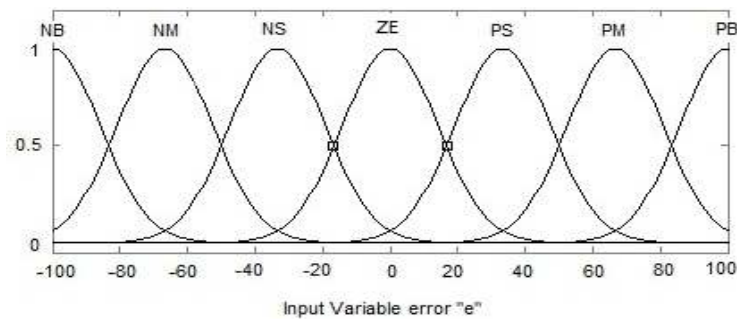
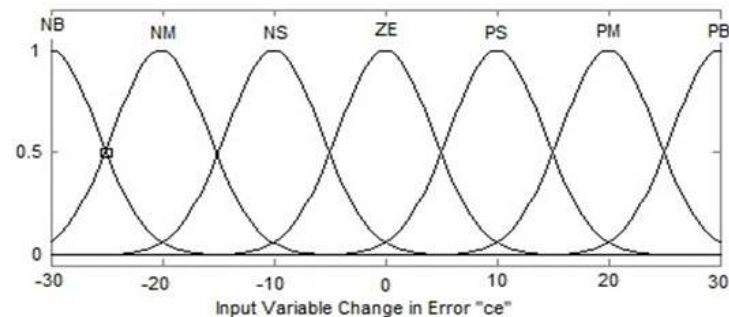


Fig. 4: Schematic diagram of fuzzy logic controller



(a)



(b)

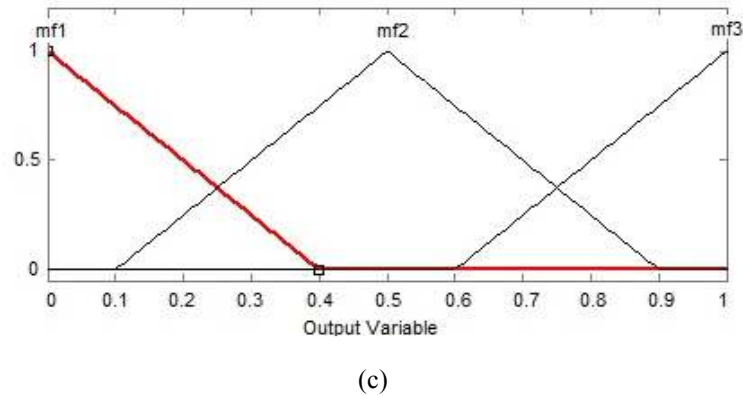


Fig. 5: Membership functions for the (a) error e (pu), (b) change in error ce (pu) (c) output du (pu)

Table 2: Rule base to find K_p

E							
CE	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NM	NS	ZE	PS
NM	NB	NB	NM	NS	ZE	PS	PM
NS	NB	NM	NS	ZE	PS	PM	PB
ZE	NM	NS	ZE	PS	PM	PB	PB
PS	NS	ZE	PS	PM	PB	PB	PB
PM	ZE	PS	PM	PB	PB	PB	PB
PB	PS	PM	PB	PB	PB	PB	PB

Table 3: Rule base to find K_i

E							
CE	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NB	NM	NS	ZE	PS
NS	NB	NB	NM	NS	ZE	PS	PM
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PM	PB	PB
PM	NS	ZE	PS	PM	PB	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB

The FLC is differentiate as follows:

- Seven fuzzy sets (NH, NB, NS, Z, PS, PB, PH) for each input and output variables
- Triangular membership function
- Mamdani-operator
- Defuzzification using the centroid method

Fuzzification: The Fuzzification Process converts numerical variables into linguistic variables. This is achieved with the different types of fuzzifiers (membership functions). Fuzzy Linguistic Variables are used to represent qualities spanning a particular spectrum. In this SAPF system, the error between reference signal and actual signal can be assigned as Negative High (NH), Negative Big (NB), Negative Small (NS), Zero (Z), Positive Small (PS), Positive Big (PB) and Positive High (PH). The error, change in error and output membership functions is shown in Fig. 5.

Membership functions: The membership function is a graphical representation of the magnitude of contribution of each input. It associates a weighting

with each of the inputs that are processed, define functional overlap between inputs and ultimately determines an output response.

Rule elevator: The essential FL operations are necessary for estimation of fuzzy set rules are AND (\cap), OR (\cup) and NOT ($-$) for intersection, union and complement functions, respectively.

Defuzzification: It is the process of creating a necessary output in linguistic variables according to the equivalent membership degrees and these variables have to be transformed in to crisp number. The various methods of Defuzzification methods are Centroid, Bisector, Middle of Maximum (MOM), Smallest of Maximum (SOM) and Largest of Maximum (LOM) etc. In this system centroid method is used for implementation.

Rule base: The linguistic control rules are stored by rule base which are given to rule evaluator (decision making logic). The 49-rules are proposed to find the value of K_p and K_i to estimate the reference current for the SAPF is given in Table 2 and 3.

Table 4: Ranges of error

Fuzzy set	Ranges of error $e(n)$	Ranges of change in error $ce(n)$
ZE	$ZE = 0$	$ZE = 0$
NS	$(0 \geq NS \geq -33.34)$	$(0 \geq NS \geq -10)$
NM	$(-33.34 \geq NM \geq -66.13)$	$(-10 \geq NM \geq -20)$
NB	$(-66.13 \geq NB \geq -100)$	$(-20 \geq NB \geq -30)$
PS	$(0 \geq PS \geq 33.34)$	$(0 \geq PS \geq 10)$
PM	$(33.34 \geq PM \geq 66.13)$	$(10 \geq PM \geq 20)$
PB	$(66.13 \geq PB \geq 100)$	$(20 \geq PB \geq 30)$

Fuzzy-PI controller: The error can be determined from the difference between the reference DC voltage and actual voltage across the capacitor. The output of the fuzzy logic controller determines the K_p and K_i values based on the lower and upper values error ranges in the fuzzy rules. The error ranges of K_p and K_i are given in the Table 4. The simulation diagram of the fuzzy and PI

controller is shown in Fig. 6. The saturation block obliges upper and lower bounds on a given signal. When the input signal is within the specified range the lower limit and upper limit parameters, the input signal passes through unchanged. When the input signal is outside these bounds, the signal is clipped to the upper or lower bound. The output $u(t)$ determines the maximum current I_{max} which is multiplied with actual source current to calculate the actual reference current.

RESULTS AND DISCUSSION

The proposed SAPF is designed and simulated using MATLAB/SIMULINK platform. The scheme consists of source and filter impedance, nonlinear load

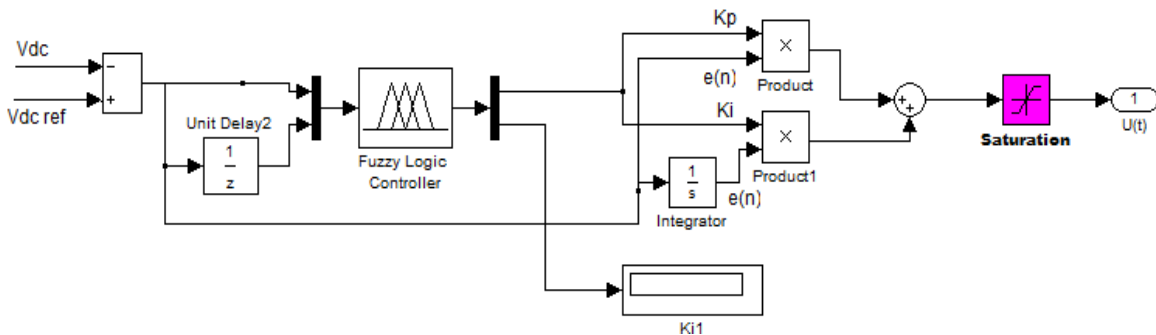


Fig. 6: Simulation diagram of the fuzzy and PI controller

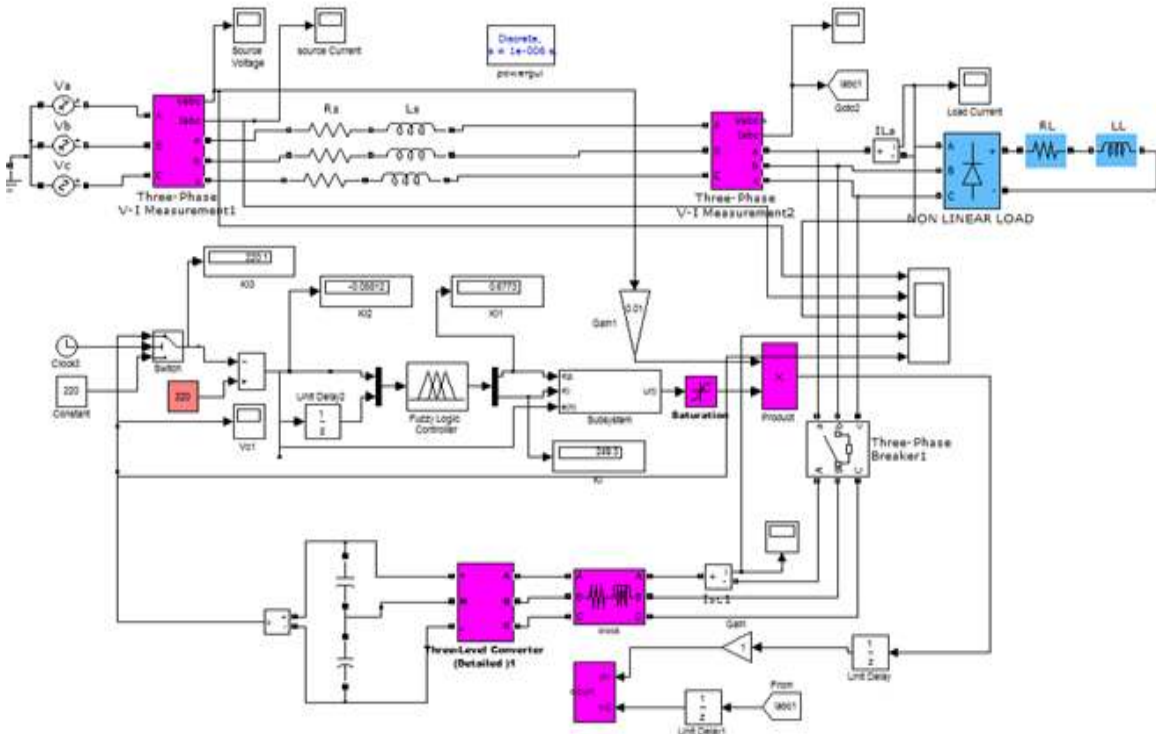


Fig. 7: Simulation model of shunt active power filter

and three phase three level diode clamped inverter is used. Shunt active filter is connected at the point of common coupling. The simulation parameters are used for the proposed system as follows: Input source peak to peak voltage is 100 V, 50 Hz and source impedances are $R_s = 0.1 \Omega$ and $L_s = 0.002$ H. The resistance and inductance value for the filter network are $R_c = 0.1 \Omega$ and $L_c = 0.66$ mH, respectively. The non Linear Load used for the simulation model are $R = 15 \Omega$ and $L = 40$ mH connected with a bridge rectifier circuit. The value of the capacitor used in DC link is 4400 μ F and DC reference voltage is 220 V. The reference current is generated through the fuzzy logic and PI technique. The PWM pulses for the inverter can be obtained from the sampled reference phase voltage magnitudes as in the case of conventional space vector PWM.

Steady state performance of SAPF: The simulation model is presented in Fig. 7. Owing to the presence of non linear load connected with the SPAF, the source current waveform becomes nonlinear and the total harmonic distortion is higher and its value is 22.64%. During the period ($0 \leq t \leq 0.04$) sec the filter circuit is not connected and the therefore the power factor of the system is 0.910. At time $t \geq 0.04$ sec the filter circuit is enabled, the input source current is found to be sinusoidal and the capacitor voltage reaches the steady state value and the THD value is reduced to 1.87%. The required reactive power is supplied at the point of common coupling after the SAPF is on and the

power factor is found to be 0.997. The simulation results of source voltage, source current, load current, filter current and capacitor voltage are presented with and without SAPF is shown in Fig. 8a to e. The harmonic spectrum with and without SAPF is presented in Fig. 9 and 10, respectively.

Dynamic performance of SAPF:

Increasing load with balanced supply: The performance of SAPF is tested with different load conditions. Initially the load on the SAPF system is kept at 0.564 kW during the time ($t = 0$ to 0.15) sec. The SAPF is switched on at $t = 0.04$ sec and the load is added to 800 kW at $t = 0.15$ sec. The load is further increased to 1.07 kW at $t = 0.25$ sec. The values of supply currents of a, b and c phases are 29.5, 30.5 and 29.8 A, respectively. The input supply rms phase voltage is kept balanced at 70 V and the dc-link voltage across capacitor is maintained at 220 V. It is observed that, waveforms of source currents are sinusoidal and balanced even if load currents are unbalanced and non-sinusoidal. The simulation results of source voltage, source current, load current, filter current and capacitor voltage are presented with and without SAPF is shown in Fig. 11a to e.

Increasing load with unbalanced supply: The unbalance supply is created by increasing the input supply rms phase (Ph-a) voltage is 92 V and other two phases b and c are kept constant as 70 V. The same

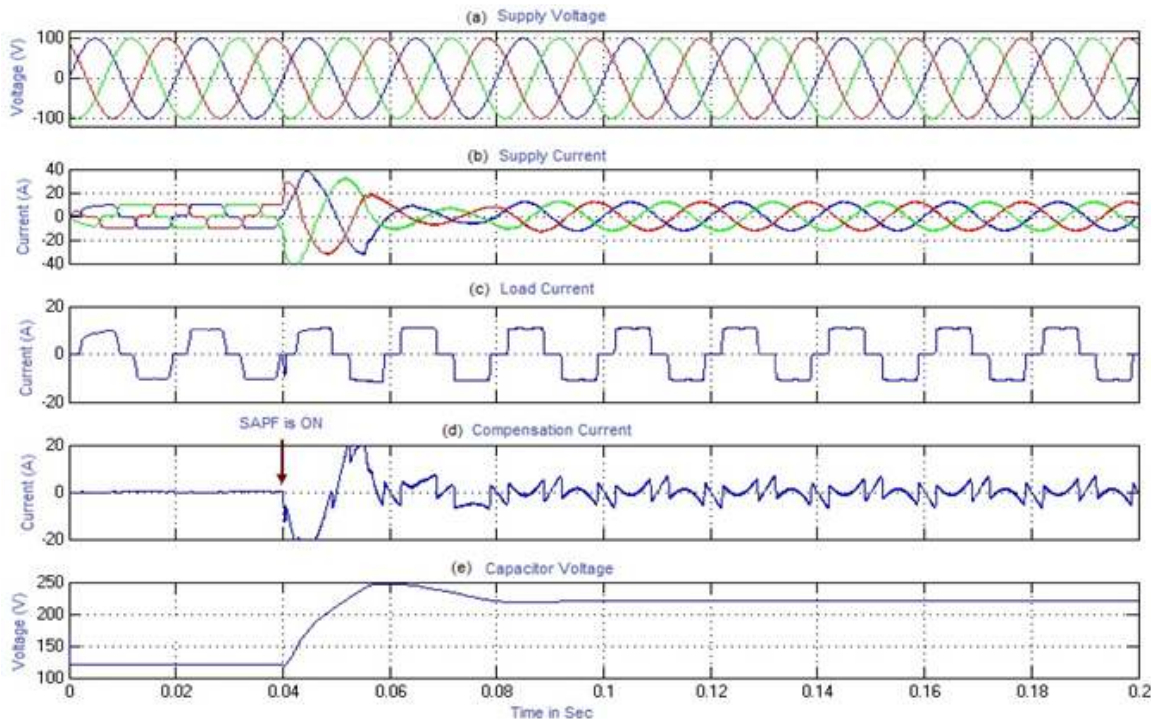


Fig. 8: Simulation outputs for static load conditions, (a) supply voltage, (b) supply current, (c) load current, (d) filter current, (e) capacitor voltage

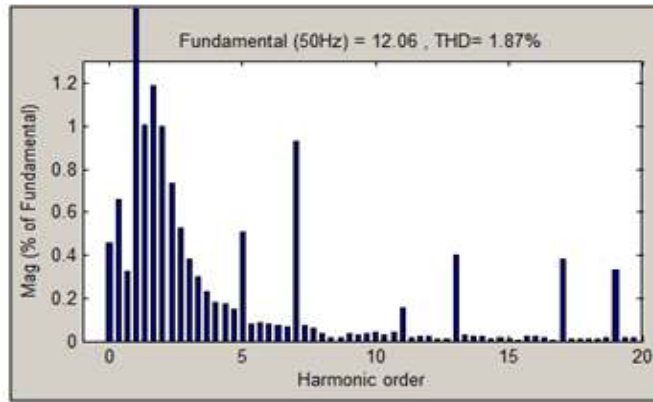


Fig. 9: Harmonic spectrum with SAPF

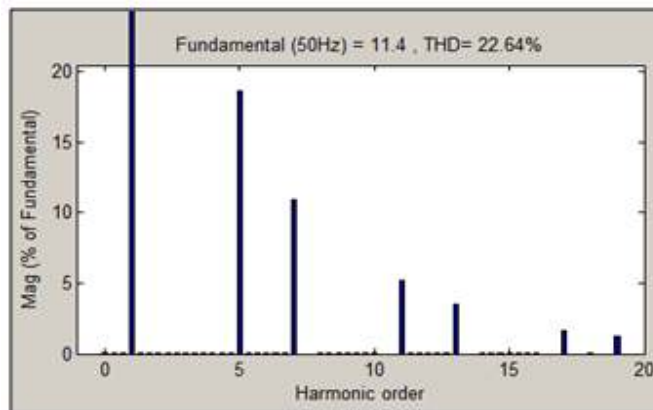


Fig. 10: Harmonic spectrum without SAPF

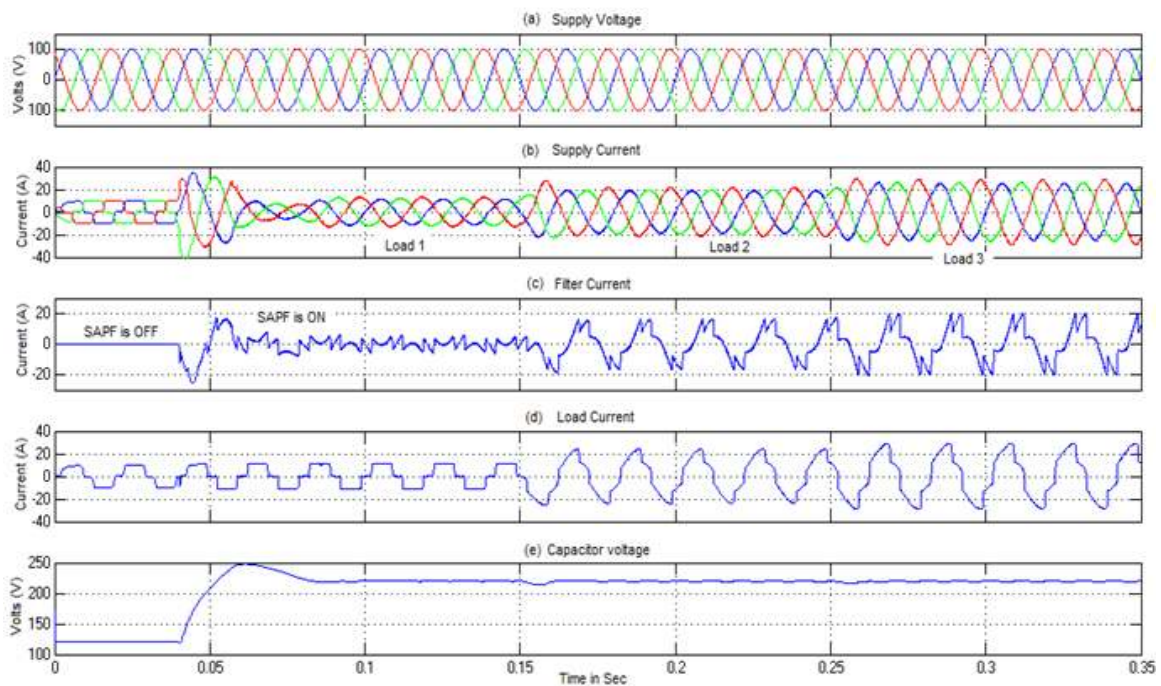


Fig. 11: Simulation outputs for dynamic load conditions-increasing load with balanced input supply, (a) supply voltage, (b) supply current, (c) load current, (d) filter current, (e) capacitor voltage

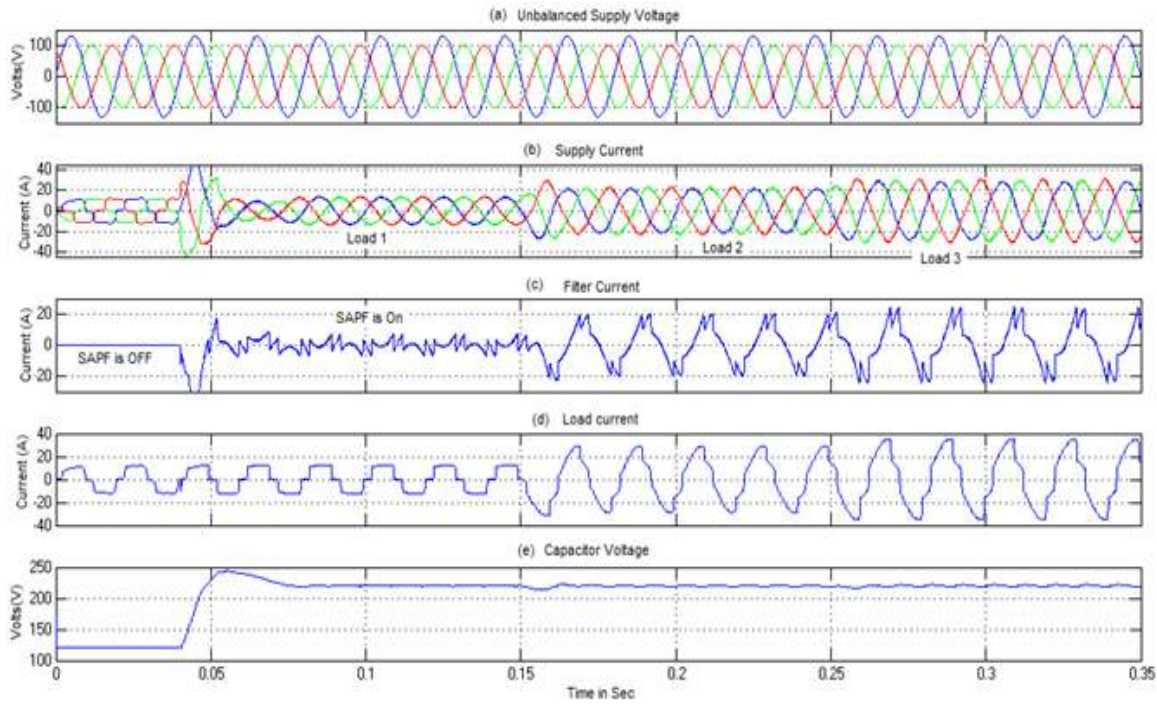


Fig. 12: Simulation outputs for dynamic load conditions-increasing load with unbalanced input supply, (a) supply voltage, (b) supply current, (c) load current, (d) filter current, (e) capacitor voltage

Table 5: Comparison of results

		Proposed PI-FLC controller								
		Static conditions			Dynamic conditions					
		With balanced load			With increasing load and balanced supply			With increasing load and unbalanced supply		
		Ph- a	Ph-b	Ph-c	Ph- a	Ph-b	Ph-c	Ph- a	Ph-b	Ph-c
Voltage at pcc V_{ms}		70.000	70.000	70.000	70.0000	70.000	70.000	92.0000	70.000	70.000
Supply current (A), I_{rms}		12.000	12.000	12.000	29.5000	30.500	29.800	30.5000	31.000	30.800
Settling time		0.030 sec			0.0320 sec			0.0350 sec		
K_p		0.675			0.6669			0.6866		
K_i		246.900			239.5000			255.4000		
% THD	Without	22.640	22.640	22.640	22.6400	22.640	22.640	24.3900	24.390	24.390
(supply current)	With	1.870	1.870	1.870	2.0900	2.090	2.090	2.1700	2.170	2.170
Power factor	Without	0.930	0.930	0.930	0.9520	0.952	0.952	0.9450	0.945	0.945
	With	0.997	0.997	0.997	0.9950	0.995	0.995	0.9890	0.989	0.989

environment loaded conditions it is observed that the source currents of Ph-a, Ph-b, Ph-c are well balanced with values of 30.5, 31 and 30.8 A, respectively and the THD of source currents is found to be 2.17%. Figure 12a to e shows that the source voltage, source current, filter current, load current and capacitor voltage with and without SAPF.

The performance of SPAF using fuzzy logic controller and PI controller is best suitable for static and dynamic conditions with balanced and unbalanced supply. The conjunction of fuzzy logic controller and PI controller is automatically tuned the required reference current to the multilevel inverter so that the nature of the source currents is always be sinusoidal and balanced. Table 5 gives the comparison of voltage at

PCC, value of source current, THD of source current, settling time of DC capacitor, power factor, appropriate tuning values of K_p and K_i for the static and dynamic conditions of performance of SAPF.

CONCLUSION

In this study, a conjunction of PI and FLC logic technique have been projected to estimate the required reference current for the proper function and controlling the DC voltage across the capacitor of Three Level Voltage Source Inverter. The supply current THD is observed without SAPF is 22.64% and it is well reduced below the limit of 5% provided in standard IEEE519 after switched SAPF at $t = 0.04$ sec. The DC

voltage regulation is settled after few cycles. In this method, the K_p and K_i values are automatically tuned by error values with the help of fuzzy logic controller so that the performance of the active filter is efficient on both static and dynamic conditions. It is observed that THD of supply current and settling time is quite low and reactive power is also compensated which in turn power factor of the system is close to unity.

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