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Research Article

VLSI Architecture Using a Modified SQRT Carry Select Adder in Image Compression

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Abstract: Designing a compressor with the parameters such as power, delay and area are most considerable metric in VLSI design. Compression process plays a vital role in image processing and the main building block is the multiplier. Image conversion is done in MATLAB and the compression is done using VHDL in VLSI. Finally, the compression ratio is predicted using MATLAB. CPA (Carry Propagation Adder) and CSA (Carry Save Adder) occupies more chip area than other adders. To overwhelm the problem this study proposes a modified Square Root Carry Select Adder (SQRT CSLA) in Dadda multiplier used in compression system. The modified SQRT CSLA performs faster than other adders and power consumption is low. Compression techniques pay more attention in image processing. In this study 4-2 compressor is employed to reduce the complexity.

Keywords: Dadda multiplier, image compression, modified Square Root Carry Select Adder (SQRT CSLA)

INTRODUCTION

In recent communication technology Very Large Scale Integration (VLSI) circuits in low power becomes very important to design a high performance and convenient devices. The parameters such as speed, cost and area become most important parameters in VLSI. These parameters play a vital role in performance. More focus is given for consumption of low power to achieve high speed in low cost to occupy small area. Day by day the importance of low power VLSI is increasing because of its performance. In image processing it finds a strong application hence the VLSI tool is not a general purpose tool for systems. Imaging and video applications becomes fastest growing sector in day today life. It finds more application in medical science, machine vision, digital cameras, HDTV, security surveillance and set top box. Most powerful technique is image compression in image processing. The adder used in the compressor is to reduce the storage space required and to increase the data bit transfer rate. Preserving the image quality by increasing the reliability is preferred. It also find its application in nanoscale technology because of its higher speed it has become more important.

Multiplication is the fundamental for all mathematical operations and finds its application in computation system and graphics in digital computer and in signal processing systems. Apart from addition and subtraction, more processing time and hardware resources are required for it. In VLSI technologies, there is a need to develop the chip design tools for continuous development. An algorithm was proposed (Pekmestzi, 1999) based on a different mechanism which consists of one bit of the multiplier and one bit of the multiplicand and both can be interchanged. The operand is used as a bit in each step. The multiplier circuit design is more complex since it consists of number of transistors and gates in CMOS VLSI technology.

The compression of fractal image weaknesses was analyzed. The rate-distortion performance was encoded and decoding speed by considering cluster centres using Mean Shape-Gain Vector Quantization (MSGVQ) code book method (Raouf and Dietmar, 2000). This method is not competitive with the state-of-the-art wavelet coders and does not generate an embedded code because it allows scalability and progressive transmission.

A low power multiplier by booth algorithm (Chen *et al*., 2003) was designed to reduce the implementation complexity. The proposed column based, row based and hybrid based multipliers can design dynamic-range determination units. But reduction in switching activity is difficult. A new methodology was proposed with XOR and exclusive NOR for 4-2, 5-2 compressor (Chip-Hong *et al*., 2004) consumes low power and acquires sufficient drivability on CMOS technology at very low voltages. The 4-2 compressors display better efficient power and 5-2 compressor composed to carry generator module. Its operation is reflected in a tree structured multiplier.

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Two methods in lossy compression technique (Wei *et al*., 2006) were developed using JPEG 2000 for efficient entropy encoding and rate control. The specified bit rate distortion is minimized by rate control method for the specified bit rate. The authors proposed a Greedy Heap based Rate-Control algorithm (GHRaC), by implementing a greedy marginal analysis method to achieve efficient post compression rate control using the heap sort algorithm and for entropy coding an Integrated Rate-control and Entropy-Coding (IREC) algorithm reduces the complexity of computation. An automatically-determined Region of Interest (ROI) (Chen and Chih-Chang, 2007) scheme embedded in JPEG 2000 in video compression employed with Lagrangian multiplier to optimize ROI masks in order to reduce distortion. Locating ROI in an image with no obvious object or with complex background becomes semi-automatic.

In this study a new technique is discussed to reduce delay and low power consumption for image compression in which an image is converted to hexadecimal from decimal using MATLAB. The compression is carried out in VLSI in which the 4-2 compression unit consists of a modified SQRT Carry Select Adder (CSLA). The modified SQRT CSLA (Square Root Carry Select Adder) adder uses 16 bit.

PROPOSED METHODOLOGY

An image is randomly selected in which the image is compressed, to be compressed the process is carried out in two steps. The first step consists of a converting the pixel values in the image to the hexadecimal values, which is executed in MATLAB. The second step is to compress the hexadecimal values using 4-2 compressor technique in VHDL. The third step is to calculate the compression ratio. The block diagram for the proposed study is given in Fig. 1.

Image: A RGB image of 8 bit is selected and it is converted into gray scale. RGB stands for red, green and blue. It is represented from 0 to 255 in decimal. Gray scale image holds the information about intensity of each pixel. Pixel is the fundamental unit in a computer image and depends on resolution of an image. An image pixel has a value "0" for black and value "1" or "255" for white where the intensity level become weakest and strongest, respectively. These images are stored in a format like UINT8, UINT16, UINT32 and UINT64, double and single, JPEG, PNG, GIF, TIF, BMP, TIFF etc. Most commonly used image file extensions are .jpeg, .jpg, .bmp, .png, .tiff, .tif, .gif etc. UINT8, UINT16, UINT32 and UINT64 denotes unsigned 8, 16, 32 and 64 bit integer, respectively. This technique makes use of unsigned 8 bit integer.

Hexadecimal: Hexadecimal is one of the numeral system. It uses the standard decimal from 0 to 9 and for 10 to 15 it takes English alphabet from A to F or a to f. A nibble is said to have one hexadecimal digit. 00 to FF represents two hexadecimal values. Since it is user friendly it finds more application in computer by programmers, system designers and digital electronics. Initially the uncompressed image of larger quantity in decimal is converted to hexadecimal which is executed in MATLAB. For image compression using VLSI design the 4-2 compressor receives hexadecimal as input for further process in order to transfer or store the image data efficiently.

Compressor: A 3-2 compressor (Siliveru and Bharathi, 2013) is used in multiplier which has 3 inputs with 2 outputs (Fig. 2). A 3-2 static mirror compressor is employed to connect slow input with fastest output (Hsu *et al*., 2006). In this study a 4-2 compressor is utilized which compresses four partial products. The 4-2 compressor (Momeni *et al*., 2015) consists of series connected of two full adders which is designed with XOR, XNOR gates and Multiplexers. In the proposed

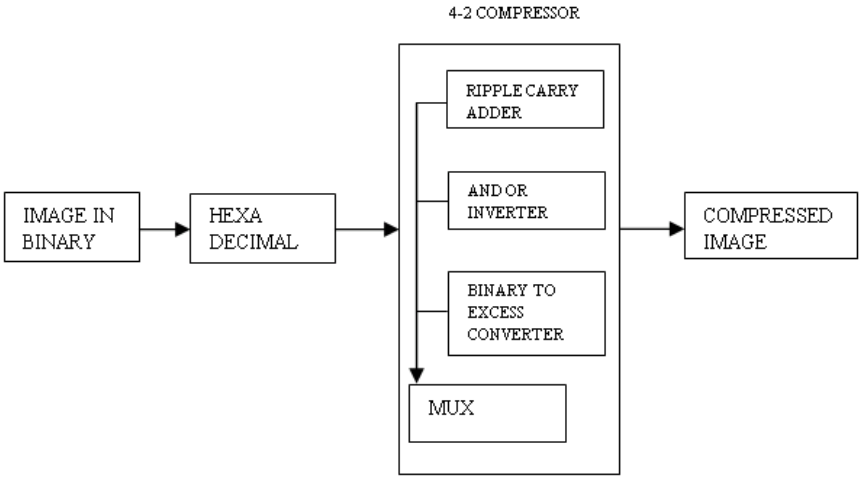

Fig. 1: Proposed block diagram

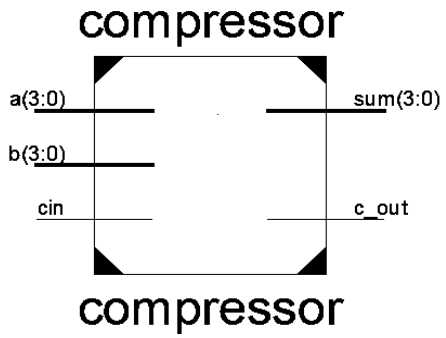

Fig. 2: Schematic diagram of 4-2 compressor

method the 4-2 compressor is designed with modified SQRT carry select adder. The proposed 4-2 compressor is shown in Fig. 3 which consists of 16 bit modified SQRT CSLA. It designed with Ripple Carry Adder (RCA) and OR Inverter (AOI), Binary to excess-1 converter and multiplexers.

Ripple carry adder: A 16 bit ripple carry adder is employed in this method which consists of several full adders to build a logical unit adding n bit numbers. A logic circuit in which output of an adder is fed as input to next adder and each carry bit gets rippled into the next stage is a ripple carry adder. Its valid only when carry in occurs. RCA in this study perform calculation to get correct sum and carry.

AND OR inverter: A simple AND OR inverter to calculate sum and carry is constructed of one NOR gate with two AND gates. More transistor gates are needed to implement AND, OR and NOT functions separately which consumes more power, high fabrication cost, reduced speed and more space. AOI in this modified SQRT CSLA is to calculate final sum and output carry becomes more efficient.

Binary to excess-1 converter: Binary to Excess-1 Converter consists of many full adders and half adders. The modified CSLA using BEC use AOI instead of either full adder or half adder which reduces area, power consumption and speed up the operation in calculating carry and sum.

Multiplexer: A multiplexer also known as data selector has a select line to carry analog or digital signals. A select line carries one signal. For 2:1 multiplexer 1 select line is needed. Multiplexer reduces integrated circuit package number in turn reduces the cost.

SIMULATION RESULTS

Input image: Figure 4 is taken as input for the system. The size of the input image is 8 KB (8200 bytes).

4-2 compressor: The Dadda multiplier designed using modified SQRT CSLA has been developed using VHDL and synthesized in Xilinx ISE14.2. Figure 5 shows RTL schematic diagram of 4-2 compressor.

Comparing the delay attained by Array, Booth, Vedic multipliers (Sumit and Deepak, 2010) with proposed Dadda multiplier during compression of a 16×16 image is shown in Table 1. The delay attained by proposed Dadda multiplier is 18.641 nsec delay.

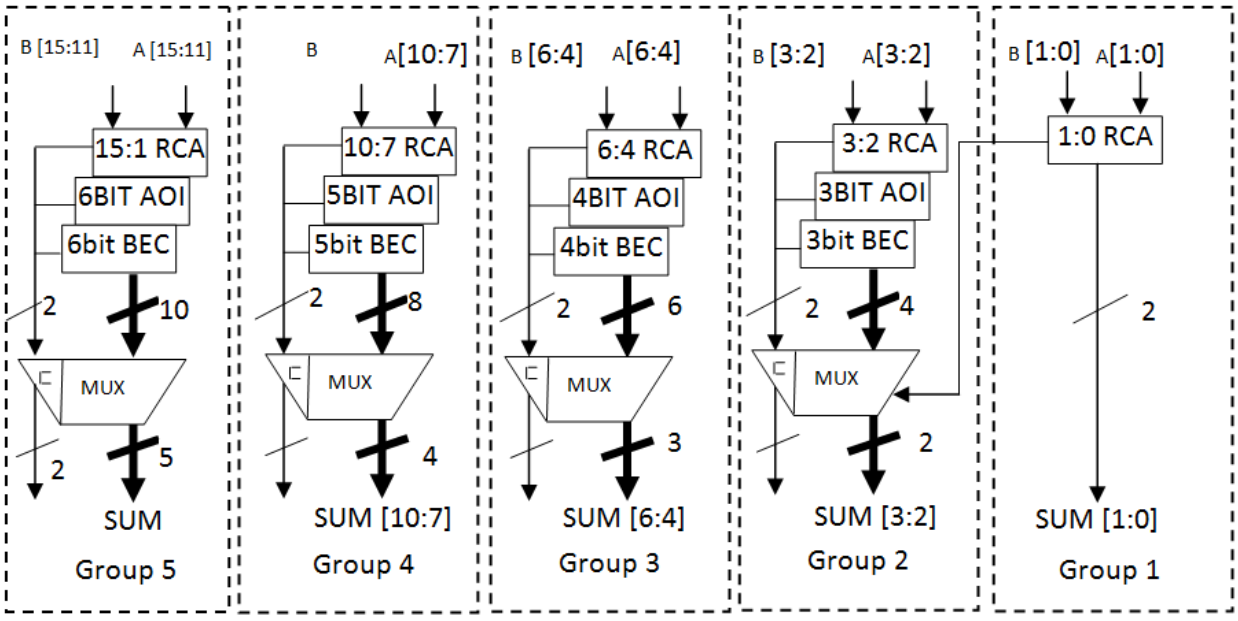

Fig. 3: A 4-2 compressor

Fig. 4: Input image

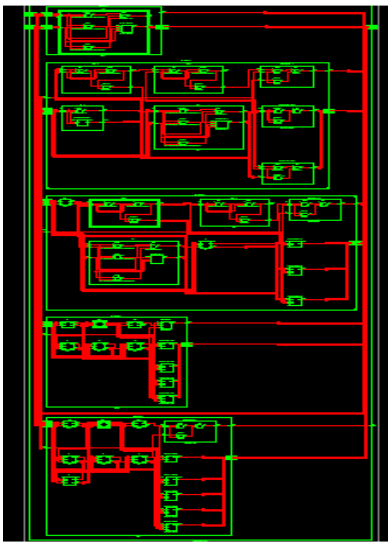

Fig. 5: RTL schematic diagram of 4-2 compressor

Table 1: Comparison between multipliers with delay (nsec)

Name of multiplier	Array multiplier	Booth multiplier	Vedic multiplier	Proposed dadda multiplier
Delay (nsec) 16×16 bit	92.034	232.021	39.023	18.641

Table 2: Approximate multipliers and their features

Design	Feature
Multiplier 1	Design 1 in all columns
Multiplier 2	Design 2 in all columns
Multiplier 3	Design 1 in LSBs and exact compressor in MSBs
Multiplier 4	Design 2 in LSBs and exact compressor in MSBs
Multiplier 5	Approximate 2×2 multiplier blocks

Table 3: Delay improvement in reduction circuitry design

Design	Improvement (%)
Multiplier 1	3.38
Multiplier 2	5.52
Multiplier 3	3.24
Multiplier 4	4.51
Multiplier 5	0.00

Table 4: Macro statistics

XOR utilization	CSA	Proposed modified SQRT CSLA
Total XOR	30	16
1-bit XOR2	18	4
1-bit XOR3	12	12

Table 2 shows the design and features of multipliers in each group shown in Fig. 2.

The reduction in circuitry for delay improvement is shown in Table 3.

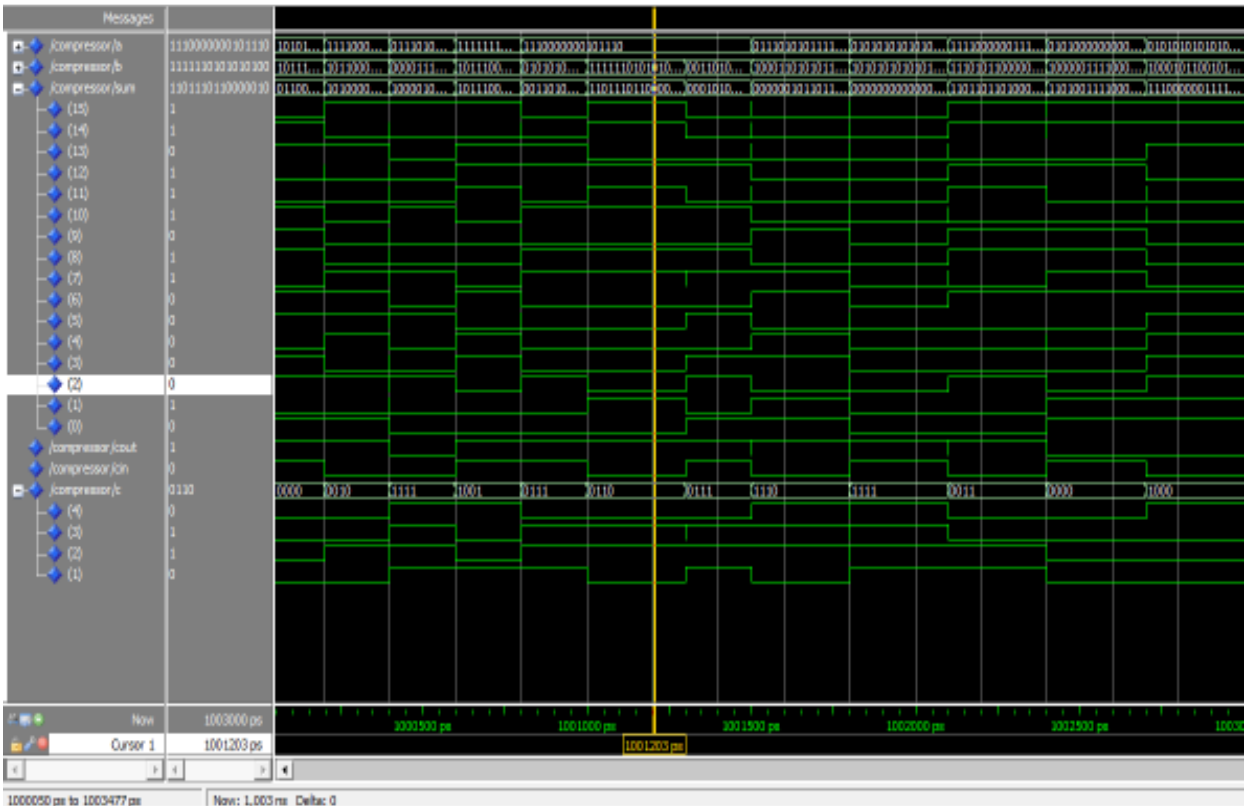

Fig. 6: Simulation result of compressed image in model SIM

Fig. 7: Output image

The proposed modified SQRT CSLA utilizes XOR gate comparatively less with Carry Save Adder (CSA) is shown in Table 4.

The simulation result of a compressed image is shown in Fig. 6 and the delay occurred by the proposed method seems to be better when compared with other multipliers (Sumit and Deepak, 2010).

Output image: The output image obtained is 5.34 KB (5478 bytes) is shown in Fig. 7. The compressed ratio is 66.80%.

CONCLUSION

An image is randomly selected to be compressed in two steps to calculate delay time. The first step is to convert the pixel values in the image to the hexadecimal values, which is executed in MATLAB. The second step is to compress the hexadecimal values in VHDL. In this proposed method image compression is performed by 4-2 compressor technique using modified SQRT CSLA. The delay metric is measured and compared with other multipliers and the simulation result shows the measured performance metric is more efficient than the compared existing multipliers.

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