Research Journal of Applied Sciences, Engineering and Technology 12(3): 339-346, 2016
DOI: 10.19026/rjaset.12.2341
ISSN: 2040-7459; e-ISSN: 2040-7467

Submitted: August 21, 2015 Accepted: September 11, 2015 Published: February 05, 2016

Research Article

VLSI Based New Pipelined Architecture Design for Radix-2 FFT

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Abstract: Improvements of wireless digital communication application have large demands on Signal Processing operations. Frequency transformation techniques are recognized as high potential in the field of digital communication. In this study, a new pipelined based Fast Fourier Transformation (FFT) architecture is designed for performing frequency transformation techniques. Delay Feedback (DF) and Delay Commutator (DC) based structures are widely used to perform frequency transformation techniques. A new architecture called "Single path Delay Commutator (SDC)" is introduced in this study to estimate the frequency representation of discrete time input samples. Further, Single path Delay Feedback (SDF) structures are utilized in the final stage of SDC architecture for obtaining response in bit reversing order. Proposed new architecture is named as "Radix-2 Mixed SDC-SDF FFT" To increase the processing speed of FFT architectures, pipelining techniques is introduced in the proposed Mixed SDC-SDF FFT architecture. Hence, the proposed new architecture named as "Pipelined Radix-2 Mixed SDC-SDF FFT". The performance evaluation of proposed architecture is determined through Very Large Scale Integration (VLSI) System design environment. Less area utilization, low power consumption and high speed are the main concerns in VLSI System design environment. Hence, the aim of proposed new architecture is to reduce the hardware architecture, power consumption and increasing both speed and throughput of the system. Proposed new Pipelined Radix-2 Mixed SDC-SDF FFT architecture offers 17.6% reduction of Slices, 21.65% reduction of LUTs, 45.92% reduction of maximum combinational delay and 24.22% reduction of power consumption than best existing Radix-2 SDF FFT structure.

Keywords: Fast Fourier Transformation (FFT), Inverse Fast Fourier Transformation (IFFT), Multi-path Delay Commutator (MDC), Single path Delay Commutator (SDC), Single path Delay Commutator-Single path Delay Feedback (SDC-SDF) FFT, Single-path Delay Feedback (SDF) FFT, Very Large Scale Integration (VLSI) system

INTRODUCTION

Fast Fourier Transformation (FFT)/Inverse Fast Fourier Transformation (IFFT) are the best frequency transformation techniques in wireless digital communication system. Orthogonal Frequency Division Multiplexing (OFDM) System is one of the best digital communication mechanism in which FFT/IFFT techniques are used to perform frequency transformation techniques. FFT is used for converting the time domain signals into frequency domain signals and IFFT is used for converting the frequency domain signals into time domain signals. Normal Radix-2 FFT architecture has more computational path to implement the conversion techniques. In theoretically, worst case performance of FFT processors is represented as in terms of O ($\log_2$ n). To reduce the complexity of dataflow, Single path Delay Feedback (SDF) and Multi-path Delay Commutator (MDC) structures have been suggested by large endeavours (Garrido *et al*., 2013; Arunachalam and Raj, 2014). Both SDF and MDC architectures have different types of advantages in terms of different kind of VLSI concerns. In case of SDF FFT structure, high speed operation can be achieved due to parallel structures. On the other hand, MDC structure utilizes less hardware and power consumption than SDF structure. Hence, MDC architecture has been preferred for performing frequency conversion process. But, delay feedback structure has somewhat easy to design than multi-path delay commutator structures. In every stage of FFT operations, delay feedback and delay commutator structure has been used for providing pipelining technique.

In order to improve the architecture of SDF, Single path Delay Commutator (SDC) architecture is preferred in this research work. In final stage of SDC circuit, SDF circuit is used in this study. Hence, Proposed a new architecture is referred as Radix-2 Mixed SDC-SDF FFT. In addition, Pipelining technique is to improve the architectural performances of Radix-2 Mixed SDC-SDF FFT.

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LITERATURE REVIEW

Fast Fourier Transformation (FFT) technique is widely used in OFDM based digital communication systems for analyzing the spectrum characteristics of digital inputs. But FFT structure has more computational path to determine the spectrum characteristics of digital inputs. In order to overcome this problem, VLSI based Serial Parallel FFT Processor has been introduced (You and Wong, 1993). Parallel FFT processor can be executed within a clock cycle, but it consumes large amount of hardware elements like adder and complex multiplier. Hence, Serial FFT Processor has been preferred in the past to implement the FFT function. Pipelined function of FFT Processors has been briefly explained in Cortés *et al*. (2009). For OFDM applications, both real valued and complex valued FFT processors are essential for estimating the spectrum characteristics. Real Valued and Hermitian Symmetric FFT processors have been designed in Salehi *et al*. (2013). Bit Reversing property of FFT functions is very important for matching frequency characteristics. In order to meet this requirement, Bit-Reversal circuit for MDC structures have been designed in Chen *et al*. (2014). In dataflow path of FFT structures, complex multiplier structures has utilize large hardware than other parts. Hence, taking more concentrations on twiddle factor multiplier in FFT structure is very important. A lot of research work has been worked on complex multiplier structure of FFT structures. Two types of Complex Multiplier structures has been widely used for Sharing the same hardware and to improve the architectural performances in terms of VLSI Concerns, they are Reconfigurable Complex Multiplier (RCM) and Bit Parallel Multiplier (BPM). The procedures for sharing the twiddle factor multiplication architecture of MDC FFT have been briefly explained in Yang and Lee (2014).

Further to minimize architectural dataflow of FFT processors, Pipelined Radix 2^k Feedforward FFT architectures have been designed in Garrido *et al*. (2013). In this design, 688 hardware Slices have been utilized and 25ns delay has been consumed to perform the frequency conversion process. Next to Architectural improvement, Reconfigurable FFT architectures have been designed by large endeavours to improve the adaptation techniques (Nair, 2015; Joshi, 2015). On the other hand, Memory reduction techniques are also very important in the design of FFT Processors. In order to fulfil this requirement, Memory Reduction based FFT implementation circuit has been designed in Wang *et al*. (2007). Finally different type of FFT structures have been analyzed and compared in Sharad and Jyoti (2015). In Arunachalam and Raj (2014), theoretical gate count calculation has been estimated as 2083 for implementing 8-point FFT function. But, Practically it utilizes 88 hardware Slices. This is the best architecture as identified in Sharad and Jyoti (2015). In order to differentiate the entire architecture, SDC architecture has been introduced in Wang *et al*. (2015). This architecture consumes 25ns for executing 8 point FFT function. The architecture of Wang *et al*. (2015) is considered in this study for improving the architecture performance further.

RADIX-2 FFT STRUCTURE

Discrete Fourier Transformation (DFT) has been used for calculating the frequency representation of digital signals. In general, DFT of N-point discrete time signal is represented as follows:

$$X_k = \sum_{n=0}^{N-1} x_n W_N^{nk} \quad 0 \le k \le N-1 \tag{1}$$

where, X_k is the DFT (frequency) representation of discrete signal x_n, W_N^{nk} denotes the twiddle factor and N represents the number of points. The average worst case performance of Radix-2 DFT Processor has been denoted as O (n^2). Due to intensive computational requirements, straightforward implementation of this algorithm is impractical. Hence, to reduce the complexity of DFT Process, FFT transformation techniques has been introduced. The average worst case performance of Radix-2 FFT Processor has been denoted as O ($\log_2 n$). In general two types of FFT have been used for performing frequency transformation techniques. One of them is Decimation in Time (DIT) FFT and another one is Decimation in Frequency (DIF). In DIT FFT, input is given to Bit-Reversing order and output is obtained as Normal order, but in DIF FFT, input is given to Normal order and output is obtained as Bit-Reversing order. For instance, the Signal Flow Graph (SFG) of 16-point DIF FFT has been illustrated in Fig. 1.

In every stage of FFT Processor, first half of N point input data is processed with second half of N point input data. In second half of the input data, it must be need to multiply the subtracted data with corresponding twiddle factor values. The processing of every stage has been represented as follows:

$$X[2k] = \sum_{n=0}^{\frac{N}{2}-1} \left(x[n] + x\left[n + \frac{N}{2}\right] \right) W_{N/2}^{kn} \tag{2}$$

$$X[2k+1] = \sum_{n=0}^{\frac{N}{2}-1} \left(x[n] - x\left[n + \frac{N}{2}\right] \right) W_N^n W_{N/2}^{kn} \tag{3}$$

From Eq. (2) and Eq. (3), it is clear that the computational path of Normal N-point FFT has been increased when increasing the input points. Hence, therefore Normal SFG based N-point FFT architecture is not suitable for determining the frequency transformation technique. Therefore, Serial inputs

based FFT architecture is preferred in this study to implement the function of 16 point FFT.

RADIX-2 SINGLE PATH DELAY FEEDBACK STRUCTURE

Radix-2 Single path Delay Feedback (R2SDF) FFT is a serial FFT Processor which provides high speed operation. In R2SDF FFT, inputs are given into serial manner. The architecture of 16 point R2SDF FFT structure is illustrated in Fig. 2.

Both Normal Radix-2 FFT and Radix-2 Single path Delay Feedback (R2SDF) FFT has same stages to implement the 16 point FFT, but dataflow architecture is different. In R2SDF FFT, single processing element is used in every stage of FFT Processor whereas Normal Radix-2 FFT Processor uses more than five or six processing element. The Processing Element (PE) structure of R2SDF FFT is indicated as "Butterfly" in Fig. 3. In R2SDF FFT, N/2 point input data is sequentially controlled with the help of Flip-Flop (FF) circuit. The PE structure of R2SDF FFT has been illustrated in Fig. 3.

In R2SDF FFT, inputs are given into sequentially and intermediate processes are performed in a parallel manner. Hence, this architecture is referred as "Parallel-Pipelined Architecture". As shown in Fig. 3, inputs are given sequentially and four sequential inputs are processed concurrently with the help of single butterfly (Processing Element) unit. However, this architecture consumes more hardware utilization and power consumption due to utilizing or storing bulk of unwanted intermediate processing digital signals. Hence, more wastage of power consumption is one of the main disadvantages of R2SDF FFT. Hence, to improve the architectural performances of FFT, Mixed

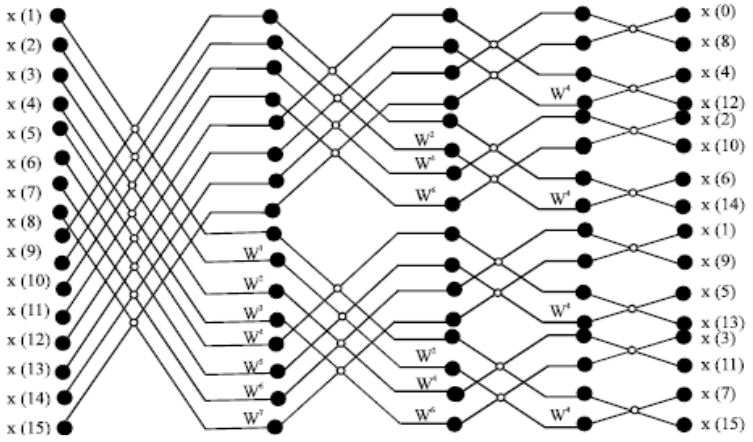

Fig. 1: Signal Flow Graph (SFG) of 16-point DIF FFT

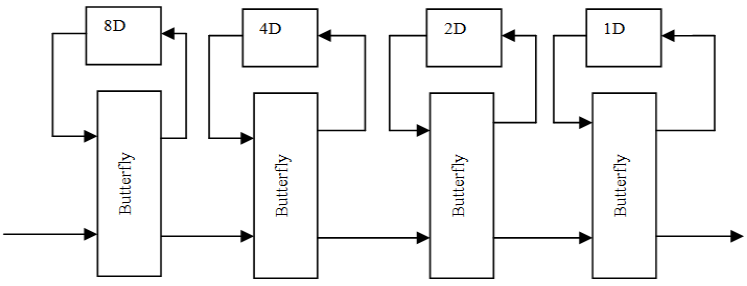

Fig. 2: Architecture of 16-point Radix-2 Single path Delay Feedback (R2SDF) FFT

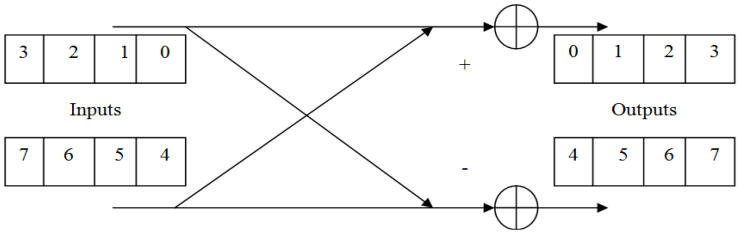

Fig. 3: Processing Element (PE) structure of R2SDF FFT

Single path Delay Commutator (SDC) -SDF architecture has been designed in this study.

PROPOSED PIPELINED RADIX-2 MIXED SDC-SDF STRUCTURE

In this study, architecture of Single path Delay Commutator (SDC) is preferred to reduce the hardware utilization, power consumption and to improve the speed of the processors. Unlike SDF FFT, SDC FFT has more number of single delay commutators within one stage. But in case of SDF FFT, one number of large delay feedbacks is used to perform the functions of FFT. In the proposed technique both SDC and SDF architecture is presented for improving the architectural performances in terms of VLSI main concerns. The architecture of Proposed 8-point Radix-2 Mixed SDC-SDF FFT architecture is illustrated in Fig. 4.

As shown in Fig. 5, both SDC and SDF architectures are used in the proposed design. In the final stage of FFT computation only, SDF procedure is used in proposed design. In the place of multiplier unit, Bit Parallel Multiplier is used to multiply the subtracted data into corresponding twiddle factor values. The architecture of SDC for single stage is illustrated in Fig. 5. Complex input data is considered to perform the FFT function. In every step, there is single delay commutating function has been used to process the appropriate data points. Similarly in every stage, two N/2 delay processing has been made to align data with appropriate clock cycles. The Multiplexer units have been used to provide control signals for performing commutator functions. Further signed addition and signed subtraction units are used to perform accumulation and subtraction functions.

When compared to SDF structure, SDC architecture has more computational paths to perform FFT function. However, Implementation result (Synthesis results) shows that, more reduction of VLSI concerns can be achieved in SDC architecture. This achievement can be obtained due to sharing or utilizing 50% of same hardware resources for computing multiple functions. Full in depth architectural view for proposed Radix-2 Mixed SDC-SDF FFT architecture is illustrated in Fig. 6.

In Fig. 6, Register unit has been added for introducing the pipelining mechanism. In pipelining mechanism, asynchronous effects are eliminated due to pipelining registers. Further final stage of SDF FFT is used to improve the speed of architecture. Finally Bit Reversing Unit (BRU) is used to arrange the input in specified order. The disadvantage of proposed system is only taking 2N clock cycles to generate the output sequentially. Figure 6 is a new architecture of Proposed Pipelined 8-point Radix-2 Mixed SDC-SDF FFT.

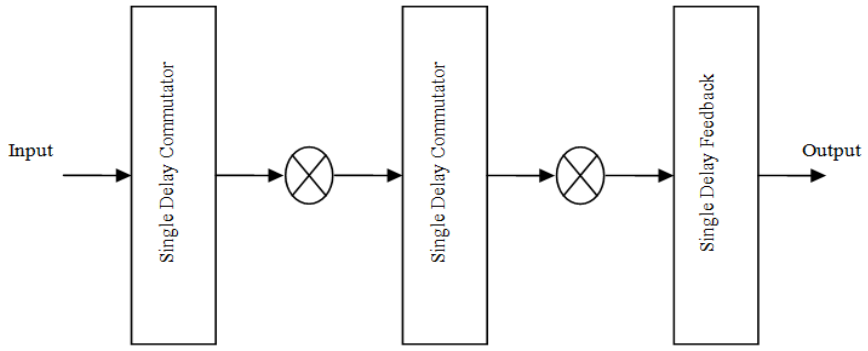

Fig. 4: Architecture of proposed 8-point radix-2 mixed SDC-SDF FFT

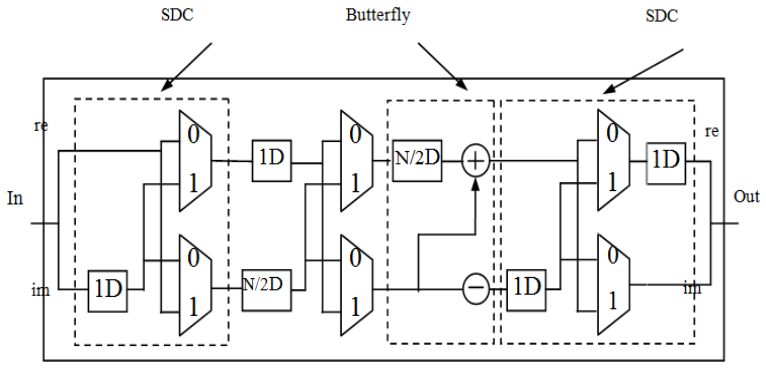

Fig. 5: Architecture of Single path Delay Commutator (SDC)

RESULTS AND DISCUSSION

The design of mixed SDC-SDF FFT architecture has been made by using Verilog Hardware Description Language (Verilog HDL). The simulation results has been evaluated by using ModelSim 6.3C and Synthesis Performances are estimated by using Xilinx 10.1i (Package: pq208, Family: Spartan-3, Device: Xc3s200) design tool. The Simulation result of conventional 8-point R2SDF FFT is illustrated in Fig. 7. Similarly, the

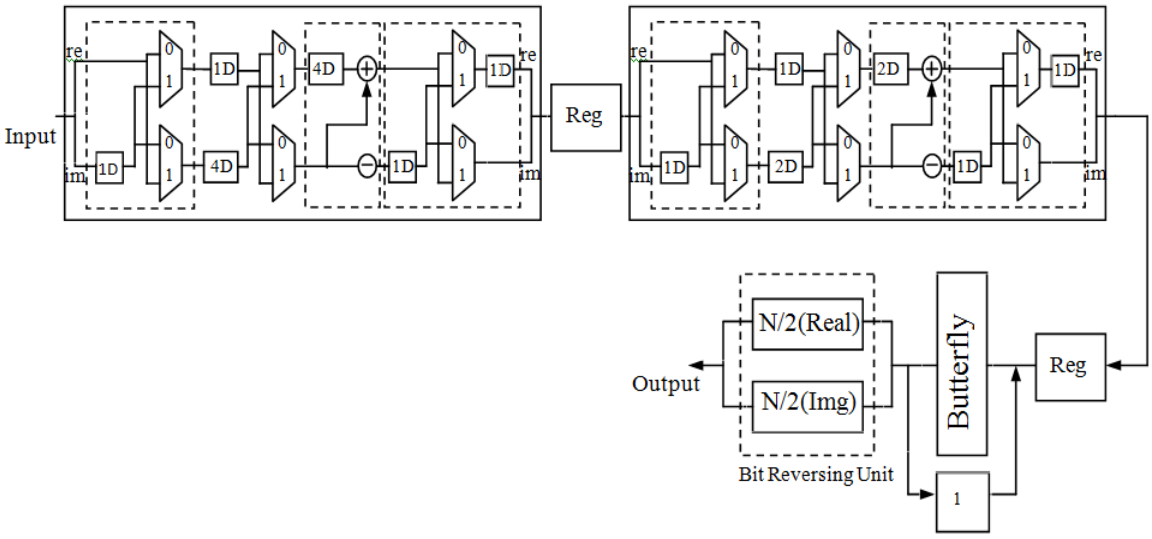

Fig. 6: Full architecture of proposed 8-point radix-2 mixed SDC-SDF FFT

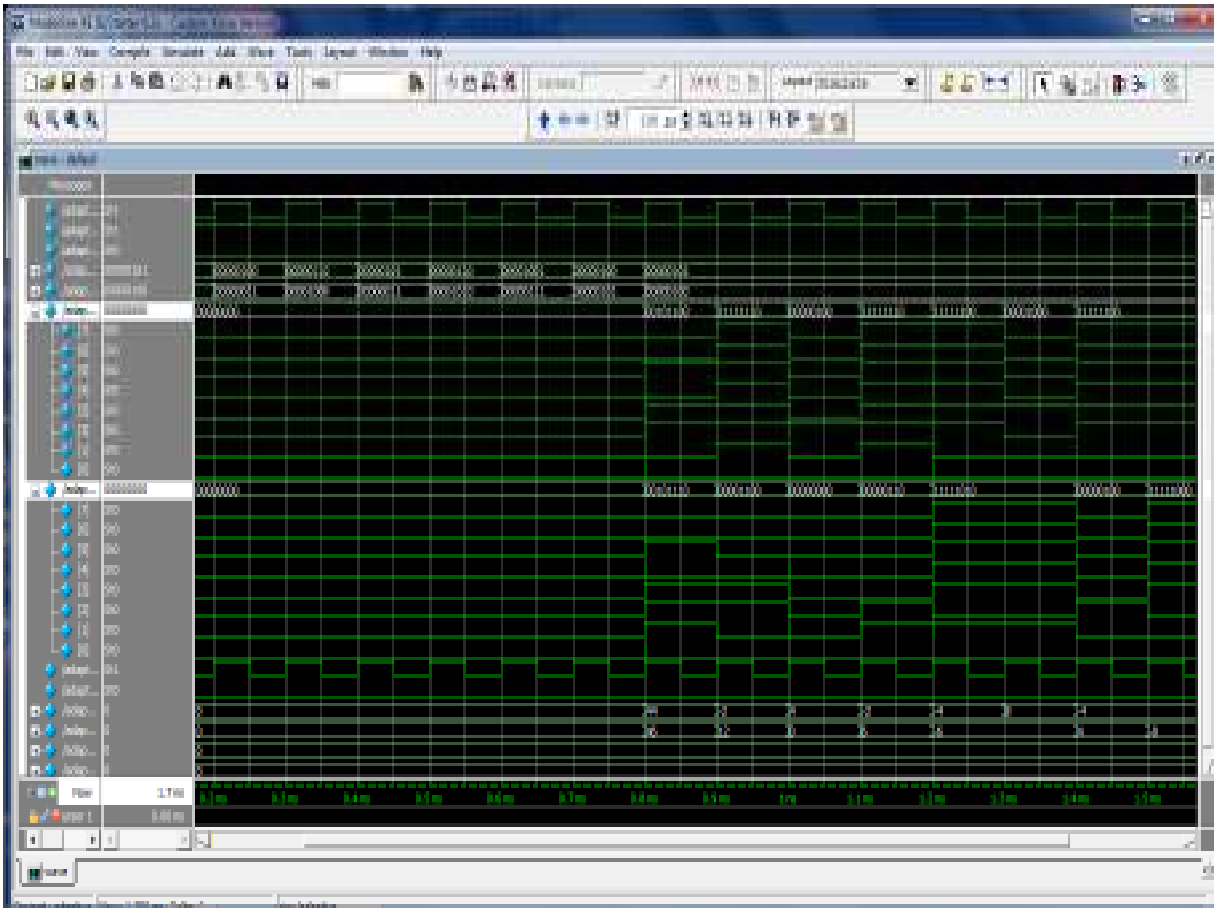

Fig. 7: Simulation result of conventional 8-point R2SDF FFT

simulation result of Proposed Pipelined 8-point Radix-2 Mixed SDC-SDF FFT is illustrated in Fig. 8.

When compared to Fig. 7 (conventional R2SDF FFT), Fig. 8 (Proposed Pipelined Radix-2 Mixed SDC-SDF FFT) takes more clock cycles to provide frequency representation of digital inputs. It is one of the main drawbacks of Proposed System. However, architectural performances of Proposed System have been improved in terms of less Silicon area utilization, high speed and lower power consumption than conventional one. Register Transfer Logic (RTL) view of conventional R2SDF and Proposed Pipelined Radix-2 Mixed SDC-SDF FFT is illustrated in Fig. 9 and 10 respectively.

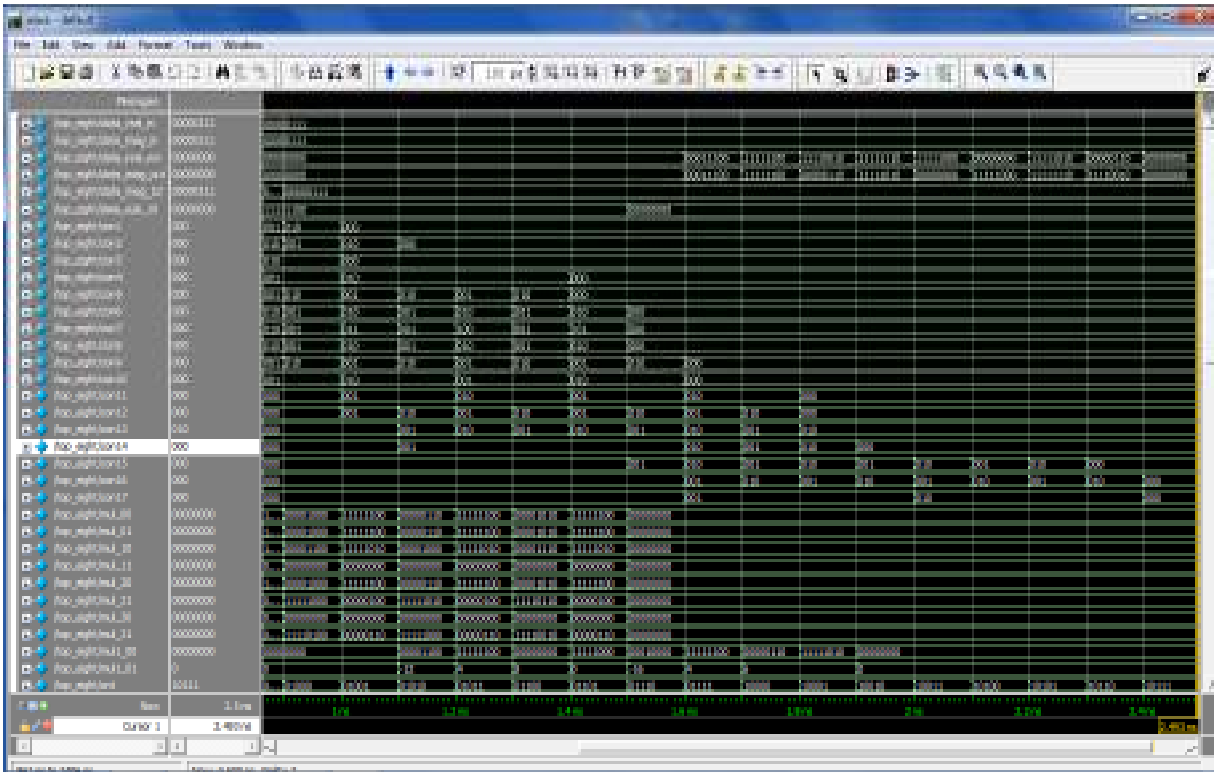

Fig. 8: Simulation result of proposed pipelined 8-point radix-2 mixed SDC-SDF FFT

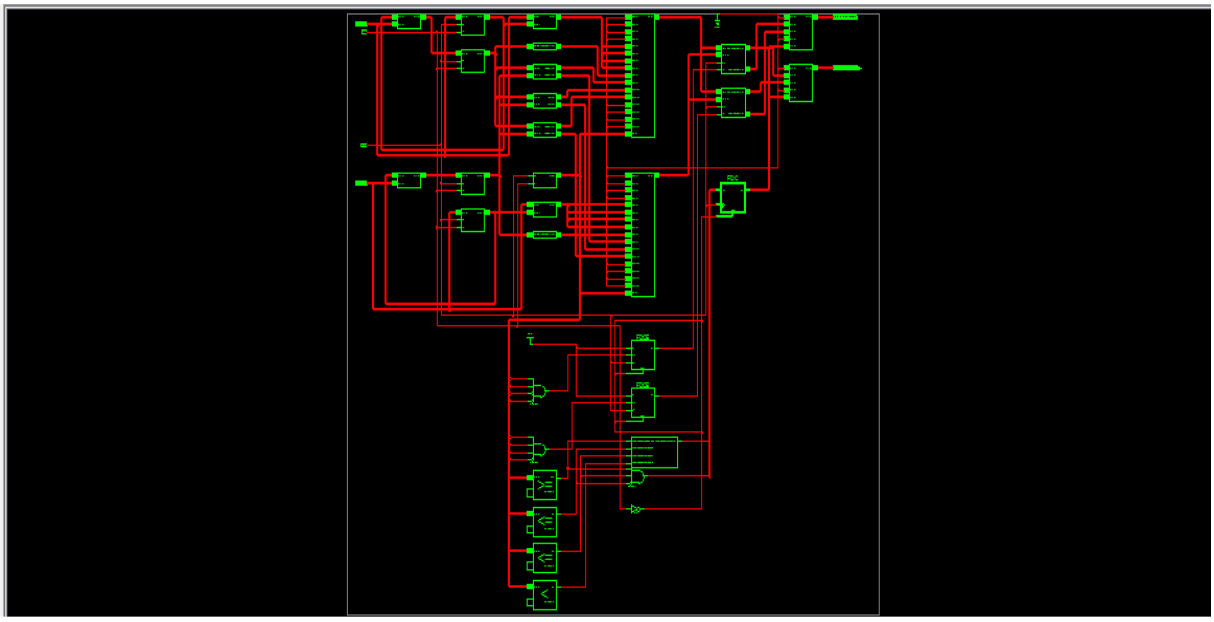

Fig. 9: RTL view of conventional R2SDF FFT

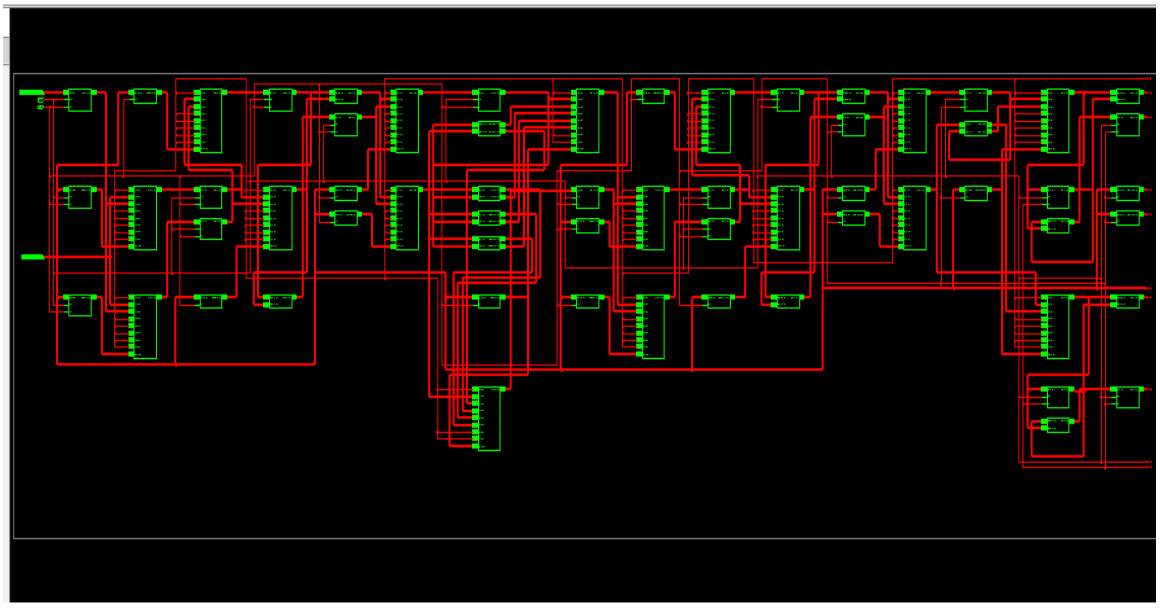

Fig. 10: RTL view of proposed pipelined radix-2 mixed SDC-SDF FFT

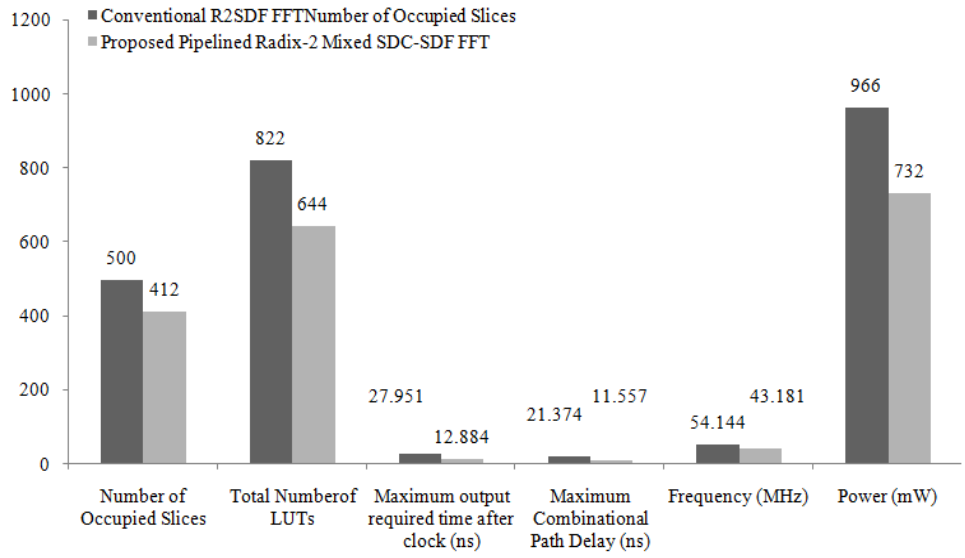

Fig. 11: Performance evaluation of conventional R2SDF FFT and proposed pipelined radix-2 mixed SDC-SDF FFT

Table 1: Comparison of conventional R2SDF FFT and proposed pipelined radix-2 mixed SDC-SDF FFT

Types/VLSI concerns	Number of Occupied Slices	Total Number of LUTs	Maximum Output Required time after clock (ns)	Maximum Combinational Path Delay (ns)	Frequency (MHz)	Power (mW)
Conventional R2SDF FFT	500	822	27.951	21.374	54.144	966
Proposed Pipelined Radix-2 Mixed SDC-SDF FFT	412	644	12.884	11.557	43.181	732
Percentage Reduction	17.6%	21.65%	53.90%	45.92%	20.24%	24.22%

The Performance Evaluation of both conventional 8-point R2SDF FFT and Proposed pipelined Radix-2 SDC-SDF FFT are analyzed and compared in Table 1. Also the performance evaluations are graphically illustrated in Fig. 11.

From Table 1, it is clear that Proposed Pipelined Radix-2 Mixed SDC-SDF FFT offers 17.6% reduction in hardware Slices, 21.65% reduction in number of LUTs, 53.90% reduction in maximum output required time after clock and 45.92% reduction in maximum

combinational path delay and 24.22% reduction in Power consumption than conventional R2SDF FFT.

CONCLUSION

In this study, a new architecture "Pipelined Radix-2 Single path Delay Commutator (SDC) -Single path Delay Feedback (SDF) FFT" has been designed through Very Large Scale Integration (VLSI) System design environment. The primary aim of this research work is to reduce the hardware utilization and power consumption of FFT Processors and the secondary goal is to increase the speed and throughput of the System. Proposed Mixed SDC and SDF architecture utilizes 50% same hardware for performing multiple computations. Traditional Bit Parallel Multiplication (BPM) is used instead of Reconfigurable Complex Multiplier to perform complex multiplication. Hence, Proposed System gives more advantage than conventional R2SDF FFT structures. Proposed Pipelined Radix-2 Mixed SDC-SDF FFT structure offers 17.6% reduction in hardware Slices, 21.65% reduction in number of LUTs, 53.90% reduction in maximum output required time after clock and 45.92% reduction in maximum combinational path delay and 24.22% reduction in Power consumption than conventional R2SDF FFT. In future, the proposed architecture will be absolutely useful in OFDM based digital communication to perform the function of frequency transformation and to analyze the spectrum characteristics of digital inputs.

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