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Research Article

FPGA Based ASFSRBN Controller for Low Offset Integrator for Long Pulse Operation in Aditya Tokamak

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Abstract: Tokamaks are the most proficient devices for acquiring nuclear fusion energy from high-temperature, ionized gas termed as Plasma. Mostly, tokamaks are utilized the toroidal magnetic plasma component and poloidal magnetic plasma component to retain and automatic control. Similar characteristics of two operational amplifiers should be needed in the integration system to calculate the drift value. Inductive magnetic sensors are routinely utilized on existing Tokamaks, are well comprehended and they oblige signal integration to focus the strength of the magnetic field. However, the signal integration failed to solve the problem of deciding the stability of the controlled systems. The Sample and Hold Amplifier (SHA) is an essential part of the sampling (Analog Devices, 2009) to digital convert (ADC). The proposed method is used for eliminating the offset drift of the Integrator for long pulse operations. Adaptive Self Organizing Fuzzy Radial Basis-Function Neural Network Controller (ASFRBNC) and DAC amplifiers are able to adjust the signal for utilization of the PCS and DAS dynamic ranges. The loop processing has done with MATLAB Simulink process. This tokamak has 100s pulse lengths, oblige integrators with better attributes in drift and noise with the long pulse lengths. The proposed system was implemented in Field Programmable Gate Array (FPGA) chip with the use of Verilog Hardware Description-Language (Verilog HDL). The experimental results shown that the proposed method obtained 745 Slices, 61 Flip-Flops (FF), 46 I/O buffers (IOBs), 1221 4bit Look up Tables (LUT) and synchronized with the maximum 50.36MHz clock frequency. The obtained hardware results have been matched with the MATLAB simulation results.

Keywords: ASFSRBN controller, DAC amplifier, integrator circuit, instrumentation amplifier, sample and hold amplifier

INTRODUCTION

A tokamak Alan (2008) is a torus molded device utilizing capable magnetic fields to bind the plasma. The tokamak Bora *et al*. (2002) is worked in a pulsed mode, which is kept up within the tokamak for 80-100 milliseconds. It is utilized to study the responses of plasma, which happen at high temperatures. Different techniques of magnetic profiles, inductive pickup loops are one of the essential magnetic diagnostics in current fusion theories due to their simple development and robustness. Indeed the most advanced fusion devices utilize inductive pick up loops, with numerous descriptions planned for estimations in long-pulse burning plasma devices and analyses.

The lines of magnetic field stirring around the torus shaped restriction helically are needed to get a stable equalization of the plasma. Such a field is produced by including two individual magnetic field components. One component, toroidal magnetic field moves in loops all through the torus and other components, poloidal magnetic field is perpendicular to the toroidal field. The toroidal field is created by the electromagnets around the tokamaks and the poloidal field is produced by the plasma current streaming in the torus. In nuclear fusion, such a technique of magnetic confinement is utilized because no further techniques of solid restrictions can withstand such very high temperatures of the plasma. Plasma is the fourth state of matter. This state of matter is very similar to the gaseous state yet the plasma particles are ionized. However, plasma is not only influenced by electric and magnetic fields but also influenced by the magnetic field of the earth. Different tokamak devices have been designed in different types of integrators to reduce the integrator drift. Without modifying basic principles, Analog integrator for thousand second long pulses (Bishop *et al*., 1995), improved the precision and reliability of the magnetic field measurements up to 1000s long time pulses. A Hybrid Digital Analog Long Pulse Integrator Spuig *et al*. (2003), described for very long pulse durations. However, the error of the integration computes at the square root of the pulse length. Strait *et al*. (1997), the Integrator introduced another technique of integration method by using a Voltage to Frequency Converter and Up Down Counter (VFC-

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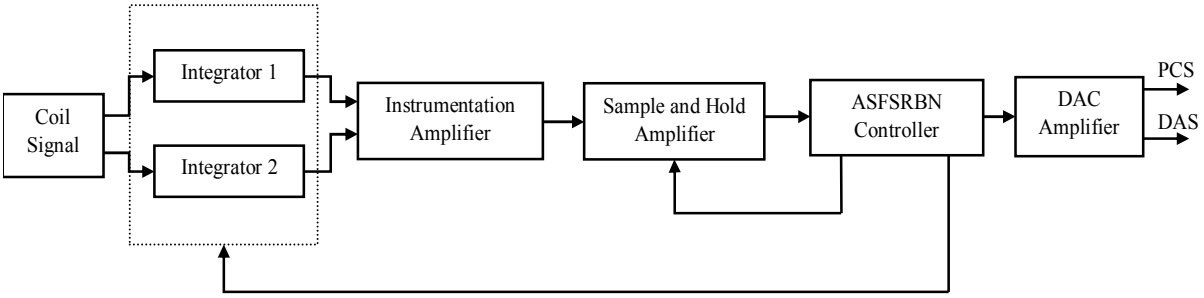

Fig. 1: FPGA based block diagram of the integrator system

UDC). In this technique, it consisted of three VFC-UDC units and Digital Signal Processing (DSP) selects from these three consecutive outputs of the integrator. However, the above techniques of signal integration failed to solve the problem of deciding the stability of the controlled systems.

The proposed technique introduced new technique which is done FPGA based ASFSRBN controller for low offset integrator for long pulse operation in plasma tokamak. The methodical diagram of the proposed system is shown in Fig. 1.

The FPGA based new integration system is essentially created the integral part and the ASFSRBN control module. The integral part integrates the input signals and generates output signals. Then the result of the Integrator circuit follows the sample and hold amplifier. The major electronic issue is to recognize little physical drifts of the plasma from the inalienable drift of obliged signals because of little uncorrected offsets in the procurement circuit. In SHA, the output follows the input with a small offset voltage in sample mode. However the output does not follow the input accurately in sample mode, in hold command only the output gets accurately. Then ASFSRBN controller is able to adjust the signal for the plasma equilibrium and shape control of the Plasma Control System (PCS) and the Data Acquisition System (DAS) dynamic ranges. The ASFSRBN controller solves the problem of deciding the stability of the system control (PCS and DAS). It additionally applies a versatile law to change the fuzzy ensuing parameter of a fuzzy logic controller to control an automated system to enhance its control execution. Hence, the ASFSRBN accomplished better control execution over the other controlling techniques.

PROPOSED METHOD

Integration circuits: To calculate the drift value, similar characteristics of two operational amplifiers needed. Hence, in two operational amplifiers, one amplifier should be grounded and other operational amplifier should be connected to the inductive coil pick up loop via few set of switches. A dual operational amplifier is adopted to realize two integrators. The input of the integrator II is connected to the coil and the input of the integrator I is connected to the ground.

Figure 2, the clearing feedback capacitor step and integration functional steps are the two processed steps. In the clearing feedback capacitor step, before the integrator works the electric charges contained feedback capacitors are removed through sw1, sw3 switches on and sw2, sw4 switches off. In the integrator functional step, the control signal integration time is sent to switch by sw1, sw3 switches off and sw2, sw4 switches on.

The input coil signal $v_i(t)$ is applied to the Integrator-II for integration using the resistor R_1 and the capacitor C and Integrator-I is connected to ground with the resistor R_2. Hence, the offset current and offset voltages of Integrator-I and Integrator-II are denoted as I_{os1}, I_{os2} and v_{os1}, v_{os2} respectively:

$$v_{01}(t) = -\frac{1}{T_1}\int_{t_0}^{t}[v_i(t) + R_1 I_{os1} - v_{os1}]\,dt \qquad (1)$$

$$v_{02}(t) = -\frac{1}{T_2}\int_{t_0}^{t}[v_i(t) + R_2 I_{os2} - v_{os2}]\,dt \qquad (2)$$

where, $T_1 = R_1 C$ and $T_2 = R_2 C$.

The integration drift is dominated by the accumulated drift caused by the offset current (I_{os}) and voltage (v_{os}) of the operational amplifier. The two integrators outputs can be combined to make a persistent integral of the source signal, with the commitment from both integrators corrected with the prior drift estimation on that integrate. It can be done to suit the necessities of continuous plasma position control, which is limited by the frequency response of the Integrator and the negligible drift correction processing time.

Instrumentation amplifier: The instrumentation amplifier is utilized to subtract the Integrator I output signal from the Integrator II output signal, Hence, the drift is compensated by the output of the instrumentation amplifier is called as integration signal. From to Eq. (1 and 2), the instrumentation amplifier is defined as:

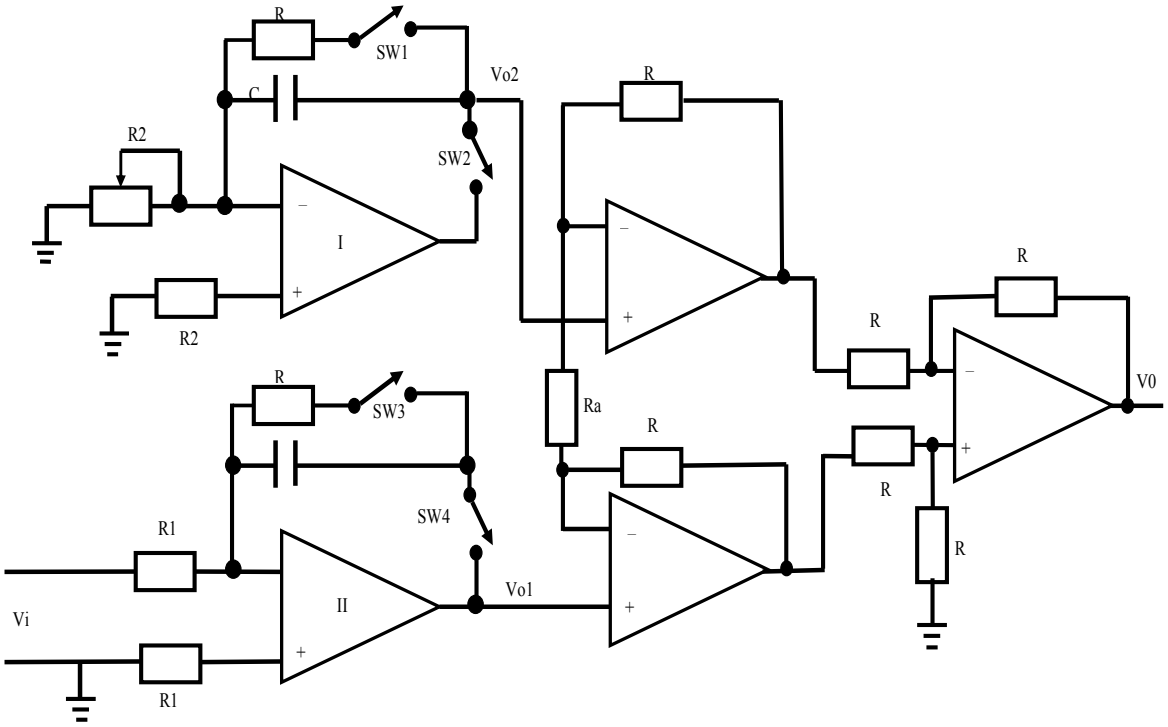

Fig. 2: A detailed circuit of parts of the circuits in the integration circuit

$$v_0(t) = v_{01}(t) - v_{02}(t) \quad (3)$$

$$= -\frac{1}{R_1C}\int_{t_0}^{t}[v_i(t) + R_1I_{os1} - v_{os1}]\,dt + \frac{1}{R_2C}\int_{t_0}^{t}[R_2I_{os2} - v_{os2}]\,dt$$

$$= -\frac{1}{R_1C}\int_{t_0}^{t} v_i(t)dt + \left[-\frac{1}{R_1C}\int_{t_0}^{t}(R_1I_{os1} - v_{os1})\,dt + \frac{1}{R_2C}\int_{t_0}^{t}[R_2I_{os2} - v_{os2}]\,dt\right]$$

$$= -\frac{1}{R_1C}\int_{t_0}^{t} v_i(t)dt + (t - t_0)\left[\frac{(R_2I_{os2} - v_{os2})}{R_2C} - \frac{(R_1I_{os1} - v_{os1})}{R_1C}\right] \quad (4)$$

The Eq. (4) should be equal to zero, to eliminate the drift for a long time:

$$\frac{(R_2I_{os2} - v_{os2})}{R_2C} = \frac{(R_1I_{os1} - v_{os1})}{R_1C}$$

Sample and Hold Amplifier (SHA): The Sample and Hold Amplifier (SHA) is an essential part of the sampling Analog to digital convert (ADC). And ADCs are major applications to the SHAs. The AC and DC performance is completely specified in a sampling ADC. The Sample and Hold Amplifier (SHA) is a discriminating part of Data Acquisition Systems (DCS). It catches an analog signal and holds it during some operation. SHA performed by input amplifier, switch driver, capacitor and output buffer, shown in the Fig. 3. The capacitor is the most important component in SHA. Initially, the input amplifier buffers the input signal with high impedance and current gain presents to charge the hold capacitor. In the sample mode, the switched is closed and then the input signal with delay is followed by the voltage on the hold capacitor. The switch is open in the hold mode and the hold capacitor keeps the voltage before disconnected from the input buffer. Hence, the output buffer presents high impedance to the hold capacitor to retain the held voltage from discharging early.

Adaptive Self Organizing Fuzzy Radial Basis-Function Neural Network Controller (ASFSRBN) controller: Adaptive Self Organizing Fuzzy Radial Basis-Function Neural Network Controller (ASFRBNC) and DAC amplifiers are able to adjust the signal for utilization of the PCS and DAS dynamic ranges. Figure 4, the output of SHA is applied to a sliding surface with the difference, sliding surface is utilized to gain controlling and the fuzzy logic controller is used to improve the performance of the integrator. Adaptive law is utilized to consistence of the integrator performance and RBFN and self organizing techniques are used to eliminate the wrong selections problems of the selection parameter of the integrator and SHA. The DAC amplifier is generated the digital to

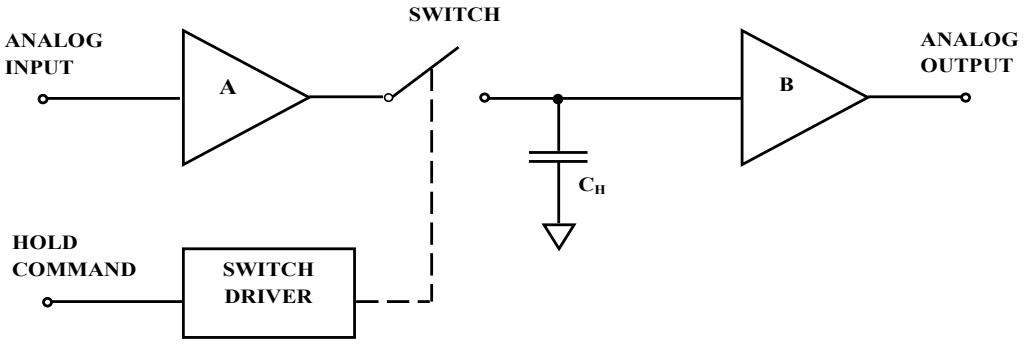

Fig. 3: SHA circuit diagram

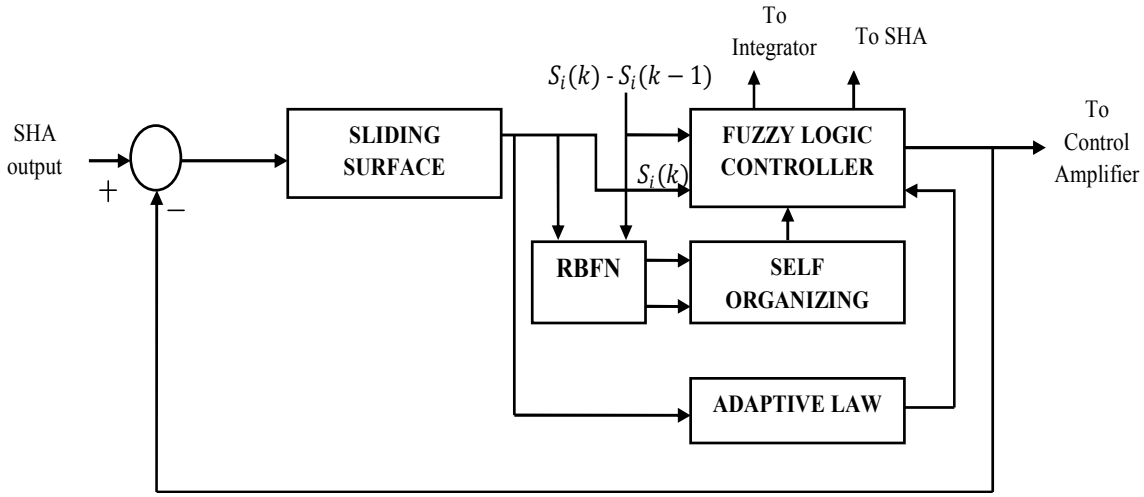

Fig. 4: FPGA based adaptive self optimized fuzzy sliding mode radial basis function neural network (ASFSRBN) controller

analog output. Therefore, the proposed integration system is able to eliminate the offset drift of the integrated amplifier system.

RESULTS AND DISCUSSION

Every integrator components are completely established in the dual integrated circuits. Each integrator input is connected to the magnetic coil. In general, the magnitude of the integrator output signal is controlled by the time length a voltage is present at its input through the feedback loop either charges the capacitor or discharges the capacitor as the requisite negative feedback goes through the capacitor. The input voltage is 1mVs and time constant RC is 20 ms then the output signal is 0.5 mVs, shown in Fig. 5.

This process can regulate the time constant of the integrator. The integration time set as 100 sec and unity gain of the control amplifier. Due to the error of the baseline signal and input signal, the overall drift of the integrated system is less than 0.5%. The approximated noise level is 5 mV.No conspicuous drifts have been examined within the element scope of the digitizer. During the performance of the integrators, the drift is less than 5 mV for 100s.The time varying drift issue and its mitigation by base-line signal, is represented in Fig. 6. The current of the both integrators goes through the signal source during the overlap. However this overlap is constrained on operation times. The source signal and resistor ought to match DC resistances else linear drift will be produced in the integral. So, by using the resistance inside the integrators, this error can be reduced.

For implementation of ASFSRBN controller in analog domain, FPGA is interfaced with the both Analog to Digital Converter (ADC) which is used as SHA and Digital to Analog Converter (DAC) which is used in DAC amplifier. FPGAs are flexible and reprogrammable which is utilized for hardware implementation for fast implementation and verification. The programming was generated by using Verilog Hardware Description Language (Verilog HDL). The Verilog HDL code for ASFSRBN controlling was implemented in Xilinx ISE Design Suite 13.1. The zynq-7000 FPGA is used XC7Z010 device for the design realizations. The zynq-7000

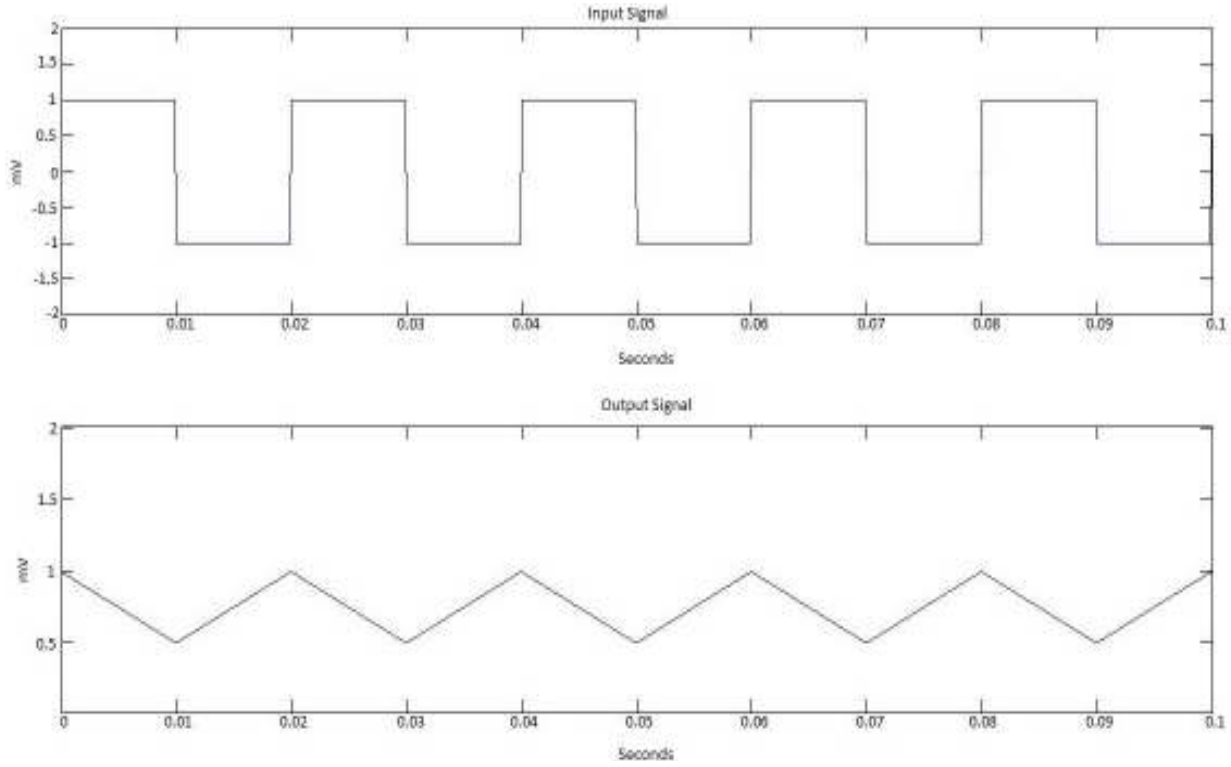

Fig. 5: Integrator test from the input signal

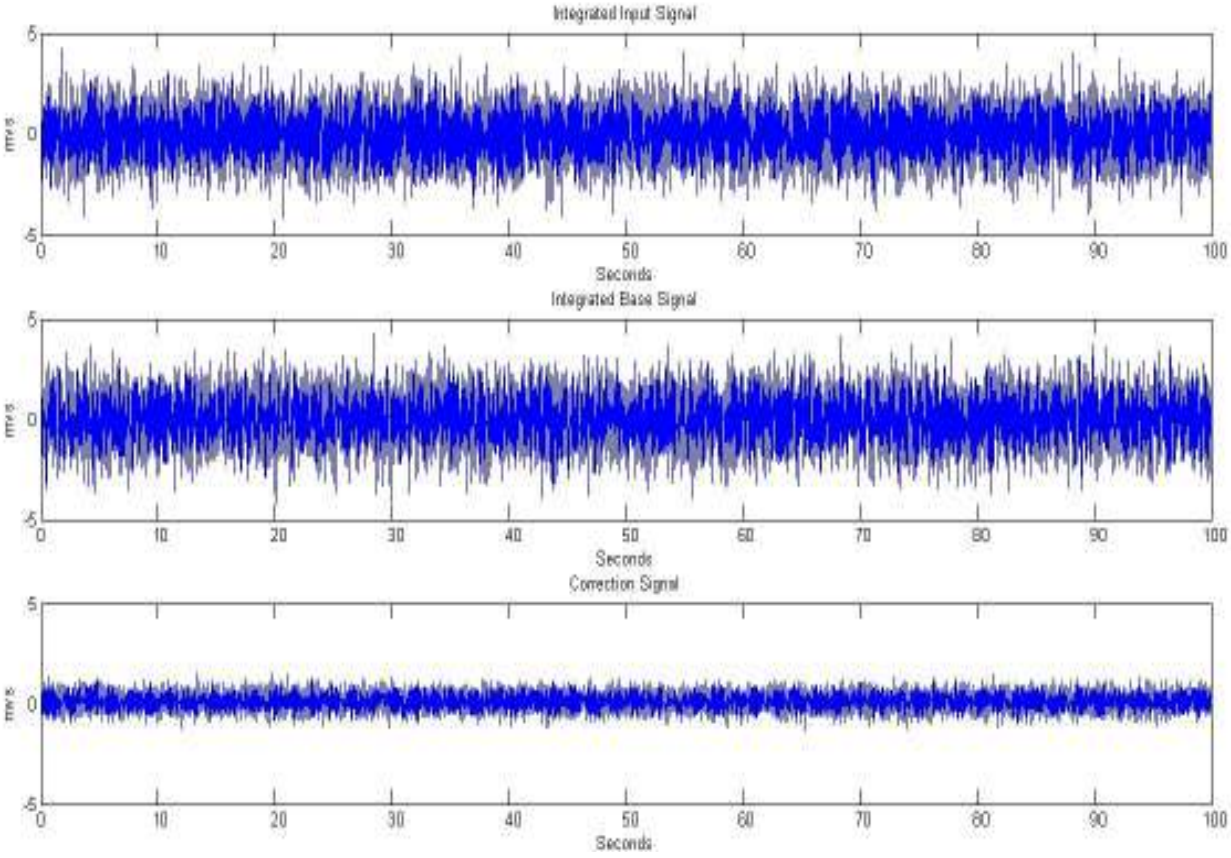

Fig. 6: Integration drift for 100 seconds

FPGA is a dual ARM core processor with the frequency of 866 MHz.

According to the all timing constraint results, the ADC conversion time is 2 sec and DAC settling time is 16 sec per each channel. The entire concept is obtained 745 slices, 61 Flip-Flops (FF), 46 I/O buffers (IOBs), 1221 4bit Look Up Tables (LUT) and synchronized with the maximum 50.36 MHz clock frequency. The obtained hardware results have been matched with the MATLAB simulation results.

CONCLUSION

This study proposes the FPGA based Adaptive Self Organizing Fuzzy Radial Basis-Function Neural Network Controller (ASFRBNC) for low offset integrator for long pulse operation in Aditya tokamak. The ASFSRBN controller solves the problem of deciding the stability of the system control (PCS and DAS). It additionally applies a versatile law to change the fuzzy ensuing parameter of a fuzzy logic controller to control an automated system to enhance its control execution. Hence, the ASFSRBN accomplished better control execution over the other controlling techniques. This study approaches for the implementation of the proposed method in Zynq-7000 XC7Z010 FPGA device. The MATLAB results indicate that the proposed method is able to reduce the offset drift values at 100s integration time set. Due to the error of the baseline signal and input signal, the overall drift of the integrated system is less than 0.5%. The approximated noise level is 5 mV. The hardware results shown that the whole system is obtained 745 Slices, 61 Flip-Flops (FF), 46 I/O buffers (IOBs), 1221 4bit Look up Tables (LUT) and synchronized with the maximum 50.36 MHz clock frequency. The obtained hardware results have been matched with the MATLAB simulation results.

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