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Research Article

Unequal Divider with Asymmetric Shunt Open Stub for Reduced Size and Harmonic Suppression

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Abstract: This study presents an unequal divider with asymmetric shunt open stubs to reduce circuit size and achieve harmonic suppression. The design method was derived from S- to admittance parameter conversion of unequal divider. We validated the use of the parameter conversion method to reduce the size and achieve harmonic suppression of the unequal divider by implementing the divider at a power ratio of 3 at a center frequency of 1 GHz. The measured characteristics agreed well with the results of the calculation and the harmonic suppression was improved by more than 14 dB between the 2nd and 4th harmonics with 20% reduction in size compared to a conventional divider.

Keywords: Asymmetric shunt open stub, harmonic suppression, reduced size, S-parameter conversion, unequal divider

INTRODUCTION

A power divider is a basic component for RF/microwave system and performs functions such as power divide and combine network for amplifier (Jang *et al*., 2014; Feng *et al*., 2013) and mixer (Razavi, 1997) modules and feed networks for antenna (Nikfalazaar *et al*., 2016; Stutzman and Thiele, 2000). Wireless systems require a harmonic rejection filter (Madadi *et al*., 2016; Guo *et al*., 2015) for the microwave circuit, because the harmonic signals cause normal operation to malfunction. However, this filter increases the cost and the size of the equipment.

To eliminate influence of the harmonic signal, the wireless systems require to insert a harmonic rejection function at the point which signal split and combine occurs. Recently, many paper for divider and combiner have been reported for harmonic suppression, such as two quarter-wave open stub located at the center of the quarter-wave branches (Yi and Kang, 2003), an asymmetric spiral defected ground structure in quarter-wave line (Woo and Lee, 2005), an electromagnetic band-gap structure (Lin *et al*., 2007; Zhang and Li, 2008), a high-low impedance resonator cell (Wang *et al*., 2009), a series inductor (Mirzavand *et al*., 2013) and a general π-type structure for an equal divider (Wang *et al*., 2015). Most of these papers are concerned with equal dividers for harmonic suppression and unequal dividers have not received much attenuation.

This study describes an unequal divider with harmonic suppression and size reduction based on S- to admittance parameter conversion. Figure 1 shows the equivalent circuit of conventional and the proposed unequal divider. The quarter-wave line of conventional unequal divider in Fig. 1a can be change to a line with asymmetric shunt open stubs in Fig. 1b, which consists of one transmission line and two shunt open stubs and their characteristic impedance and electrical length are different all. In contrast to the even-/odd-mode analysis method, the S- to admittance parameter conversion (Miao *et al*., 2014, 2012; Kim, 2016) constitutes a simple design method for unequal divider to include phase delay information and arbitrary port impedances and asymmetrical configurations. Thus, parameter conversion methods are introduced for unequal dividers, the design equations are derived and synthesis procedures are provided. The reported general π-type structure divider in reference (Wang *et al*., 2015) is a special case of one proposed in this letter. The performance of an unequal divider with power ratio of $k^2 = 3$ at operating frequency of 1 GHz is evaluated by measuring its insertion loss, reflection and harmonic suppression characteristics and its ability to reduce circuit size.

MATERIALS AND METHODS

When and where this study was conduct: This research was conducted at Kumoh National Institute of Technology test facility in 2016.

The equivalent circuit of an unequal divider with power ratio k^2 (= P_3/P_2) is depicted in Fig. 1. The S-

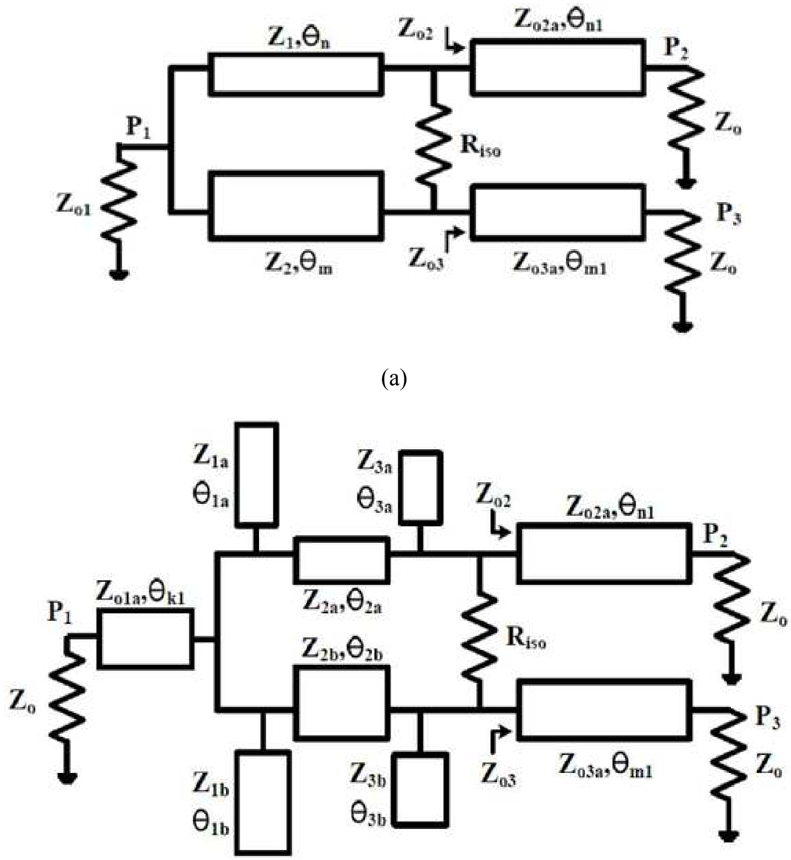


Fig. 1: Equivalent circuit of (a) conventional and (b) proposed unequal divider

parameters of this divider with phase delay θ can be expressed as:

$$(S)=\frac{1}{\sqrt{1+k^2}}\begin{pmatrix} 0 & e^{-j\theta} & ke^{-j\theta} \\ e^{-j\theta} & 0 & 0 \\ ke^{-j\theta} & 0 & 0 \end{pmatrix} \tag{1}$$

The S- to admittance parameter conversion can be performed using following equations:

$$(Y)=(Y_{oi})(U-S)(U+S)^{-1}(Y_{oi}) \tag{2}$$

$$(Y_{oi})=\begin{pmatrix} \sqrt{Y_{01}} & 0 & 0 \\ 0 & \sqrt{Y_{02}} & 0 \\ 0 & 0 & \sqrt{Y_{03}} \end{pmatrix} \tag{3}$$

where $Y_{01} = 1/Z_{01}$, $Y_{02} = 1/Z_{02}$ and $Y_{03} = 1/Z_{03}$ are the port admittance and U is the unit matrix.

Using Eq. (2), the admittance matrix of an unequal divider with power ratio k^2 and electrical length $\theta = 90°$ is given as:

$$(Y)_{conventional}=\begin{pmatrix} 0 & \frac{j}{\sqrt{(1+k^2)Z_{01}Z_{02}}} & \frac{jk}{\sqrt{(1+k^2)Z_{01}Z_{03}}} \\ \frac{j}{\sqrt{(1+k^2)Z_{01}Z_{02}}} & \frac{k^2}{(1+k^2)Z_{02}} & \frac{-k}{(1+k^2)\sqrt{Z_{02}Z_{03}}} \\ \frac{jk}{\sqrt{(1+k^2)Z_{01}Z_{03}}} & \frac{-k}{(1+k^2)\sqrt{Z_{02}Z_{03}}} & \frac{1}{(1+k^2)Z_{03}} \end{pmatrix} \tag{4}$$

On the other hand, according to the definition of an admittance parameter, the admittance parameters of the proposed unequal divider in Fig. 1b can be written as:

$$(Y)_{proposed}=\begin{pmatrix} Y_{11} & Y_{12} & Y_{13} \\ Y_{12} & Y_{22} & Y_{23} \\ Y_{13} & Y_{23} & Y_{33} \end{pmatrix} \tag{5}$$

$$Y_{11}=jY_{1a}\tan\theta_{1a}-jY_{2a}\cot\theta_{2a}+jY_{1b}\tan\theta_{1b}-jY_{2b}\cot\theta_{2b} \tag{6}$$

$$Y_{12}=\frac{j}{Z_{2a}\sin\theta_{2a}}\quad,\quad Y_{13}=\frac{j}{Z_{2b}\sin\theta_{2b}} \tag{7}$$

$$Y_{22}=-jY_{2a}\cot\theta_{2a}+jY_{3a}\tan\theta_{3a}+\frac{1}{R} \tag{8}$$

$$Y_{23} = -\frac{1}{R} \tag{9}$$

$$Y_{33} = -jY_{2b}\cot\theta_{2b} + jY_{3b}\tan\theta_{3b} + \frac{1}{R} \tag{10}$$

We obtain the simple design equations of the proposed unequal divider by assuming the following conditions:

$$\theta_{1a} = \theta_{1b} = \theta_1 \quad , \quad \theta_{2a} = \theta_{2b} = \theta_2 \quad , \quad \theta_{3a} = \theta_{3b} = \theta_3 \tag{11}$$

$$Z_{01} = Z_o \quad , \quad Z_{02} = \frac{Z_o}{k} \quad , \quad Z_{03} = \frac{Z_o}{k^3} \tag{12}$$

Imposing admittance parameter equality of (4) and (5) and using (6) ~ (10), the design parameters specified in Fig. 1b can be obtained as follows:

$$Z_{2a} = \frac{\sqrt{(1+k^2)Z_{01}Z_{02}}}{\sin\theta_2} \quad , \quad Z_{2b} = \frac{\sqrt{(1+k^2)Z_{01}Z_{03}}}{k\sin\theta_2} \tag{13}$$

$$Z_{3a} = Z_{2a}\tan\theta_2\tan\theta_3 \quad , \quad Z_{3b} = Z_{2b}\tan\theta_2\tan\theta_3 \tag{14}$$

$$\left(\frac{1}{Z_{1a}} + \frac{1}{Z_{1b}}\right)\tan\theta_1 = \left(\frac{1}{Z_{2a}} + \frac{1}{Z_{2b}}\right)\cot\theta_2 \tag{15}$$

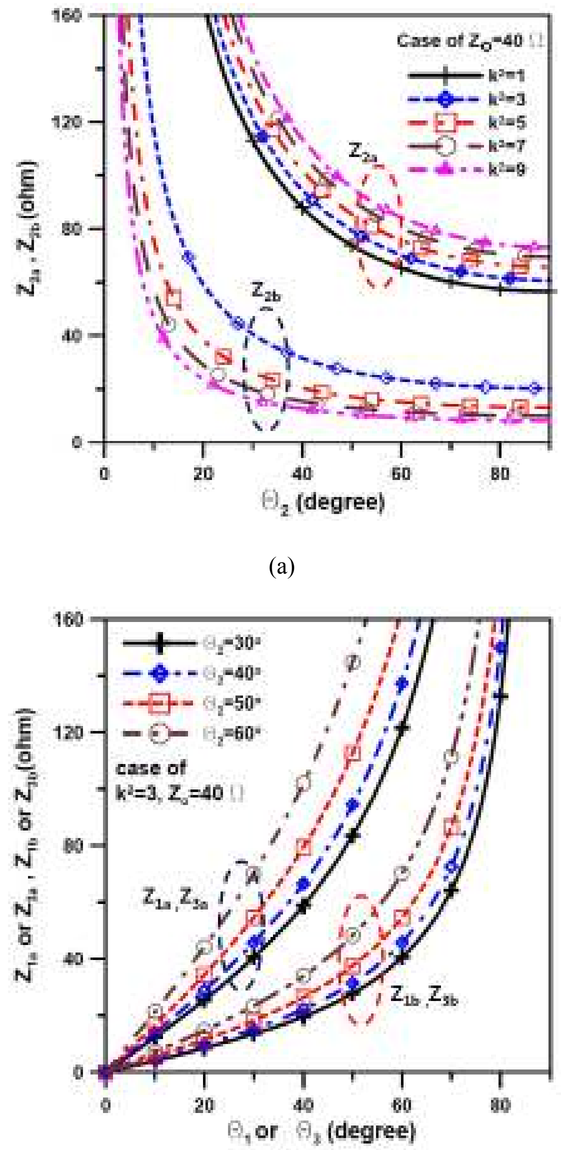
$$R = \left(k + \frac{1}{k}\right)\sqrt{Z_{02}Z_{03}} \tag{16}$$

RESULTS AND DISCUSSION

We designed the proposed unequal divider by calculating the impedance values using Eq (13) ~ (16). Characteristic impedance values from 10 Ω to 150 Ω were chosen to obtain the possible width of implementation transmission line in microstrip technology.

The impedance values of divider are obtained when the electrical length of θ_2 and power ratio of k^2 using Eq. (13) are varied. The impedance values of Z_{2a} and Z_{2b} are presented in Fig. 2a in case of Z_o = 40 Ω. When the power ratio of k^2 and electrical length of θ_2 are determined, the graph showed the relation between the electrical length θ_3 and impedance values of Z_{3a} and Z_{3b} in Fig. 2b. In addition, when the power ratio of k^2 and the electrical length of θ_2 and θ_3 are determined, the relation between electrical length θ_1 and impedance values of Z_{1a} and Z_{1b} can be obtained, as shown in Fig. 2b. This relationship graph between impedance values of Z_{1a} and Z_{3a} and electrical length θ_1 and θ_3 represents the same data if the impedance ratio satisfied the condition of $Z_{1a} = Z_{1b}/k^2$.

We validated the proposed unequal divider with asymmetric shunt open stubs by designing and simulating an unequal divider with a power ratio of k^2 = 3 at an operating frequency of 1 GHz. Fabrication of the high impedance lines of the unequal divider was facilitated by selecting the characteristic impedance of Z_o = 40 Ω. Using Eq. in (13) ~ (16), we obtain the following design parameters: impedance values of Z_{1a} = 55.6 Ω, Z_{2a} = 94.6 Ω, Z_{3a} = 37.0 Ω, Z_{1b} = 18.5 Ω, Z_{2b} = 31.5 Ω, Z_{3b} = 12.3 Ω and electrical lengths of θ_1 = 35°, θ_2 = 40°, θ_3 = 25°. Furthermore, to match the impedance of port of 50 Ω, we used the quarter-wave transformer impedance of Z_{o1a} = 44.7 Ω at port 1, Z_{o2a} = 34.0 Ω at port 2 and Z_{3a} = 19.6 Ω at port 3. The isolation resistor we used is a chip resistor of 30 Ω.



(a)

(b)

Fig. 2: Design parameter data of the unequal divider (a) Z_{2a} and Z_{2b} versus θ_2, (b) Z_{1a} or Z_{3a} and Z_{1b} or Z_{3b} versus θ_1 or θ_3

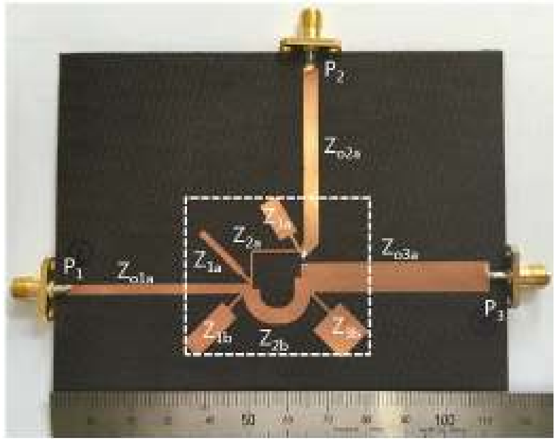
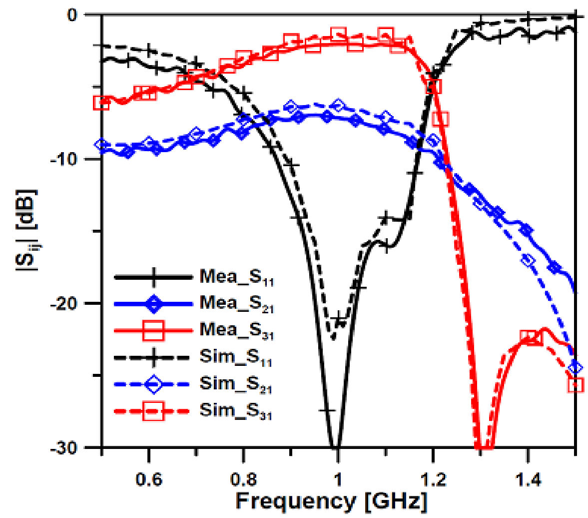
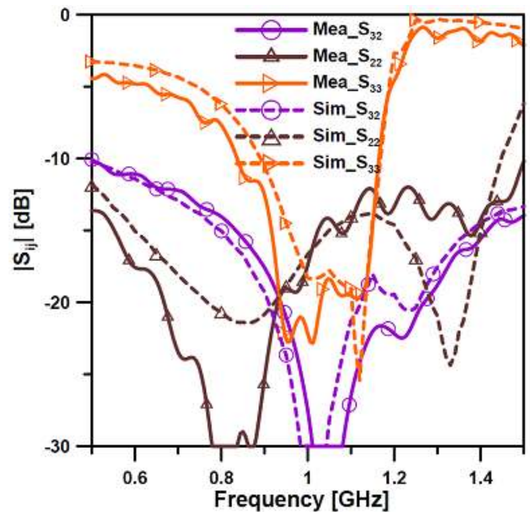


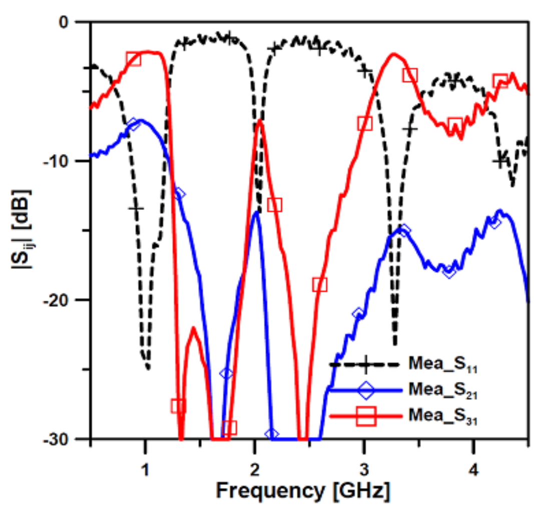
Fig. 3: Photograph of the fabricated unequal divider with asymmetric shunt open stubs



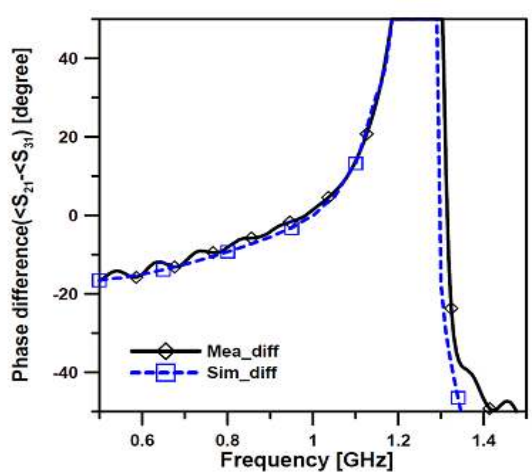
(a)



(b)



(c)



(d)

Fig. 4: Simulated and measured results; (a): $|S_{11}|$, $|S_{21}|$, $|S_{31}|$; (b): $|S_{22}|$, $|S_{33}|$, $|S_{23}|$; (c): harmonic characteristics; (d): phase difference of S_{21} and S_{31}

Table 1: Summary of published power divider

Reference	Operating band	Design approach	Harmonic suppression	Size reduction
Yi and Kang (2003) (equal divider)	2.05 GHz	Open stub	3rd 40 dB	-
Lin *et al*. (2007) (equal divider)	2.4 GHz	EBG	3rd 32.5 dB 5th 12 dB	30%
Zhang and Li (2008) (equal divider)	0.9 GHz	Parallel coupled on DGS	3rd 35 dB	34%
Wang *et al*. (2009) (equal divider)	2.65 GHz	Resonator	3rd 29 dB 5th 34 dB	36.5%
Mirzavand *et al*. (2013) (equal divider)	1 GHz	Inductor	2nd 28 dB 3rd 32 dB 4th 20 dB	60%
Wang *et al*. (2015) (equal divider)	1 GHz	Open stub	-	-
This work (unequal divider)	1 GHz	Open stub	2nd ~ 4th 14 dB	20%

Figure 3 shows a photograph of the fabricated 3:1 unequal divider with asymmetric shunt open stubs. The main circuit size is 45 mm × 40 mm (0.237 λ_g by 0.21 λ_g), only about 80% of conventional divider (0.31 λ_g by 0.2 λ_g). The PCB was fabricated Teflon PCB of Taconic, with dielectric constant ε_r = 2.5, a height of h = 0.787 mm and conductor thickness of t = 0.035 mm. This unequal divider was designed and optimized with the Microwave Office software, developed by National Instruments.

The measured data for this proposed unequal divider are shown in Fig. 4; the simulated and measured results can be seen to be almost coincident.

In Fig. 4, the insertion losses are $|S_{21}|$ = 7.16 dB and $|S_{31}|$ = 2.06 dB. These values are slightly different from those obtained from the simulation, because of the PCB substrate and fabricated losses. The isolations are $|S_{23}|$ = 27.5 dB and return losses are more than $|S_{ii}|$ = 17 dB, where i = 1, 2 and 3. The harmonic signals are rejected more than 14 dB at port 2 and 7 dB at port 3, respectively, between the 2nd and 4th harmonics, as seen in Fig. 4c. There is a frequency range between 0. 98 ~ 1.04 GHz for phase difference of ±5° between output ports.

A comparison of power dividers for reduction size and harmonic suppression is summarized in Table 1. As the results show, this study presents a size reduction unequal divider with harmonic suppression.

CONCLUSION

This study describes the development of an unequal divider with asymmetric shunt open stubs using the simple design method of S- to admittance parameter conversion. The experimental results show that the performance characteristics of the fabricated unequal divider correspond to the simulation results and that harmonic suppression of more than 14 dB at port 2 and 7 dB at port 3 between the 2nd and 4th harmonics is achieved. In addition, the size of the newly developed unequal divider is reduced by 20% compared to that of a conventional divider.

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