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Research Article

Study on Fault Detection and PCB Picture-Location Method of Logic Circuit

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Abstract: The main content of logic circuit fault detection includes describing circuit to be diagnosed, determining fault and circuit initial information, generating circuit location test set. In this study, LASAR is used to carry out the logic circuit simulation so as to create such documents as fault dictionary, node truth value table, etc. for the preparation of fault detection. Due to the limitation of circuit observability and testing vectors, the diagnosis program can not accurately locate the fault just once in the process of diagnosis because the circuit is complex and users are not quite familiarity with the circuit. Therefore, the new circuit-fault-detection technology incorporates techniques of PCB picture-location so that the users can locate the fault quickly and accurately.

Keywords: Fault detection, logic circuit, PCB picture-location

INTRODUCTION

The main content of digital circuit fault detection includes describing circuit to be diagnosed, determining fault and circuit initial information, generating circuit location test set, simulating fault, judging whether location test set meets predetermined fault diagnosis requirement, setting up fault diagnosis test program. In the process of fault detection, the fault diagnosis and location can be completed as long as test sequence to the circuit is applied in order, circuit response is measured successively and fault dictionary is retrieved. Gu and Liu (2005) study the fault diagnosis based on automatic testing system. Gao (2000) study the electronic circuit fault diagnosis technology. Zhang and Qiao (2002) analyse the virtual instrument software development environment lab windows/cvi. Yang (2000) has a research of the digital system fault diagnosis and reliability design.

This study designs the logic circuit fault detection system in missile launch control system by LASAR circuit simulation and VXI bus technique. LASAR is used to create such documents as fault dictionary, node truth value table, etc. for the preparation of fault detection. The detection program drives VXI bus to apply exciting signal to the circuit under diagnosis and to read its response and analyzes the fault location according to circuit response and simulation created file. When the circuit could not locate the fault once due to the influence of observability and limitation of test vector, probe is required to test and locate accurately the fault point. The last user can locate the probe quickly and accurately with the new circuit-fault-diagnosis technology which incorporates PCB picture-position technique.

FAULT DICTIONARY TECHNIQUE

Testing functional module and fault positioning module are two modules necessary for a circuit fault diagnosis system. The testing functional module is used for detecting the condition of the target circuit and the fault positioning module is used for analyzing the fault based on the tested result. The actual fault diagnosis just can be carried out under the combination of the testing function and the fault positioning. Said two parts are carried out respectively in the system according to the fault dictionary technique, VXI bus testing technology and related software which are briefly introduced as follows:

Fault dictionary technique: The fault dictionary method is to compare a known correct value with the measured value. If both values coincide, it means the measured module is working normally. Otherwise it must be at fault. This method is characterized in the concept of "ideal module", which must be faultless (ideal) or have a far lower failure rate than the tested module if it has the same function as the tested module. It is only under this precondition that its output can be deemed as corrected expected. The ideal module may also be an "input-output mapping table" storage module. Upon each input, it will output a correct piece of output information. This storage module has a simpler structure and higher reliability than the tested module. The feature of the fault dictionary method is that it can be used to directly tell if the tested module is at fault according to the output of the check.

VXI bus testing technique fault: VXI bus has been known as the 21st century outstanding platform of instrument bus system and automatic testing system.

VXI bus is the tension of VME bus in the field of instrument (VMEbus eXtensions for Instrumentation) and is the modularization automatic instrument system under the control of computer. After several decades of developments, serialization, generalization and the interchangeability and interoperability of the VXI bus instrument are achieved by means of modularization based on effective standardization. And the testing speed of VXI bus is beyond that of other buses. VXI bus technique is excellent in irreplaceable performance in the field of industrial and military measurement and control and that's why this method is used in the fault diagnosis system.

How to utilize the VXI bus testing technique in the circuit fault diagnosis system? The testing functional is majorly worked in two aspects, wherein one aspect is that sending exciting signal to the target circuit board and receiving the response of the output end and another aspect is that extracting the signal in the circuit, wherein said signal in the circuit is the signal of the targeted pin. The fault positioning must be carried out under the precise pin of the element, so the utilization of the signals of the input port and the output port of the target circuit board are not go far enough, the intermediate signal of the circuit must be extracted to supplement, thus, the computer has enough information to determine the special position of the fault. The method of extracting signal in circuit is commonly carried out by needle bed, fixture with chip, testing probe, etc. The testing probe has simple structure, low cost and is convenient to use, so the testing probe is used as the way to extract signal from the circuit in this system.

SR192 module is an impact/response VIX digital testing module capable of implementing said two works in a series of VXI bus equipment. SR192 can implement bus simulation and traditional impact/response in a single chip and housing. To meet the requirement, SR192 is provided with 1 to 12 input/output cards (sum to 192 sockets) and can select the flexibility of I/O card for various circuits (TTL, CMOS, differential calculus, variable, etc.).

LASAR simulation technique: LASAR (Logic Automatic Stimulate and Response) is the software of digital testing procedure producing and diagnosis and simulation system, has the special function of producing fault dictionary after fault simulation. The fault dictionary is a diagnosis database for implementing fault separation to the target circuit board. When testing, a comparison is made to the actual state and ideal output state of PO under each testing so as to probe the fault; if there are the same waveform in the whole testing process, the target digital circuit can be determined it is perfect and no need to undergo fault separation. If there is on different waveform, the circuit would be determined it is in fault and need to separate.

Fault dictionary is a collection of the properties of all detectable faults in the circuit. E.g. some set of faults may have the same properties in the circuit and these faults are formed to be FAULTSET (fault set).

The faults in the fault set cannot distinguished from each other without referring to all previous results, thus, other diagnosis techniques must be used for distinguishing, such as probe. LASAR is able to precisely forecast various responses of the target board in testing, so the testing procedure also can performance overall diagnosis on LASAR software and therefore, the time for debugging the testing equipment can be removed. And LASAR can completely achieve the requirement of TPS (Digital Test Procedure).

Lab window/CVI software: Lab Windows/CVI is used as the development tool of circuit fault diagnosis software and takes Windows operating system as the basic operating environment. Just like other common software development tools, Lab Windows/CVI is also the quick-development condition under graphical interface, which can transfer the focus of work of the designer to the design on actual function of the software, thus, excessive time for writing the interface can be saved. Lab Windows/CVI adopts C as the programming language which brings great flexibility in programming. Moreover, Lab Windows/CVI organically combines powerful C language platform with special measurement and control tools which perform data gathering, analysis and presentation, as well as providing massive development library to improve the function of C language, as a result, Lab Windows/CVI not only can be used for developing common Window application program, but also can be used for developing engineering measurement and control software related to industry or military. As the modularization programming language under instrument control, Lab Windows/CVI is also one of the major software development conditions for VXI bus testing system currently, Lab Windows/CVI can process daily tasks like instrument control, measuring process and testing report, as well as simplifying the tasks produced in testing and developing, such as system integrating, debugging, structural programming design, document processing, etc. In a word, Lab Windows/CVI can make the software development efficient.

THE METHOD OF FAULT DICTIONARY IN SPF LOGIC CIRCUIT

The fault dictionary method is to compare a known correct value with the measured value. If both values coincide, it means the measured module is working normally. Otherwise it must be at fault. This method is characterized in the concept of "ideal module", which must be faultless (ideal) or have a far lower failure rate than the tested module if it has the same function as the tested module. It is only under this precondition that its output can be deemed as corrected expected. The ideal module may also be an "input-output mapping table" storage module. Upon each input, it will output a correct piece of output information. This storage module has a simpler structure and higher reliability than the tested module. The feature of the fault dictionary method is

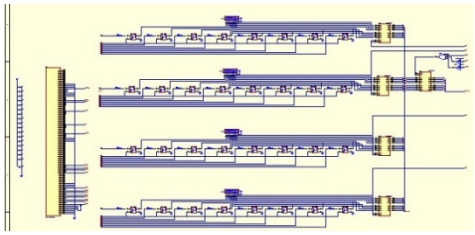

Fig. 1: Lower half of SPF logic circuit

that it can be used to directly tell if the tested module is at fault according to the output of the check.

The fault dictionary method is used in the tested logic-digital circuit SPF (Fig. 1) of missile control and launch system .During the test, excitations are applied to the input ports of the circuit through a VXI and the responses at the output ports are measured through the VXI bus.

For more efficient selection of high-quality testing excitations, typical digital simulation software

LASAR is used to achieve a satisfactory fault coverage rate and to provide data about the evaluation of testing excitations. Its specific function is to generate fault dictionary based on fault simulation. The fault dictionary is used as a diagnosis database of fault isolation for a tested circuit. It stores a list of all the tested faults. Tens of output files can be generated when LASAR is used to simulate circuit. Three core files relating to circuit fault diagnosis, i.e. fault dictionary, node truth table and pin connection table, are design bases for circuit fault location.

During the test, we have to completely understand the principles and design of the circuit compile the testing excitations corresponding to its logic functions and input them together with the connection diagram of the circuit into the simulation software. The simulation software will calculate the correct responses of the circuit to these testing excitations, provide excitation quality indicators such as the fault coverage rate and isolation rate of testing excitations and provide information about how to improve such indicators (e.g., by listing faults not yet detected) in order to consummate the testing excitations. Once the indicators of the testing program meet relevant requirements, it can be loaded into the automatic testing system to perform functional test of the circuit board and the subsequent fault diagnosis. The development of the testing program with LASAR simulation software can be divided into four major steps:

- Modeling of tested unit
- Simulation of a normal board
- Fault simulation
- Post-treatment

The fault dictionary records which step of a certain output has fault when pumping signal is applied (i.e., the output is different from truth value), the chip pins which may cause the problem and the explanation of

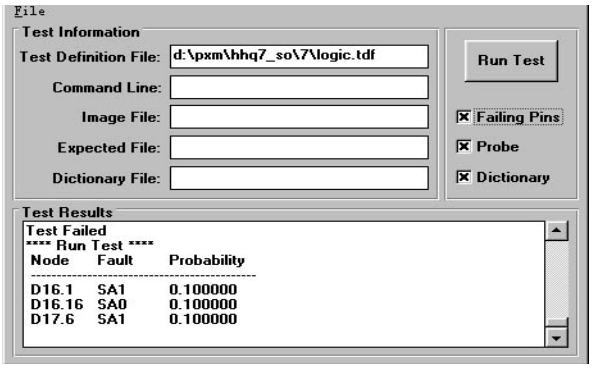

Fig. 2: Detection platform

fault causes. The following are extracts from fault dictionary files:

P 2 A11 D1.3 SA1 3 0-
P 2 A11 D1.14 SA0 3 0-
P 2 A11 D2.6 SA1 3 0-
……

Every line of above file indicates a possible fault. Take first line “P 2 A11 D1.3 SA1 3 0” as an example:

P2 indicates the second step of output response sequence has a fault. It means the actual response is different from the truth value.

A11 indicates which chip pin has a fault. A11 is the label of certain output.

D1.3 indicates the third chip pin of component D1 which may cause the fault of A11.

SA1 indicates a fault with display of 1. Two kinds of fault normally occur in digital circuit: display of 0 (SA0) and display of 1 (SA1).

Three indicates the fault probability in node D1.3. It is actually the number of times the node D1.3 appears in fault dictionary.

The linkage of fragments of data listed above shows the complete fault data which implicates that the fault display of 1 in chip pin D1.3 may cause the fault of output pin A11 in its 2nd step.

The test and detection platform (Fig. 2) design includes designs of diagnosis interface circuit, test program based on VXI and fault location grogram. Test and detection platform software design uses Lab Windows/CVI. Its integrated platform, interactive programming, plentiful function panels and library functions make programming easy.

When the system runs, the automatic calling of fault dictionary, node truth table, pin connection table as well as the relevant files deeded in probe location is first selected according to diagnostic object. Then followed by interface circuit self checking and identification. The access to the corresponding tested circuit is suggested after the self checking and identification are passed. Test and detection program drives SR192 module in VXI bus device to apply pumping signal compiled in simulation to tested circuit and read its response. The possible fault

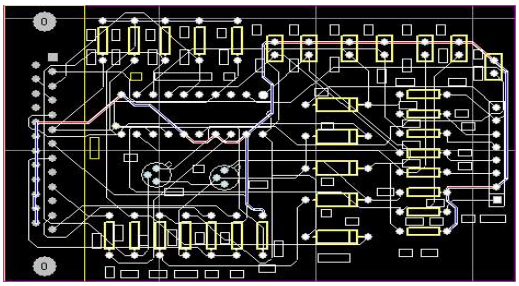

Fig. 3: PCB of SPF

can be identified with the help of circuit response and simulation output files. If necessary, the image-guided probe is used to test the possible fault points to pinpoint accurately the fault of certain component pin.

METHOD OF PCB PICTURE-LOCATION

Due to the limitation of circuit observability and testing vectors, the diagnosis program can not accurately locate the fault just once in the process of diagnosis. It only detects several possible fault locations and the actual fault can be located through probing these possible fault locations. The probing process is slow and may result in failure because the circuit is complex and users are not quite familiarity with the circuit. Therefore, the new circuit-fault-detection method incorporates PCB picture locating techniques so that the users can locate the fault quickly and accurately.

At present, the design of circuit board uses PROTEL. Produced PCB of SPF (Fig. 3) includes data of original packaging, position and connection. PCB image probe positioning directly obtains the data of image and pin position by using PCB produced from the design of circuit board as position indication of probe in circuit fault detection.

PCB default is stored in binary format. The file needs to be stored in ASCII format in order to analyze its content. This design uses "PROTEL PCB 2.8 ASCII Formatted Output" to produce ASCII. The following is part of file concerning probing data:

```
PCB FILES 6 VERSIONS 2.80
0 528 115 33 3 1 37 0 125 82
COMP
RAD0.1
0 0 17140000 22580000 1 1 0 0 0 0 0 90.000 1 1 1
CS
0 0 17060000 22700000 40000 90.000 0 1 17 0 0 0
0 8000 1 0 0
……
ENDPCB
```

Through the analysis of file structure the following is obtained: The first line is ASCII version identification of PCB. The figures 37 and 125 in second line is respectively the number of components and component pins in circuit board. COMP is the initial identification of each component description. The following two lines are data of components' packaging and their positions. CS is the leading identification of code and model of components. The second line below the first leading identification is the component code. The identification code of components needs to be obtained. CP is the initial identification of data of each pin of components. The 3rd and fourth figures of the following line are the pin coordinate. The next line is serial number of component pin. The end identification of each component description is ENDCOMP. In the process of image probe positioning, the pin needs to be in the coordinate of left bottom of circuit board. Therefore the data of boundary size of circuit board needs to be obtained. When circuit board is drawn through PROTEL, its boundary is usually set in the forbidden routing layer which has the serial number 28. FT is the initial identification of the description of each connecting line in the file. The eighth figure of following data is the code of layer where the connecting line is located. From third to sixth figures are endpoint data of connecting line. The data of boundary position of circuit board can be obtained from layer of code 28.

In PCB produced from PROTEL, the display status of each layer can be set by clicking Layers under the menu Design/Options. The pictures including components and boundary of circuit board needed in probe positioning can be obtained only by opening three layers of TopOverlay, MultiLayer and KeepOutLayer. The BMP of the images that are used in position indication can be obtained directly through grasping image software and it can also be exported in PROTEL as DWG or DXF and transformed to BMP through AUTOCAD.

During detection the circuit board that is being diagnosed is connected to VXI of bus device. In order to let users compare the image of probe positioning and circuit board, a function is created that the picture can be rotated in 90°integer multiples. In Lab Window/CVI file can be managed and pictures from different angles can be obtained. To ensure the diagnostic speed, the rotation function of drawing software is used to produce corresponding files which are called respectively according to the select angles in the process of detection.

The previous data of component pins and circuit board boundary position obtained from PCB considers the left bottom of working window as origin of coordinates and mil as the measurement. During the picture probe positioning, the pictures being used are inside the boundary. Therefore, the coordinates should be shifted first. Suppose the coordinates obtained from PCB are PcbX, PcbY. The left bottom coordinates in circuit board boundary are MinX, MinY. The right top coordinates are MaxX, MaxY. After the shifting of origin of coordinates to left bottom of circuit board and linear transform, the coordinates in circuit board are transformed to x, y:

$$\begin{cases} x = k(PcbX - MinX) \\ y = k(PcbY - MinY) \end{cases} \quad (1)$$

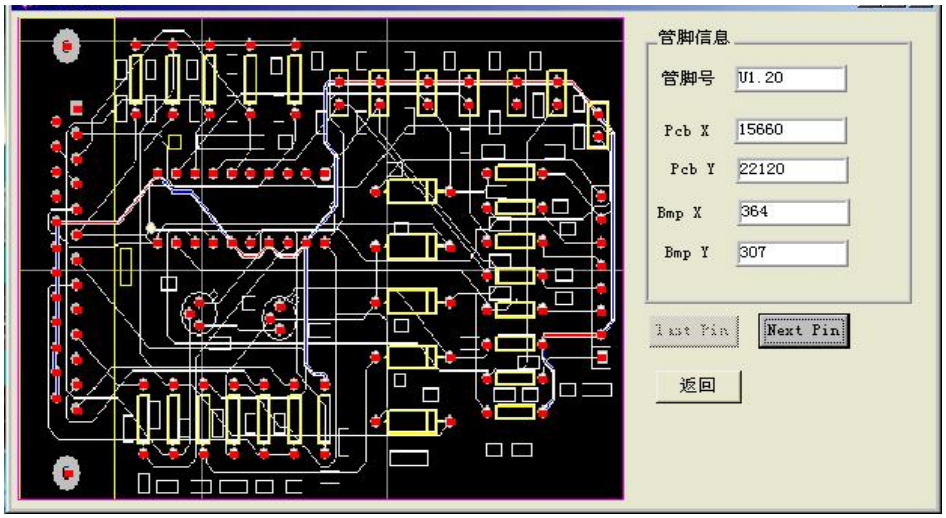

Fig. 4: Pin data of PCB

The left bottom and right top coordinates in circuit board are transformed to 0, 0 and Xmax, Ymax.

The pictures rotate counterclockwise in n×90°and then display n = 0, 1, 2 and 3. Since the obtained pin coordinates consider left bottom of circuit board as the origin of coordinates and the origin of coordinates in GRAPH is in left top of visual area, component pin coordinate x, y should be transformed to coordinate u, v in GRAPH when indication spot piloting the probe is given. The transformation formula is as follows:

$$\begin{bmatrix} u \\ v \end{bmatrix} = \begin{bmatrix} \sin\frac{(n+1)\pi}{2} & \sin\frac{(n+2)\pi}{2} \\ \sin\frac{(n+2)\pi}{2} & \sin\frac{(n+3)\pi}{2} \end{bmatrix} \begin{bmatrix} x \\ y \end{bmatrix} + \begin{bmatrix} \sigma(2-n)\sigma(1-n) \\ \sigma(1-n)\sigma(0-n) \end{bmatrix} \begin{bmatrix} x_{\max} \\ y_{\max} \end{bmatrix} \quad (2)$$

$$\sigma(i) = \begin{cases} 1, i = 0 \\ 0, i \neq 0 \end{cases} \quad (3)$$

Plot Point () is used to draw the indication spot that guides the probe in point (u, v) of GRAPH. To ensure the diagnostic speed, only transformation operation of circuit boar boundary and necessary testing points is carried out in display. Each pin data of PCB is shown in Fig. 4.

SOFTWARE DESIGN REQUIREMENTS AND ITS REALIZATION

File organization: To make users to load this file group related to a certain circuit, one user-defined project file (*.JN) is imported and the content is as follows:

```
<fault dictionary file> = "Logic.dic"
<pin net list > = "Logic.ims"
<node true value list > = "Logic.exp"
<circuit image file> = "Logic.bmp"
<pin position file> = "Logic.pos"
```

File type is declared in the bracket and the corresponding file name is on the right of the equal sign. Since these files are saved in the same catalog with the project file (*.JN), the formed struct is as follows:

```
structFileGroup
{char strPrj[MAX_PATHNAME_LEN]
//general project name
char strDic[MAX_PATHNAME_LEN]
//fault dictionary
char strIms[MAX_PATHNAME_LEN]
//pin net list
char strExp[MAX_PATHNAME_LEN]
//node true value list
char strBmp[MAX_PATHNAME_LEN]
//circuit image
char strPos[MAX_PATHNAME_LEN]
//pin postion file
}g_FileGroup
```

When loading a project, a file name can be obtained by executing the following statement:

```
sprintf (Search, "<%s>", "fault dictionary file")
strValue = ReadValue_Str(pFileBuffer, Search)
// pFileBuffer is cache of project file
    if ( strValue = = NULL ) return FALSE
strcpy ( g_FileGroup.strDic, Path )
//Path where project file is saved
strcat ( g_FileGroup.strDic, strValue)
SAFE_FREE ( strValue )
```

Design of file operation: Although each file has its own data format, they all belong to text files and each line represents one piece of data. According to this feature, basic function for reading file content is programmed. In addition, the corresponding struct is

designed according to the different structures of all the files, so as to bear the relevant information required during analysis process.

Structure related to fault analysis:

Error structure of output end (struct ErrTable): Since this structure is running through the whole analysis process, it is the most important structure in the program. There are two parts of information: the first is error description occurred in output end and the second is the list of fault points which cause the output end error. The form is as follows:

```
typedef struct tag_ErrTable
{
char Name[20]; char Name[20]; //name of output end, like A11
int Count;
  //how many steps where error occurs
 int ErrPace[STEP_NUM]; //which steps occur errors, like 2 and 3
   ErrNode *ListTail[STEP_NUM+1]; //each step has one chain and the last effective chain is the intersection result
}ErrTable
```

The previous three items in this structure describe the error situation of some output end and they become the search condition in fault dictionary for fault point searching. STEP-NUM in the above structure is a constant, as well as step number of exciter; ErrNode is the other small structure and it is a node in one linked list; pointers at tail nodes of all the chains are saved here.

Struct of current test point: This structure will be used when the analysis is completed and points to be tested are stored in "Result" of the previous structure, for information used for true value comparison is stored in it. The information includes the immediate node connected with this pin, its true value and actual test value:

```
ypedef struct tag_TestPoint //current test point
{
int Index; //serial number in g-ErrOut.Result
char Name[20]; //name of check point
char NodeName[20]; //name of node connected with check pin; in True Value structure
char NodeName[20]; //
char TrueValue[100]; //true value
char CurValue[100]; //actual value
}TestPoint
```

Design of fault point storage mode: Many uncertainties exist during the fault analysis of circuit, which are mainly reflected in the following aspects:

Where fault occurs, different fault points cause different error responses at output ends. That is to say, output ends where error responses are different, the number of output ends where error occurs is different and error step number for each output end is also different. For example, in the circuits used in this graduation design, the error D20.9 SA1 only will cause error response from the output end F12 and the steps where error occurs are Step 3 and Step 8. However, error D5.1 SA0 will cause errors to output ends from A11, A12, A13…to A33, A34 and A35. The fault analysis method adopted by us checks all the output ends where error response occurs and then performs analysis.

In addition, the number of fault points that cause error to a certain step of a certain output end is also different. For example, error in second step of A11 may be caused by fault of these points. Therefore, storage method of linked list is adopted for this program. One possible fault point and fault cause will be stored in each node, like "D5.1 SA1". In this way, the node can be easily deleted, sequenced or moved in the linked list. The node structure is shown as follows:

```
typedef struct Node //define a node in linked list
{
{char Err[20]; //fault point and fault cause
struct Node *pNext; //point to the next fault point
}ErrNode
```

CONCLUSION

The method of fault detection realizes 96.59% of fault coverage rate of excitations. The PCB picture-location techniques are used to clearly and vividly display the probe position. It is very convenient for users to reduce the testing failure and raise the efficiency in circuit fault diagnosis.

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