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Research Article

Designs of 2P-2P2N Energy Recovery Logic Circuits

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Abstract: In this study, we propose a P-type energy recovery logic named as 2P-2P2N to reduce the leakage dissipations in nanometer CMOS processes with gate oxide materials. A combinational circuit 4-bit carry look-ahead adder and a sequential circuit *D* flip-flop are realized. Near threshold techniques are used to reduce their power dissipations. All the circuits are simulated by HSPICE using 65 nm PTM technology. The results show that the 2P-2P2N circuits adopting near threshold techniques consume about 82.9-88.4% less power than conventional static CMOS logic and about 45.6-53.2% less power than 2N-2N2P adiabatic logic.

Keywords: 2P-2P2N, adiabatic circuits, leakage power, low power, near-threshold techniques

INTRODUCTION

Before the CMOS process is scaled into 130 nm process, dynamic energy loss has always dominated power dissipation, while leakage power is often ignored (Fallah and Pedram, 2005). With the feature size of integrated circuits continues to reduce, the leakage dissipation caused catches up with the dynamic power consumption gradually and is becoming an important factor in low-power design. The power consumptions of integrated circuits are attracting more attention of designers (Kim *et al.*, 2003).

There are two main sources of leakage currents in CMOS circuits: sub-threshold leakage current due to very low threshold voltage and gate leakage current due to very thin gate oxide (Roy *et al.*, 2003). With the CMOS technology approaching the 100-nm regime, the current leaking through the gate oxide is becoming an important component of power consumption and it could surpass weak inversion and DIBL as a dominant leakage mechanism in the future as oxides get thinner. In 45-nm generation and beyond, the metal gate technology is therefore applied to reduce the gate leakage current. However, the gate leakage issue still exists in the 90 and 65 nm technologies that are currently used in production without metal gate structure.

Several leakage reduction techniques, such as MTCMOS power-gating technique (Fallah and Pedram, 2005) gate-length biasing techniques (Gupta *et al*., 2006) and input vector control have been proposed in recent years (Abdullah *et al.*, 2004). However, these works focus mostly on reducing leakage power caused by sub-threshold leakage currents (Hu *et al.*, 2011). Recently, some works have been reported on how to reduce the gate leakage current in advanced CMOS processes using gate oxide materials, such as analytical modeling for gate leakage and gate leakage reduction for SRAM and domino circuits (Hu *et al.*, 2011).

Adiabatic logic is an attractive low-power approach by utilizing AC voltage supplies (power-clocks) to recycle the dynamic energy of circuits instead of being dissipated as heat (Kramer *et al.*, 1995). However, as the aggressive scaling of device dimensions and threshold voltage have significantly increased leakage current exponentially in adiabatic circuits (Hu and Yu, 2012).

Base on the fact that PMOS transistors have an order of magnitude smaller gate leakage than NMOS ones for the nanometer CMOS processes with gate oxide materials (Hamzaoglu and Stan, 2002), this study proposes a P-type efficient charge recovery logic named as 2P-2P2N to reduce the leakage dissipations in nanometer CMOS processes with gate oxide materials. A combinational circuit 4-bit carry look-ahead adder and a sequential circuit D flip-flop are realized. Near threshold techniques are used to reduce their power dissipations. All the circuits are simulated by HSPICE using 65 nm PTM technology. The results show that the 2P-2P2N circuits adopting near threshold techniques consume about 82.9-88.4% less power than conventional static CMOS logic and about 45.6-53.2% less power than 2N-2N2P adiabatic logic.

2P-2P2N LOGIC CIRCUITS

The basic structure of a 2P-2P2N logic circuit is shown in Fig. 1a. It is also a dual-rail adiabatic logic

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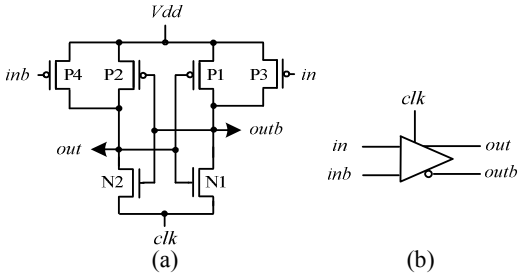

Fig. 1: (a) The basic structure of a 2P-2P2N buffer and (b) the symbol of buffer

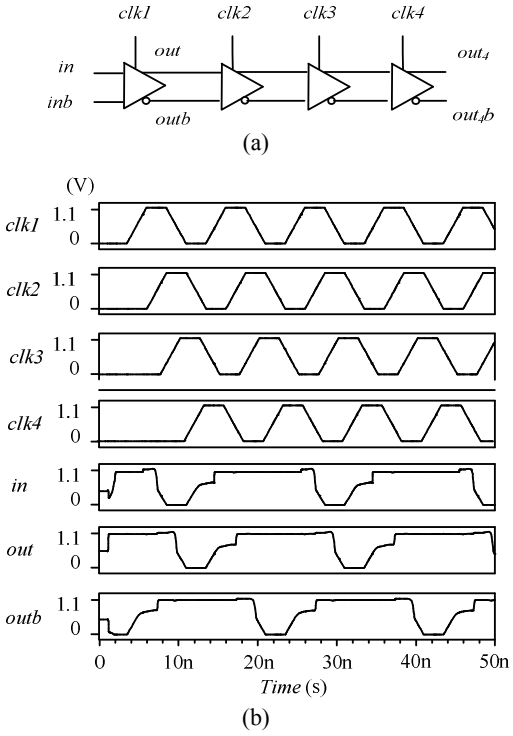

Fig. 2: (a) Cascaded scheme for 2P-2P2N gates and (b) simulation waveforms

family similar to other existing adiabatic circuits, which is composed of two main parts: the logic function block and the load driven block. However, in this structure, all the logic function blocks consist of PMOS transistors (P3 and P4) only and the load driven block consists of a pair of transmission gates (P1, N1 and P2, N2). The transistors N1 and N2 are used for energy recovery. The clamp transistors P1 and P2 make the un-driven outputs node to *Vdd*.

In Fig. 1b, a 2P-2P2N gate is supplied by a single-phase power-clock. In Fig. 2a, four cascaded 2P-2P2N gates can be driven by four-phase power-clocks (*clk1-clk4*). The simulation waveforms of input and output of the cascaded 2P-2P2N gates are shown in Fig. 2b.

The total energy dissipation consists of consumption of the power-clock and consumption of the source voltage *Vdd*. The experiments results in Fig. 3

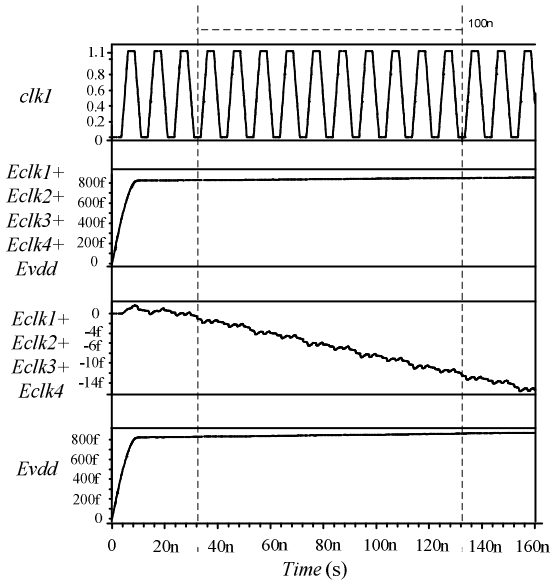

Fig. 3: Energy consumption of a 2P-2P2N buffer

show that energy dissipation of the power-clock (*clk1-clk4*) is negative and decrease with time. It means that the energy is recovering as time grows. Since the characteristics of PMOS are completely contrary to those of NMOS, the NMOS is absorbing energy from power-clock, while the PMOS is providing energy that is absorbed before from source voltage *vdd* to power-clock. Therefore, the dissipation of power-clock is in negative growth and the dissipation of source voltage *Vdd* changes sharply at first and then grows slightly.

DESIGNS OF 2P-2P2N CIRCUITS

2P-2P2N combination circuits: As described before, the logic function block in a 2P-2P2N buffer consists of P3 and P4. The other logic circuits can be realized by using the corresponding logic function block to replace the transistor P3 and P4 of the 2P-2P2N buffer. 2P-2P2N logic gate circuits are shown in Fig. 4.

Four-bit carry look-ahead adder (4-bit CLA for short) is a typical combination circuit. The 4-bit CLA based on 2P-2P2N is shown in Fig. 5. It can be seen that all logic gates in the 4-bit CLA based on 2P-2P2N are enabled successively by four-phase power clocks (*clk*1, *clk*2, *clk*3 and *clk*4).

The 4-bit CLA based on 2P-2P2N, 2N-2N2P and static CMOS are implemented and simulated by HSPICE using 65 nm PTM technology. The frequency of the power clocks is ranging from 50 to 250 MHz and its peak voltage (*Vdd*) is normally 1.1V. The energy consumptions of the 4-bit CLA based on 2P-2P2N, 2N-2N2P and static CMOS are compared, as shown in Table 1. The results show that the 4-bit CLA based on 2P-2P2N obtains energy savings of 71.0-76.4% compared with standard static CMOS, 68.6-75.1% compared with 2P-2P2N.

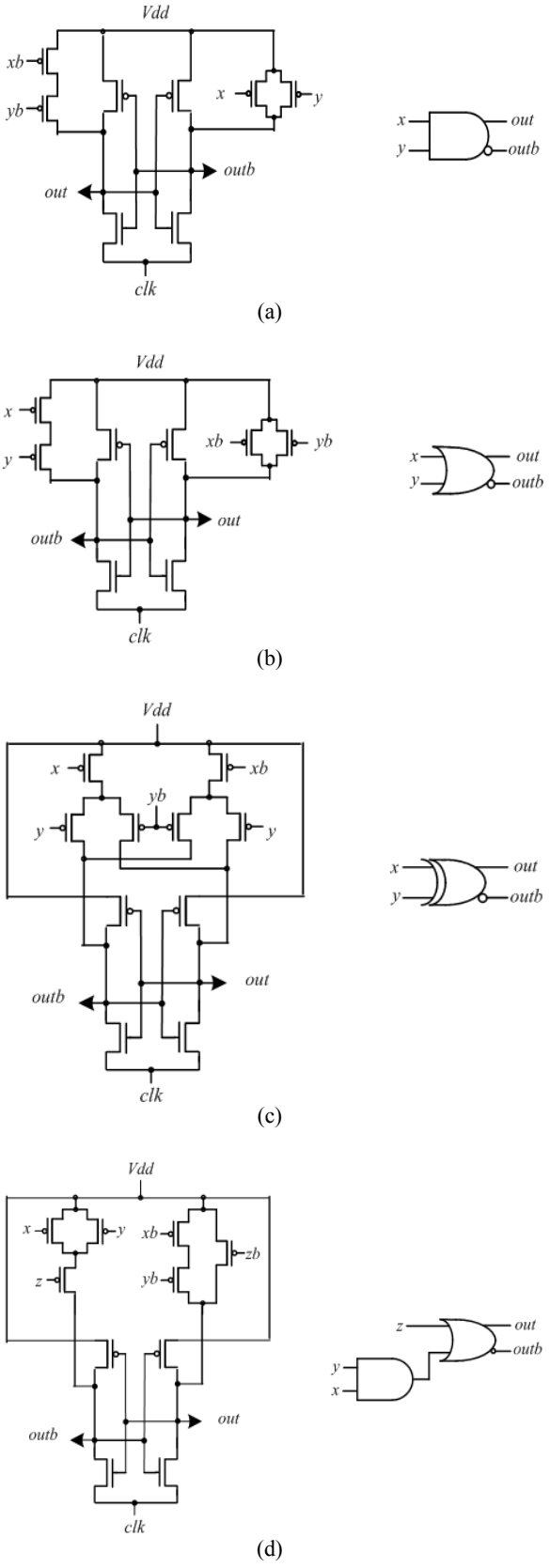

Fig. 4: Logic gates based on 2P-2P2N (a) AND, (b) OR, (c) XOR, (d) AND-OR

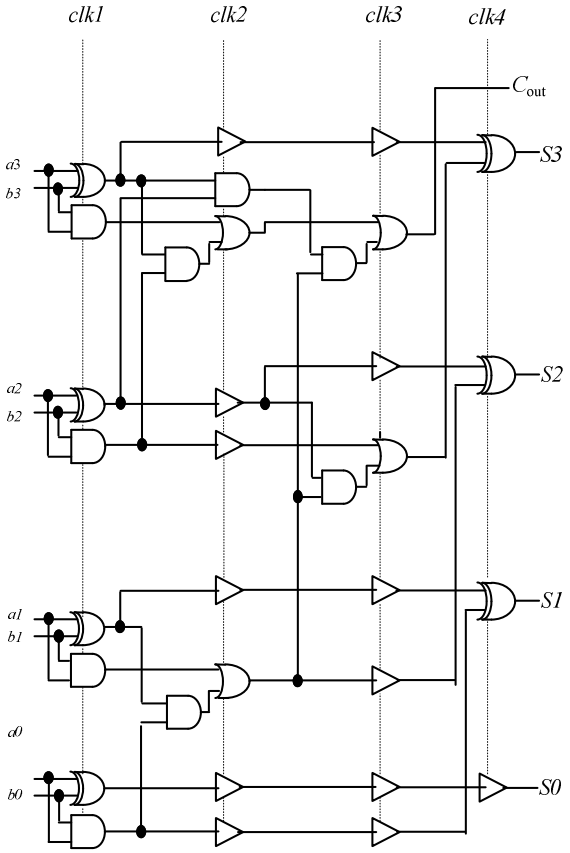

Fig. 5: 4-bit CLA based on 2P-2P2N

Table 1: Energy dissipations of 4-bit CLA in *Vdd* = 1.1V in different frequencies

	Total dissipation (fJ)		
Frequency (MHz)	CMOS	2N-2N2P	2P-2P2N
50	63.60	15.81	15.0
100	62.51	15.89	15.0
150	60.90	16.87	16.1
200	58.80	17.98	16.0
250	60.30	18.94	17.5

Table 2: Energy dissipations of DFF at *Vdd* = 1.1V in different frequencies

	Total dissipation (fJ)		
Frequency (MHz)	CMOS	2N-2N2P	2P-2P2N
50	6.22	2.002	1.90
100	6.52	2.235	2.10
150	6.04	2.416	2.30
200	5.94	2.617	2.46
250	5.96	2.812	2.59

2P-2P2N sequence circuits: D Flip-Flop (DFF for short) is a typical basic element of the sequence circuits. As shown in Fig. 6. DFF consists of four buffers and those four buffers in the DFF based on 2P-2P2N are enabled successively by four-phase power clocks (*clk*1, *clk*2, *clk*3 and *clk*4).

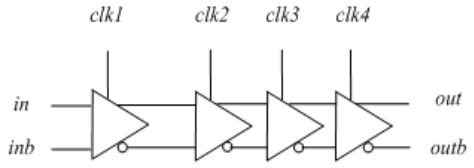

Fig. 6: *D* flip-flop based on 2P-2P2N

The DFF based on 2P-2P2N, 2N-2N2P and static CMOS are implemented and simulated by HSPICE using 65 nm PTM technology. The frequency of the power clocks is ranging from 50 to 250 MHz and its peak voltage (*Vdd*) is 1.1V. The energy consumptions of the DFF based on 2P-2P2N, 2N-2N2P and static CMOS are compared, as shown in Table 2. The results show that the DFF based on 2P-2P2N obtains energy savings of 52.8-67.8% compared with standard static CMOS, 52.8-69.5% compared with 2P-2P2N.

2P-2P2N CIRCUITS WITH NEAR-THRESHOLD TECHNOLOGY

The 2P-2P2N logic circuits can save much more energy than 2N-2N2P and static CMOS circuits. In this section, near-threshold techniques are adopted to further reduce power consumption of 2P-2P2N logic circuits. As described before, near threshold techniques is an attractive energy saving approach, which scales dynamic energy dissipation down quadratic ally by reducing the supply voltage to near threshold voltage of transistors at the cost of the performance loss (Dreslinski *et al.*, 2010).

Figure 7 shows the max operating frequencies of a 2P-2P2N buffer in different supply voltages. At each supply voltage, the maximum operating frequency is obtained, where the CPAL buffer has correct logic function. It is shown that the maximum operating frequency reduces from 480 to 7 MHz quadratic approximately, in the supply voltage decreases from 1.1 to 0.2 V, respectively.

Figure 8, 9 and 10 are energy dissipations of 2P-2P2N and 2N-2N2P and static CMOS logic buffers in different voltages at 1, 10 and 100 MHz, respectively. Energy dissipation of 2P-2P2N logic circuits varies greatly at 1 MHz, but the energy dissipation is least and changes gently at 10 and 100 MHz. It is suggested that the performances of 2P-2P2N logic circuits are affected least by supply voltages changing at 10 and 100 MHz. In other words, 2P-2P2N logic circuits are more suitable for adopting near threshold technology than 2N-2N2P and static CMOS logic circuits.

2P-2P2N combination circuits: The simulation waveforms of 4-bit CLA using near threshold technology (0.7 V medium source voltage of the power-clocks) is shown in Fig. 11. As shown in Fig. 11, the 4-bit CLA has functions correctly at 0.7 V.

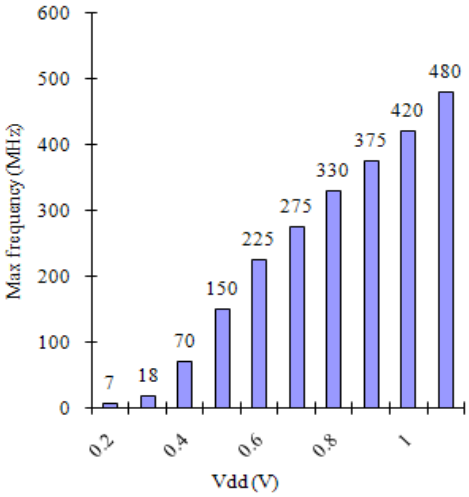

Fig. 7: Max operating frequency of a 2P-2P2N buffer in different voltages

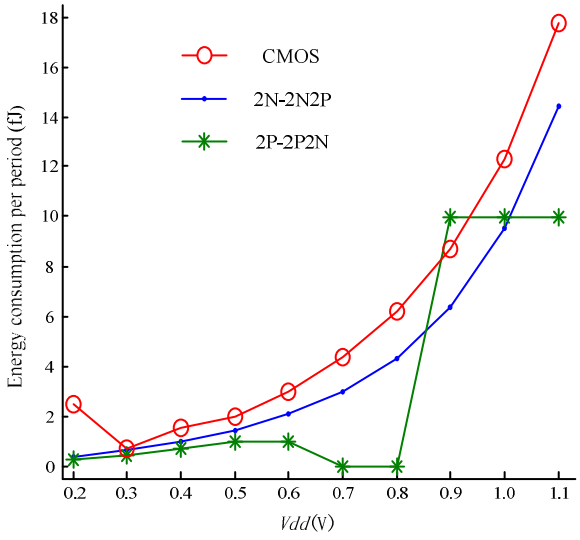

Fig. 8: Energy dissipations of 2P-2P2N, 2N-2N2P and static CMOS buffers in different voltages at 1 MHz

Table 3: Energy dissipations of the 4-bit CLA at *Vdd* = 0.7 V in different frequencies

	Total dissipation (fJ)		
Frequency (MHz)	CMOS	2N-2N2P	2P-2P2N
50	23.25	8.54	7.4
100	22.96	9.44	8.0
150	22.46	10.13	8.8
200	22.43	10.75	9.4
250	22.20	11.20	10.3

The energy consumptions of the 4-bit CLA based on 2P-2P2N in *Vdd* = 0.7V at different frequencies, 2N-2N2P and static CMOS are compared, as shown in Table 3. The simulation results show that the 4-bit CLA based on 2P-2P2N obtains energy savings of 53.6-68.2% compared with standard static CMOS, 49.5-

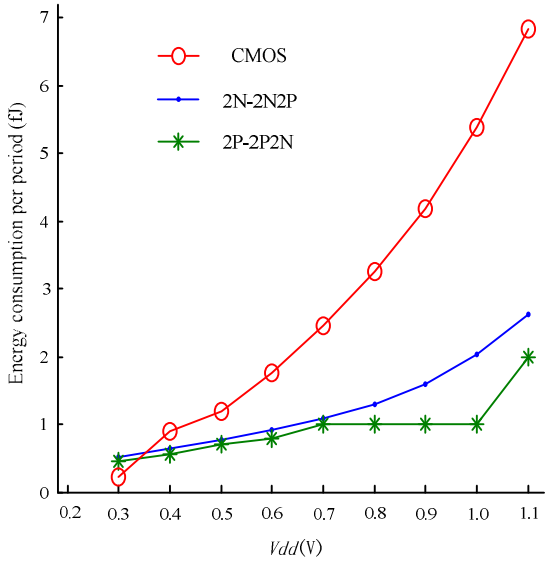

Fig. 9: Energy dissipations of 2P-2P2N2P-2P2N, 2N-2N2P, and static CMOS buffers in different voltages at 10 MHz

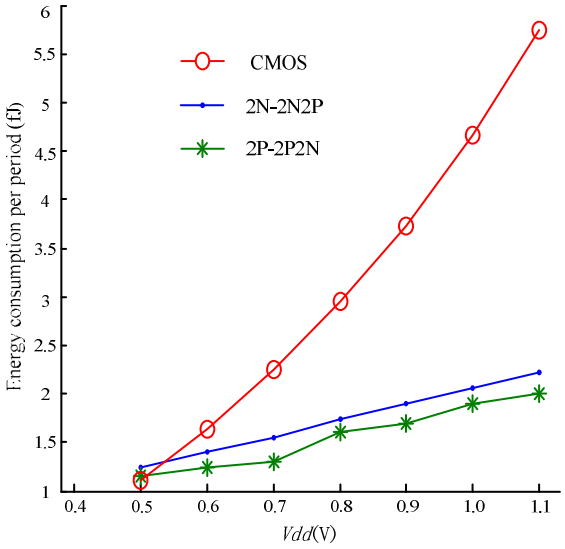

Fig. 10: Energy dissipations of 2P-2P2N2P-2P2N, 2N-2N2P, and static CMOS buffers in different voltages at 100 MHz

63.3% compared with 2P-2P2N, using near threshold technology.

2P-2P2N sequence circuits: Figure 12 shows simulation waveforms of D flip-flop using near threshold technology (0.7 V medium source voltage of the power-clocks. As shown in Fig. 12, the D flip-flop has functions correctly at 0.7 V.

The energy consumptions of the DFF based on 2P-2P2N, 2N-2N2P and static CMOS at *Vdd* = 0.7V are compared, as shown in Table 4. The results show that

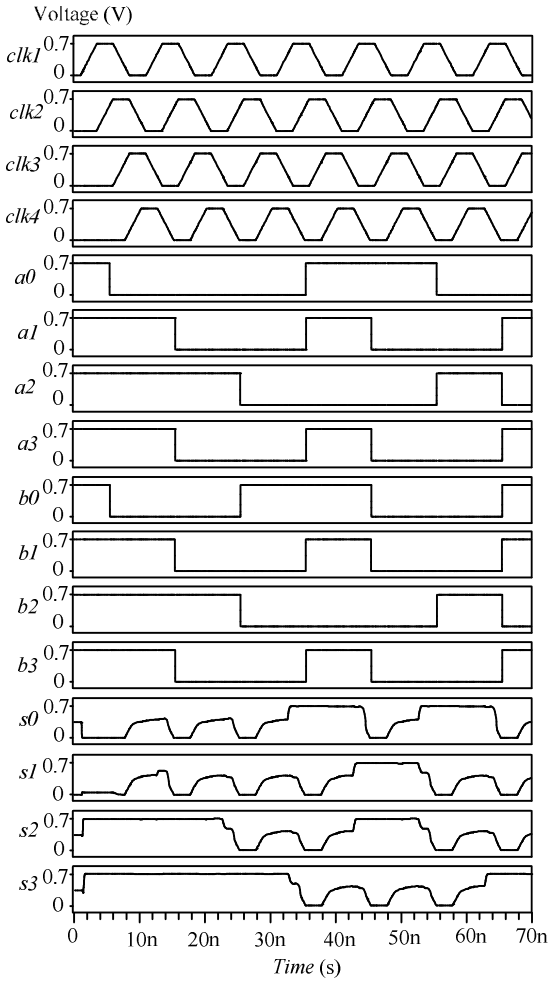

Fig. 11: Simulated waveforms of 4-bit CLA using near threshold technology

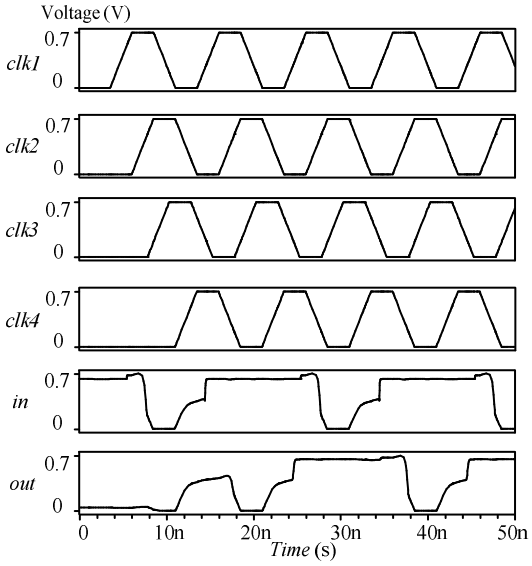

Fig. 12: Simulated waveforms of D flip-flop using near threshold technology

Table 4: Energy dissipations of *DFF* at *Vdd* = 1.1 V in different frequencies

	Total dissipation (fJ)		
Frequency (MHz)	CMOS	2N-2N2P	2P-2P2N
50	6.22	2.002	1.90
100	6.52	2.235	2.10
150	6.04	2.416	2.30
200	5.94	2.617	2.46
250	5.96	2.812	2.59

using near threshold technology the DFF based on 2P-2P2N obtains energy savings of 19.3-44.4% compared with standard static CMOS, 13.5-38.6% compared with 2P-2P2N.

CONCLUSION

A P-type efficient charge recovery logic named as 2P-2P2N to reduce the leakage dissipations in nanometer CMOS processes with gate oxide materials has been proposed in this study. Base on the fact that PMOS transistors have an order of magnitude smaller gate leakage than NMOS ones for the nanometer CMOS processes with gate oxide materials, the proposed circuits attain more lower power than the other similar circuits. A 4-bit carry look-ahead adder and a *D* flip-flop are realized. Near threshold techniques are used to reduce their power dissipations. The results show that the 2P-2P2N circuits adopting near threshold techniques consume about 82.9-88.4% less power than conventional static CMOS logic and about 45.6-53.2% less power than 2N-2N2P adiabatic logic.

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