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Research Article

Near-threshold Computing of Single-rail MOS Current Mode Logic Circuits

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Abstract: Scaling supply voltage is an efficient technique to achieve low power-delay product. This study presents low-power Single-Rail MOS Current Mode Logic (SRMCML) circuits which operate on near-threshold region. The near-threshold operations for the basic SRMCML circuits such as inverter/buffer, OR2/NOR2 and 2/NAND2, OR3/NOR3 and XOR3/NXOR3 are investigated. All circuits are simulated with HSPICE at the SMIC 130 nm CMOS process by varying supply voltage from 0.6V to 1.3V with 0.1V steps. Based on the simulation results, lowering supply voltage is advantageous. The power dissipations of the proposed near-threshold SRMCML basic gates are almost the same as the conventional Dual-Rail MCML (DRMCML) circuits and the delay of the SRMCML is less than the DRMCML because of its single-rail scheme.

Keywords: High-speed applications, low power, MOS current mode logic, near-threshold computing, single-rail structure

INTRODUCTION

High performance, low power and small area are the main objectives in IC design. MOS Current Mode Logic (MCML) techniques are usually used for high-speed applications such as high-speed processors and Gbps multiplexers for optical transceivers (Musicer and Rabaey, 2000). With the growing uses of portable and wireless electronic systems, energy-efficient designs have become more and more important in integrated circuits (Zhang *et al.*, 2011). MCML circuits have large static power due to its constant operation current (Alioto and Palumbo, 2003). Therefore, the power dissipation is much larger than the conventional CMOS ones at low frequencies (Hassan *et al.*, 2005).

In conventional CMOS, the energy consumption has two components: switching energy, short energy and static energy. A direct solution for reducing energy consumption is to scale down supply voltage, since the switching energy is reduced quadratically and leakage dissipation decreased linearly as supply voltage scales (Hu and Yu, 2012). Scaling supply voltage to sub-threshold region can reach minimum energy consumption but only suits for ultra low power design (f = 10 KHz to 5 MHz) (Dreslinski *et al.*, 2010). In order to attain more extensive application, scaling supply voltage to near-threshold region is an attractive approach especially suit for mid performances (f = 5 to 100 MHz).

Similar to conventional CMOS, the power dissipations of MCML circuits can also be reduced by lowering source voltage, since the power dissipations of MCML circuits are proportional to their source voltages. Differently from the conventional CMOS, scaling down supply voltage of MCML circuits doesn't cause the decay of performance, since their speed is independent of the source voltage (Yamashina and Yamada, 1992). However, the supply voltage of the MCML circuits has a minimum limit, at which the pull-down network NMOS transistors and the current source transistor should operate at velocity saturation region, resulting in a large minimum source voltage.

The current almost all MCML circuits are realized with dual-rail scheme (Tanabe, 2001). The dual-rail logic circuits increase extra area overhead and layout complexity (Ni and Hu, 2011). Also, for multi-level dual-rail MCML (DRMCML) circuits, such as three or more multi-level DRMCML circuits, the more high supply voltage should be used to ensure their correct operation because of more series MOS transistors of the multi-level DRMCML circuits, so that more power is dissipated.

In this study, low-power Single-Rail MOS Current Mode Logic (SRMCML) circuits which operate on near-threshold region are addressed. The near-threshold operations for the basic SRMCML circuits such as inverter/buffer, OR2/NOR2 and2/NAND2, OR3/NOR3 and XOR3/NXOR3 are investigated. For the OR/NOR logic cell, the proposed SRMCML can avoid the devices in series configuration, since the logic evaluation block of the SRMCML OR/NOR logic cell can be realized by only using MOS transistors in parallel. This can further reduce power dissipations because of the low source voltage. The delay of the near-threshold SRMCML

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circuits is less than the DRMCML ones because of their single-rail scheme.

SRMCML AND DRMCML CIRCUITS

DRMCML circuits: The DRMCML inverter/buffer and its bias circuit are shown in Fig. 1. The DRMCML inverter is composed of three main parts: the load transistors P1 and P2, the full differential Pull Down Network (PDN) consisting of N1 and N2 and the current source transistor Ns. The load transistors are designed to operate at linear region with the auxiliary of the control voltage V_{ref} produced by the bias circuit, which also controls the output logic swings. The NMOS PDN (N1 and N2) are used to perform logic operation. Ns is used to provide the constant current source, which is mirrored from the current source in the bias circuit. In the DRMCML, two signals V_{rfp} and V_{rfn} are generated from the bias circuit to ensure the proper operating for output voltage swings and to provide the constant bias current.

The operation of DRMCML circuits is performed in the current domain. The pull down network switches the constant current between two branches and then the load converts the current to output voltage swings. The high and low digital logic levels are $V_{OH} = V_{DD}$ and $V_{OL} = V_{DD} - I_B R_D$, respectively, where R_D is the PMOS load resistance. The logic swing is $\Delta V = V_{OH} - V_{OL} = I_B R_D$.

DRMCML is a type of differential logic circuit with dual-terminal input and dual-terminal output ports like DCVSL and DSL. The two-input and three-input AND/NAND, OR/NOR and XOR/XNOR gates based on DRMCML are shown Fig. 2 to 4, respectively.

SRMCML circuits: The current MCML circuits are mostly realized with dual-rail scheme. The dual-rail logic circuits increase extra area overhead and the complexity of the layout place and route. In this section, a single-rail realization scheme of MCML circuits is presented. The design methods of the basic Single-Rail MCML (SRMCML) circuits are also presented, such as AND2/NAND2 and XOR3/XNOR3.

Compared with the DRMCML circuits, SRMCML circuits should have a simple structure. A direct solution for realizing the single rail MCML is shown in Fig. 5b, which is realized with the half of the Fig. 5a. Obviously, it is Pseudo-NMOS logic with a voltage-mode operation, which loses the fast performance of the current-mode operations.

Another possible solution for realizing the single rail MCML is shown in Fig. 5c, which is realized with the half of the Fig. 5a with the tail current. Obviously, it is current-mode logic. However, the NMOS of the Fig. 5c cannot work in the switch state, because the voltage of the X point of the Fig. 5c follows the input signal, which is different from the Fig. 5a, where

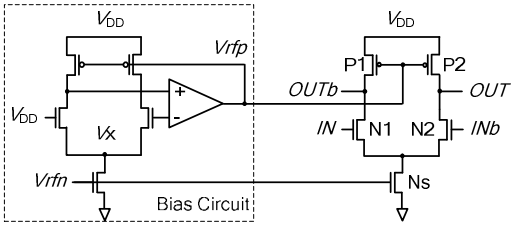

Fig. 1: DRMCML inverter/buffer and its bias circuit

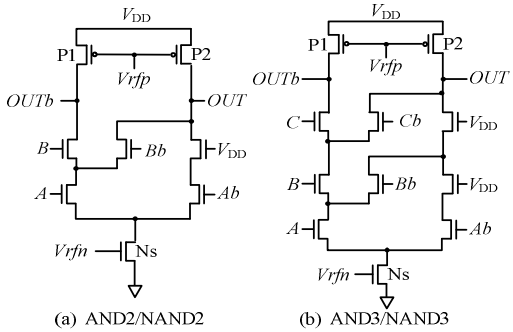

Fig. 2: The two-input and three-input AND/NAND gates based on DRMCML

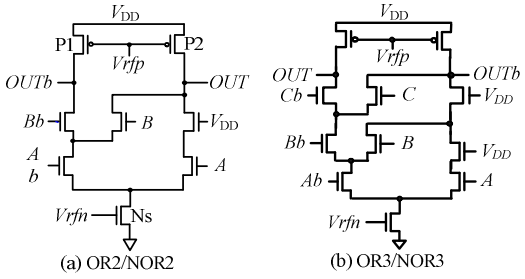

Fig. 3: The two-input and three-input NOR/NOR gates based on DRMCML

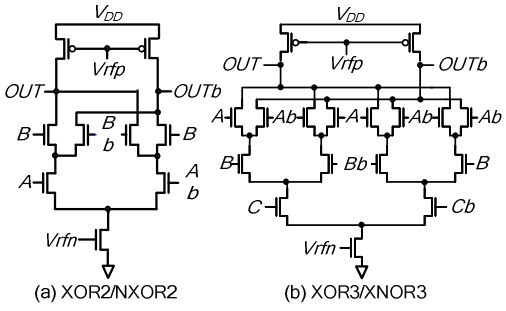

Fig. 4: The two-input and three-input XOR/XNOR gates based on DRMCML

differential work can ensure that the voltage of the X point is almost constant.

A single-rail realization scheme for MCML circuits is shown in Fig. 6. The structure of the Single-Rail MCML (SRMCML) is similar to DRMCML, but a output of the SRMCML is fed back to the gate of the

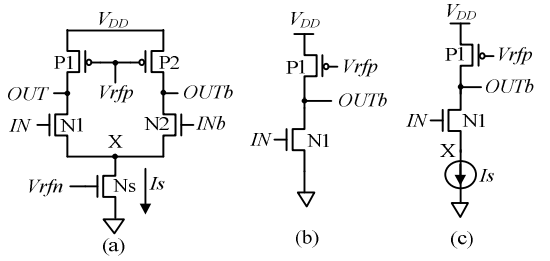

Fig. 5: The possible scheme for realizing single-rail MCML, (a) DRMCML, (b) pseudo-NMOS logic, (c) pseudo-NMOS logic with current-mode operation

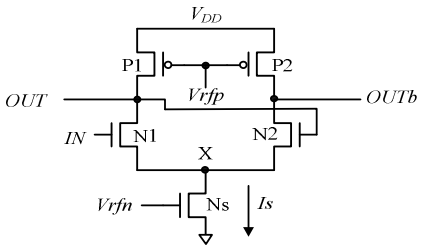

Fig. 6: The realization of single rail MCML

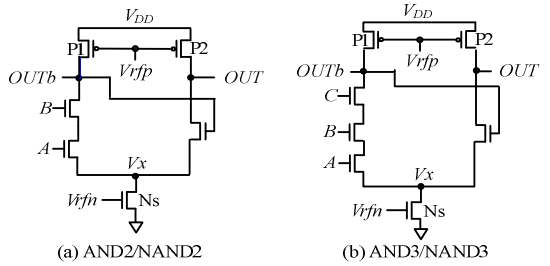

Fig. 7: The two-input and three-input AND/NAND gates based on SRMCML

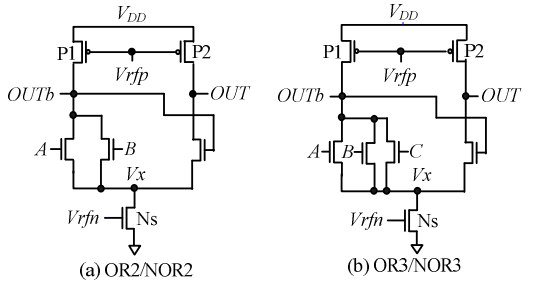

Fig. 8: The two-input and three-input NOR/NOR gates based on SRMCML

the NMOS transistor N2. The HSPICE simulations show that the proposed SRMCML circuits have correct logic functions.

The basic SRMCML gates, such as OR2/NOR2, OR3/NOR3 and2/NAND2 and 3/NAND3, XOR2/ NXOR2 and XOR3/NXOR3 are shown in the Fig. 5. From Fig. 5, compared with the DRMCML circuits, SRMCML circuits have a simple structure. The single-rail logic circuits reduce the complexity of the layout place and route and thus low delay can be expected. Figure 7 shows the two-input and three-input AND/NAND gates based on SRMCML. Figure 8 shows the two-input and three-input NOR/NOR gates based on SRMCML. Figure 9 shows the two-input and three-input XOR/NXOR gates based on SRMCML.

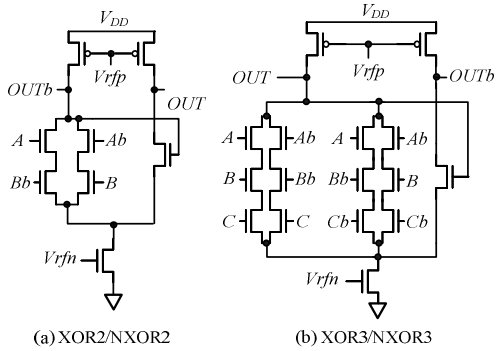

Fig. 9: The two-input and three-input XOR/NXOR gates based on SRMCML

PERFORMANCE METRICS OF MCML CIRCUITS

Power dissipation and delay: Similar to the DRMCML circuits, the important performance metrics of the SRMCML gates include propagation delay and power dissipation. Due to the operating constant current whenever it is either in active mode or in standby mode, the power consumption of a SRMCML gate is independent of the switching frequency and it can been written as:

$$P = V_{DD}.I_B \quad (1)$$

where,
V_{DD} = The supply voltage
I_B = The bias current of the SRMCML gate

For given V_{DD} and I_B, the power dissipation of MCML cells is a constant value. It is independent of both the operation frequencies and fanouts. From (1), the power dissipation of MCML cells is also independent of the logic function. The power dissipation of the SRMCML circuit is linearly proportional to the supply voltage.

The delay time of a MCML cell can be calculated assuming that, at each transition, the whole I_B, ideally, flows through one branch of the differential pair and charges the total load capacitance C, is given by:

$$t_d = 0.69.RC = 0.69 \, . \, C. \equiv \Delta V/I_B \quad (2)$$

where, C is identical load capacitance on the output nodes. The power-delay product is independent of the switching frequency and can be calculated as:

$$PDP = P.t_d = 0.96V_{DD}.\Delta V.C \quad (3)$$

where,

R : The equivalent resistance of one branch of the load PMOS transistor

ΔV : The logic swing of the output nodes, which is generated from the basic circuit

Voltage swing: It is known that the pull down network in SRMCML circuits is regulated by a constant current source. The pull down network steers the current I_B to one of the pull up resistors based upon the logic function. The resistor connected to the current source through the PDN will have a voltage drop equal to $\Delta V = I_B R_D$. Another resistor will not have any current flowing through it and thus its output node will be pulled up to V_{DD}. This voltage swing is generally much smaller than V_{DD}, with a few hundred millivolts.

As seen in (2), it is extremely desirable to reduce the voltage swing as much as possible in order to reduce the propagation delay. The lower limit on the voltage swing is determined by the gain and current switching requirements. The lower bound on the swing must also take into account possible circuit mismatch effects. The upper bound on the voltage swing comes from the nonlinearity of the PMOS loads. As the voltage swing is increased, the PMOS device on the side which is being pulled down is required to move closer to its $V_{GS,sat}$. This leads to eventual entering of the saturation region and extreme nonlinearity. At the same time, V_{DD}-ΔV must be enough low, so that the NMOS of the next MCML circuits can be shut down reliably:

$$(V_{DD} - \Delta V) - (V_{DD} - V_{GS,sat}) < V_{TH,\mathrm{N1}} \Rightarrow \\ \Delta V > V_{GS,sat} - V_{TH,\mathrm{N1}} \quad (4)$$

where, $V_{GS,sat}$ and is $V_{TH,N1}$ the drain-source saturation voltage and the threshold voltage of the NMOS transistor N1, respectively. In this study, the voltage swing is 300 mV although lower swing could be sued with extremely careful layout and noise management. The threshold value of the MOS transistor is 0.282 V.

NEAR-THRETHOLD COMPUTING

The power dissipations of the MCML circuits can be effectively reduced by lowering their source voltage, since the power dissipations of the MCML circuits are linearly proportional to the supply voltage (Wu and Hu, 2011). In order to investigate the performance of the SRMCML basic cells in near-threshold region, the DRMCML and SRMCML AND3/NAND3, OR3/NOR3, XOR2/NXOR2 and XOR3/NXOR3 have been simulated using HSPICE at the 130 nm CMOS process. The device size of PMOS load transistors and current source NMOS transistors is taken with W/L = 8λ/10λ and 16λ/4λ, respectively and λ = 65 nm. The device size of NMOS transistors of the DRMCML differential pair is taken with 4λ/2λ and the device size of NMOS transistors of the SRMCML is taken

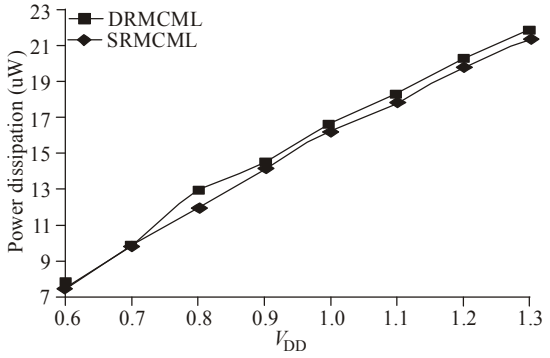

Fig. 10: Power dissipations of DRMCML and SRMCML inverter/buffer

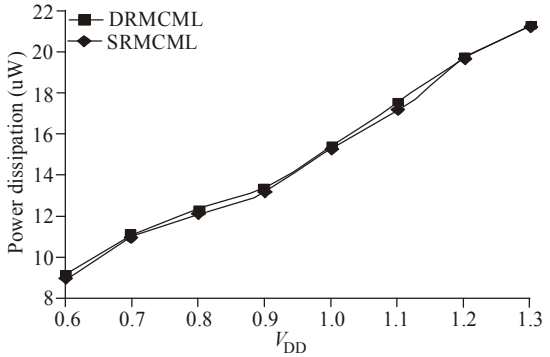

Fig. 11: Power dissipations of DRMCML and SRMCML AND2/NAND2 gates

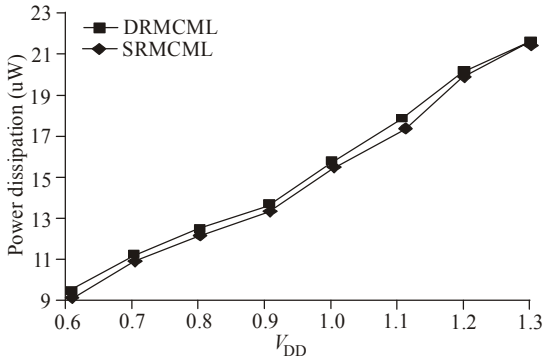

Fig. 12: Power dissipations of DRMCML and SRMCML AND3/NAND3 gates

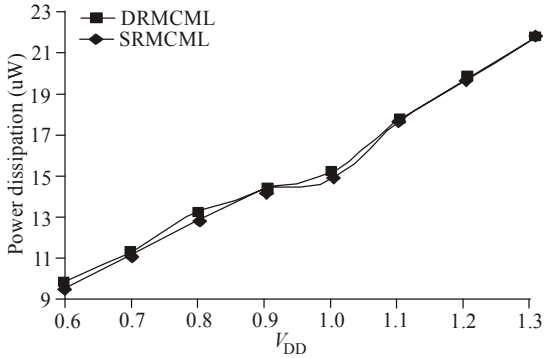

Fig. 13: Power dissipations of DRMCML and SRMCML OR2/NOR2 gates

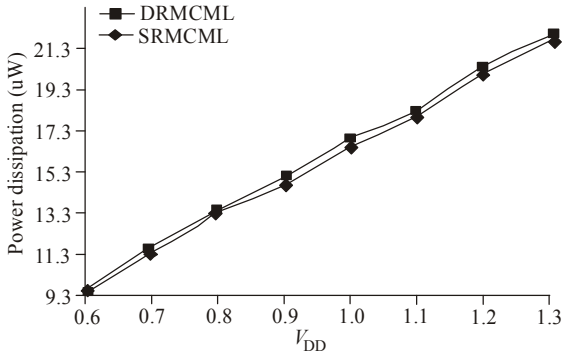

Fig. 14: Power dissipations of DRMCML and SRMCML OR3/NOR3 gates

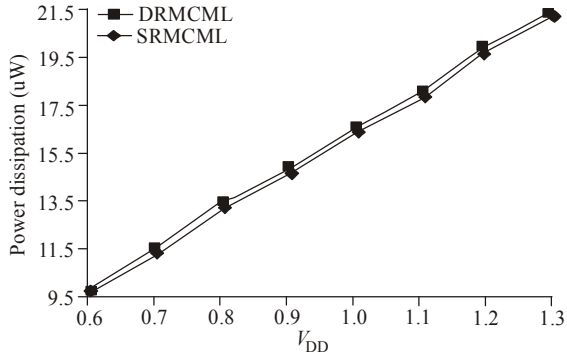

Fig. 15: Power dissipations of DRMCML and SRMCML XOR2/XNOR2 gates

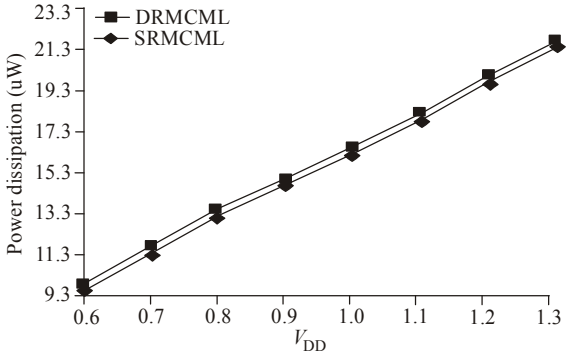

Fig. 16: Power dissipations of DRMCML and SRMCML XOR3/XNOR3 gates

with 4λ/2λ and λ = 65 nm. The bias current of the DRMCML and SRMCML all is 8uA. All the circuits are simulated by source voltage ranging from 0.6V to 1.3V with 0.1V step. The operation frequency is 1 GHz.

Power dissipations: The simulation results of the power dissipation are shown in the Fig. 10 to 16. From Fig. 10 to 16, it can be seen that the power dissipation of the SRMCML and DRMCML circuits is linearly proportional to the supply voltage. The power dissipations of the SRMCML basic gates are almost the same as the DRMCML ones in the near-threshold region. However, the SRMCML circuits have less capacitance than DRMCML ones, because of its single

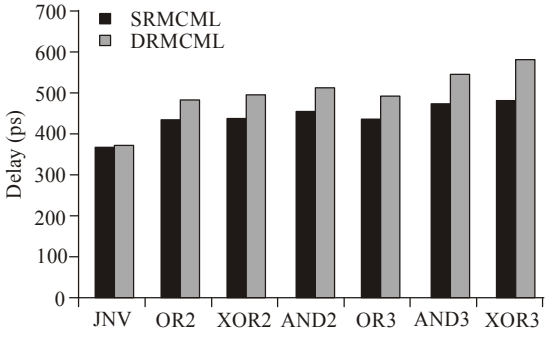

Fig. 17: Delay of SRMCML and DRMCML basic cells

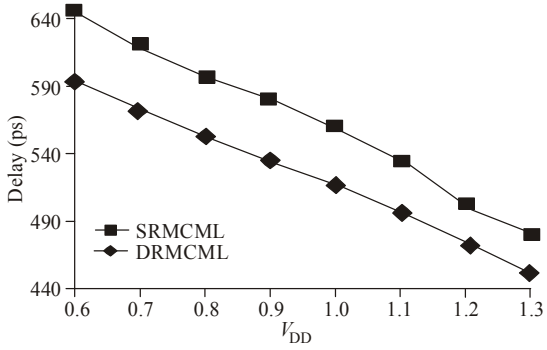

Fig. 18: Delay of SRMCML and DRMCML OR2/NOR2

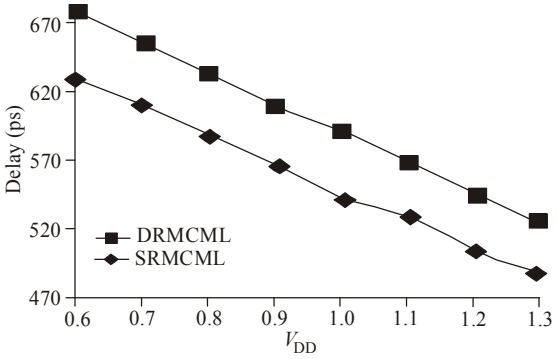

Fig. 19: Delay of SRMCML and DRMCML XOR3/XNOR3

rail scheme. Therefore, it can be expected that of the SRMCML circuit can obtain the small delay.

Delay: The delay for the basic gates based on SRMCML and DRMCML has been simulated with HSPICE. The basic SRMCML and DRMCML circuits such as inverter/buffer and 2/NAND2, OR2/NOR2 and 3/NAND3, OR3/NOR3, XOR2/ XNOR2 and XOR3/XNOR3 at the normal supply voltage (1.3V) are compared in Fig. 17. From Fig. 17, the delay of all basic gates based on SRMCML is smaller than SRMCML one because of its single-rail scheme.

In order to investigate the performance of the SRMCML circuits in near-threshold region, the DRMCML and SRMCML OR2/NOR2 and

XOR3/NXOR3 have been simulated using HSPICE at the 130 nm CMOS process in near-threshold regions. All the circuits are simulated by source voltage ranging from 0.6V to 1.3V with 0.1V step. The simulation results of the delay of the OR2/NOR2 and XOR3/NXOR3 based on SRMCML and DRMCML are shown in the Fig. 18 and 19, respectively.

From Fig. 18 and 19, it can be seen that the delay of the SRMCML circuits is less than the DRMCML ones in the near-threshold regions because of its single-rail scheme. For the OR/NOR logic cell, the proposed SRMCML can avoid the devices in series configuration, since the logic evaluation block of the SRMCML OR/NOR logic cell can be realized by only using MOS transistors in parallel. This can further reduce power dissipations because of the low source voltage.

Moreover, the dual-rail structure of DRMCML circuits increased extra area overhead and the complexity of the layout place and route and thus load capacitance on the circuit nodes in DRMCML circuits is larger than SRMCML ones. For SRMCML, small load capacitance on the circuit nodes results in small circuit delay.

CONCLUSION

High performance, low power and small area are the main objectives in IC design. MOS Current Mode Logic (MCML) techniques are usually used for high-speed applications. With the growing uses of portable and wireless electronic systems, energy-efficient designs have become more and more important in integrated circuits. Scaling supply voltage is an efficient technique to achieve low power-delay product. The current almost all MCML circuits are realized with dual-rail scheme.

In this study, low-power Single-Rail MOS Current Mode Logic (SRMCML) circuits have been addressed, which are suitable for near-threshold operating. For the OR/NOR logic cell, the proposed SRMCML can avoid the devices in series configuration, since the logic evaluation block of the SRMCML OR/NOR logic cell can be realized by only using MOS transistors in parallel. This can further reduce power dissipations because of the low source voltage. The delay of the near-threshold SRMCML circuits is less than the DRMCML ones because of their single-rail scheme.

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