

## Research Article

### A Comparative Study on SOI MOSFETs for Low Power Applications

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**Abstract:** Silicon on Insulator (SOI) technology has become one of the most promising technologies in semiconductor fabrication industry for its numerous advantages. This study presents merits and demerits of different SOIs presented in literatures and a comparative study is done based on several design and performance issues for low power applications. From the study it is found that Fully Depleted SOI MOSFET (FDSOI) technology is preferred due to its thin size, reduced leakage current and improved power consumption characteristics etc. compared to those of PDSOI and bulk silicon technology.

**Keywords:** FDSOI, Low power, MOSFET, PDSOI, SOI

## INTRODUCTION

Rapid growth in semiconductor technology urges the industrial playmaker to compete against them. Moore's Law indicated that the number of transistors on an integrated circuit chip doubles every one and a half years (Moore, 1998; Mack, 2011; Mack, 2003; Bondyopadhyay, 1998; Akter *et al.*, 2008a; Mohd-Yasin *et al.*, 2004; and Reaz *et al.*, 2007). The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is playing a vital role in technology advancement for the past 2 decades (Reaz *et al.*, 2003). MOSFETs offer advantages in performance gain and cost reduction especially in low power application in comparison to others (Tuomi, 2002).

The Fig. 1 shows the cross sectional view of a typical MOSFET which exhibit bilateral symmetry i.e., the channel carriers can be made to flow in either direction, depending on bias polarity. This symmetry is important in certain MOSFET applications. The 2 channel terminals have been named according to which one supply the carriers to the channel and which receives carrier from it and these 2 terms are source and drain, respectively.

In this study, design and performance comparisons are presented among different architectures of SOI, MOSFETs illustrated in the literatures for last 2 decades. From the study it is clear that every PDSOI, MOSFET, FDSOI and MOSFET structural designs have their own advantages and disadvantages and are preferred for particular applications.

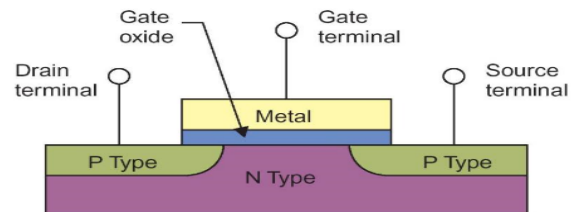


Fig. 1: Cross sectional view of a typical MOSFET

## SOI MOSFET TECHNOLOGY

Silicon on Insulator (SOI) technology has become one of the most promising technologies in semiconductor fabrication industry. The SOI transistor has been introduced by Mueller and Robinson in 1964 (Mueller and Robinson, 1964; Colinge, 1987; Pelella and Fossum, 2002). The Silicon on Insulator features (SOI) technology features a low capacitance which enables high speed operation. That is, the supply voltage can be lowered to cut the power consumption while adequate speed is provided. However, the advantages of SOI technology are not limited to the area of speed and power, it also has advantages in term of the ability to withstand high temperature and handle high voltage. A thin layer about tens of nanometer active silicon is placed on top of a thick layer of insulator such as silicon dioxide ( $\text{SiO}_2$ ) or sometimes referred as Buried Oxide (BOX) (Sugii *et al.*, 2008; Colinge, 2008; Kilchytska *et al.*, 2011; Kranti *et al.*, 2010) and this dielectric isolation of silicon reduces the parasitic or internal junction capacitance on

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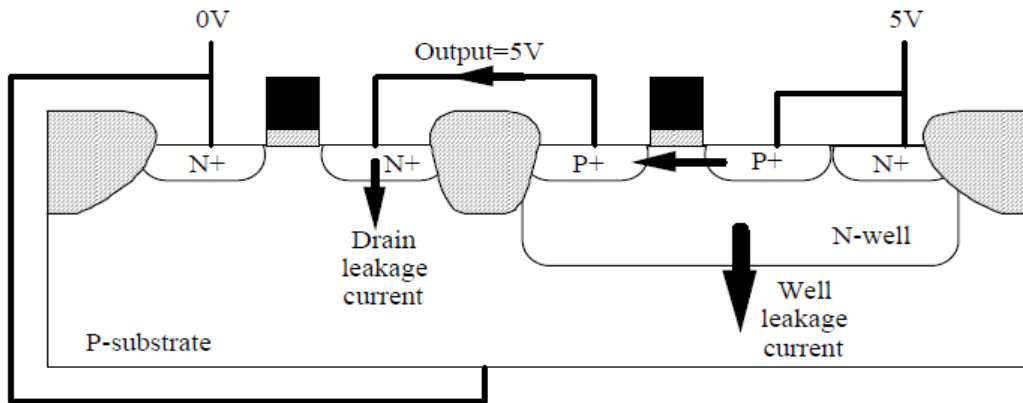


Fig. 2: Leakage current path for Bulk CMOS (b) SOI CMOS

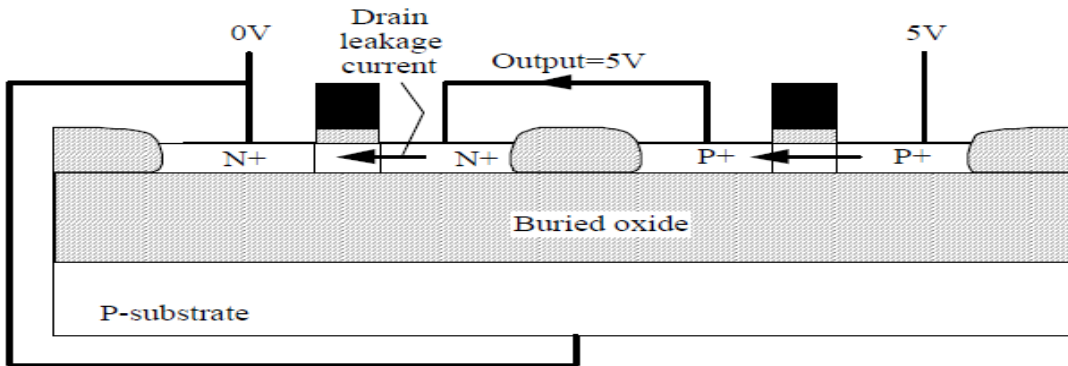


Fig. 3: Leakage current path for SOI CMOS

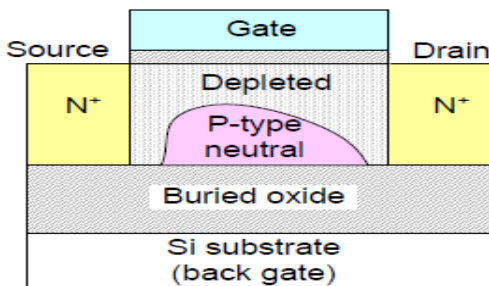


Fig. 4: Cross section of partially depleted SOI MOSFET

components and thus improves device performance by a huge percentage (Lee *et al.*, 1998; Saha, 2009; Saha, 2008).

Figure 2 and 3 shows the comparison between the Bulk CMOS and SOI CMOS in term of leakage current path and it is clear that the leakage current flows in bulk CMOS substrate whereas in SOI CMOS there is no leakage current flow in the substrate.

There are two types of SOI MOSFETs, depending on the operating mode; they are Partially Depleted SOI MOSFET (PDSOI) and Fully Depleted SOI MOSFET (FDSOI). Figure 4 shows the PDSOI configuration where an undepleted neutral region at the bottom of the SOI layer exists. The maximum depletion width is lesser than the thickness of SOI layer. It has an advantage over bulk MOSFET, that there is no leakage current and no latch-up problem (Reaz *et al.*, 2006).

Chen *et al.* (2008) proposed the design of a 65nm Partially Depleted Floating Body SOI MOSFET for off state leakage current depending on modeling of parasitic current through the floating body effect (Chen *et al.*, 2008). For low power applications or high performance technology, the supply voltage is chosen as low as feasible to minimize the power consumption and threshold voltage is also reduced as much as possible. This research shows the parasitic current through the floating body heavily influences the off state leakage current ( $I_{off}$ ) for non zero drain voltage ( $V_{ds}$ ).

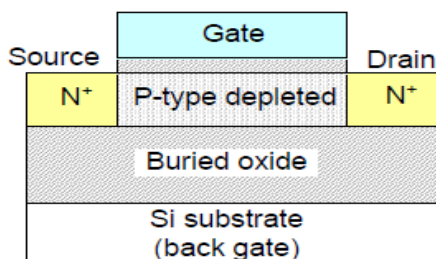


Fig. 5: Cross section of FDSOI MOSFET

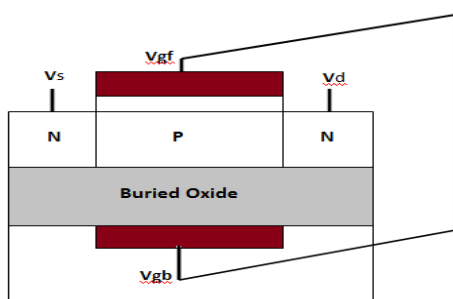


Fig. 6: Cross section of DGFD SOI MOSFET

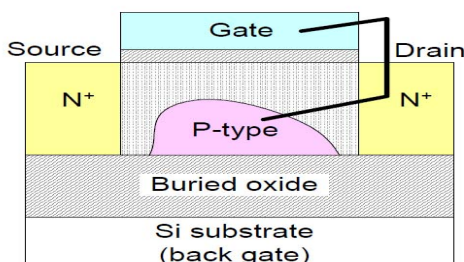


Fig. 7: Cross section of an SOI MOSFET with body and gate tied together

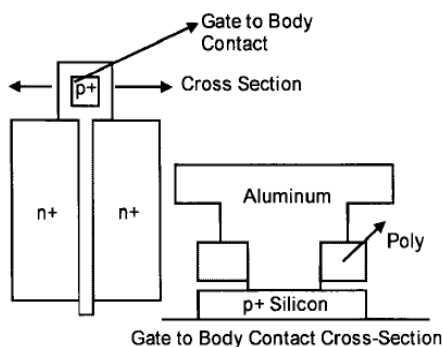


Fig. 8: Gate-to-body connection by using aluminum to short the poly gate to the P + region. This contact requires no additional processing steps

On the other hand, in case of FDSOI the entire region of SOI layer is fully depleted which offers additional advantages such as low threshold voltage, small leakage current, smaller floating body effects. Because of these characteristics, FDSOI is most appropriate device to give the better performance at low supply voltage for power consumption to be reduced. Figure 5 shows the cross section of the FDSOI MOSFET, where the maximum depletion width is greater than the thickness of the SOI layer (Warner and Grung, 1999).

Zhang and Roy (2002) introduced the Double Gate Fully Depleted SOI MOSFET (DGFD SOI) for low and high power applications (Zhang and Roy, 2002). The coupling between the front gate and back gate has been also investigated to study about the implications of the noise immunity and circuit reliability. The Fig. 6 shows the cross section of the DGFD SOI MOSFET with front gate and back gate tied together.

Wei *et al.* (1998) proposed the design and optimization of DGFD SOI MOSFET for low voltage low power circuit (Wei *et al.*, 1998). The comparison has been made between the DGFD SOI MOSFET and conventional Single Gate FD SOI MOSFET (SGFD) in term of the circuit delay, power dissipation and power delay. The results shows that the DGFD SOI MOSFET can improve the circuit performance and benefit the supply voltages scaling and the threshold voltage of DGFD SOI MOSFET can be controlled dynamically. Besides, the minimum channel length of DGFD SOI MOSFET can be reduced by 30% in comparison to that of SGFD SOI MOSFET. Thus, the DGFD SOI MOSFET is appropriate candidate for deep submicron low voltage and low power circuit.

### SOIs FOR LOW POWER APPLICATION

The design of SOI MOSFET for low power applications is proposed by Assaderaghi *et al.* (1997) where dynamic voltage threshold control is possible and is suitable for ultra low voltage (0.6V and below) operation (Assaderaghi *et al.*, 1997). It is important for the design to have a low leakage current of the transistor at the zero gate voltage. A Dynamic

Table 1: Typical electrical characteristics of 3 types of SOI MOSFETs

Items	Conventional	DTMOS	Proposed
$V_{th}$	0.675V	0.47V	0.608V
Swing	86.8 mV/dec	80 mV/dec	68 mV/dec
Mobility	260 $cm^2/V$ sec	494 $cm^2/V$ sec	368 $cm^2/V$ sec
$V_{DD}$	Free	<0.85V	<2V
$I_D$	38.2 $\mu A$	102.3 $\mu A$	66.1 $\mu A$

Table 2: Comparison of result obtained by several researchers' design

Researchers	Seng <i>et al.</i> (1998)	Tarim and Ismail (1999)	Wong and Luong (2002)	Deen <i>et al.</i> (2005)
Supply voltage	+ - 1 V	-	1.5 V	1.2 V
Output bandwidth (3 dB)	4.3 MHz	99 MHz	2.4 GHz	3 GHz
Power consumption	0.13 mW	1.5 mW	3.7 mW	1.32 mW

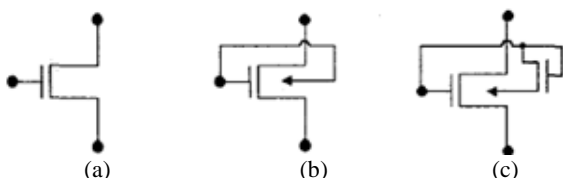


Fig. 9: A Schematic circuit diagram of 3 types of SOI MOSFET, (a) conventional, (b) DTMOS, (c) As proposed by Lee *et al.* (1998)

Threshold Voltage MOSFET (DTMOS) can be made by performing a connection tie on both the gate and the body of SOI MOSFET together. The research shown that a single MOSFET can have a higher threshold voltage when the voltage at gate to source equal to zero hence the produce a reduction in leakage current and higher speed operation. The DTMOS MOSFET configuration can be shown in Fig. 7 and 8.

Lee *et al.* (1998) also proposed a new design with an auxiliary MOSFET in which gate and drain are shorted to the main transistor's gate and thus source is connected to the channel body of the main transistor (Fig. 9) (Lee *et al.*, 1998). The result has shown a low threshold voltage, high operation voltage and high drain current as compared to conventional MOSFET and previous DTMOS designs.

Better performance achieved as it improved sub threshold voltage by 11% and increased drain current capability by 46% and decreased the leakage current and a comparison is given in Table 1.

Body effect of the Tri-Gate Bulk for DTMOS is presented by Han *et al.* (2006). In this study it is proposed that the back gate (bulk substrate) is to be utilized to offer the dynamic threshold voltage operation that exhibits high VT at VG = 0V to and low VT at VG = VDD = 0.6V to achieve low power and high performance.

The SOI MOSFET technology is also widely used in wireless and Radio Frequency (RF) applications where most of the electronic equipments can be assumed as 'power hungry' devices (Marufuzzaman *et al.*, 2010; Akter *et al.*, 2008b) because people love to perform many applications at the same time and therefore, power consumption rate is usually high. At this level, SOI technology plays a main role and yet reliable to be utilized in low power applications. The RF and mainboard circuit power consumption is to be

reduced and at the same time the performance of the devices needs to be maintained under lowest bias possibility condition. Deen *et al.* (2005) have carried out a research on RF function in low power low voltage applications and achieved a better performance compared to previous studies done by Wong and Luong (2002), Tarim and Ismail (1999) and Seng *et al.* (1998). The results are tabulated in Table 2.

Moreover thermal conductivity of the SOI MOSFET is considered as one of the crucial parameters which cannot be neglected (Hailong and Kursun, 2010). The use of Buried Oxide (BOX) with poor thermal conductivity causes the devices to experience a huge temperature rise which can be higher than 80° Celsius (Colinge, 2004). As a result, the device characteristics shift and cause malfunction condition. A tiny cutoff frequency could be sufficient for specific applications while maintaining the minimum power consumption and maximized the battery lifetime. It is shown that the improved design enhance power consumption and lifetime of the devices (Emam *et al.*, 2010; Emam *et al.*, 2008).

Therefore, Partially Depleted SOI MOSFET (PDSOI) usually used in high performance microprocessors, analog and RF systems and also memory applications. By making a connection tie on both the gate and the body together, a SOI MOSFET can have a higher threshold voltage when the voltage at gate to source equal to zero hence produce a reduction in leakage current and higher speed operation. However, PDSOI usually face a main drawback which is its physical limitation due to packaging scalability and the heat behavior also needs to be considered (Chen *et al.*, 2008).

Fully Depleted SOI MOSFET, however, built up with the ultra thin film (5 to 20nm) of Silicon. Nowadays, FDSOI technology is preferred due to its thin size, reduced leakage current and improved power consumption characteristics etc. compared to those of PDSOI and bulk silicon technology. However, the main drawback of FDSOI is its complex fabrication process (Vitale *et al.*, 2010).

## CONCLUSION

It has been shown that the appropriate candidate for low power application is Fully Depleted SOI MOSFET due to a great advantages in term of low

leakage current and power consumption is drastically reduced. Also there is no floating body effect and hence it is easier to control the short channel effects. The main challenge for FDSOI MOSFET compared to PDSOI MOSFET is the new methodology are excessively needed for defect detection in very thin layer whichever a very thin body can brought a huge challenge to manufacture and to implement the performance boosters.

## REFERENCES

- Akter, M., M.B.I. Reaz, F. Mohd-Yasin, F. Choong, 2008a. A modified-set partitioning in hierarchical trees algorithm for real-time image compression. *J. Commun. Technol. El+.*, 53(6): 642-650.
- Akter, M., M.B.I. Reaz, F.M. Yasin and F. Choong, 2008b. Hardware implementations of an image compressor for mobile communications. *J. Commun. Technol. El+.*, 53(08): 899-910.
- Assaderaghi, F., D. Sinitisky, S.A. Parke, J. Bokor, P.K. Ko and C. Hu, 1997. Dynamic Threshold-Voltage MOSFET (DTMOS) for Ultra-Low Voltage VLSI. *IEEE T. Electron Dev.*, 44(3): 414-422.
- Bondyopadhyay, P.K., 1998. Moore's Law governs the silicon revolution. *Proc. IEEE*, 86(1): 78-81.
- Chen, Q., J.S. Goo, T. Ly, K. Chandrasekaran, Z. Wu, C. Thuruthiyil and A.B. Icel, 2008. Off-state leakage current modeling in low-power high-performance Partially-Depleted (PD) Floating-Body (FB) SOI MOSFETs. *Proceeding of the 9th International Conference on Solid-State and Integrated-Circuit Technology (ICSICT- 2008)*, Beijing, China, Oct. 20-23, pp: 301-304.
- Colinge, J.P., 1987. An SOI voltage controlled bipolar MOS device. *IEEE T. Electron Dev.*, 44(4): 845-849.
- Colinge, J.P., 2004. *Silicon-on-Insulator Technology: Materials to VLSI*, 3rd Edn., Kluwer Academic Publishers, Boston.
- Colinge, J.P., 2008. A new generation of SOI MOSFET. *Romanian J. Sci. Technol.*, 11(1): 3-15.
- Deen, M.J., R. Murji, A. Fakhr, N. Jafferli and W.L. Ngan, 2005. Lowpower CMOS integrated circuits for radio-frequency applications. *IEE P-Circ. Dev. Syst.*, 152(5): 509-522.
- Emam, M., D. Vanhoenacker-Janvier, K. Anil, J. Ida and J. Raskin, 2008. High temperature RF behavior of SOI MOSFET transistors for low power low voltage applications. *Proceeding of the IEEE International SOI Conference (SOI-2008)*. New Paltz, USA, Oct. 6-9, pp: 139-140.
- Emam, M., D. Vanhoenacker-Janvier and J. Raskin, 2010. High temperature RF behavior of SOI MOSFET transistors for low power low voltage applications. *Proceeding of the IEEE International SOI Conference (SOI-2010)*. San Diego, USA, Oct. 11-14, pp: 1-2.
- Hailong, J. and V. Kursun, 2010. Dynamic forward body bias enhanced tri-mode MTCMOS. *Proceeding of the 2nd Asia Symposium on Quality Electronic Design (ASQED-2010)*. Penang, Malaysia, Aug. 3-4, pp: 33-37.
- Han, J., C.H. Lee, D. Park and Y.K. Choi, 2006. Body effects in tri-gate bulk fin FETs for DTMOS. *Proceeding of the IEEE Nanotechnology Materials and Devices Conference (NMDC-2006)*. Gyeongju, South Korea, Oct. 22-25, pp: 208-209.
- Kilchytka, V., F. Andrieu, O. Faynot and D. Flandre, 2011. High-temperature perspectives of UTB SOI MOSFETs. *Proceeding of the 12th International Conference on Ultimate Integration on Silicon (ULIS) 2011*. Cork, Ireland, March 14-16, pp: 1-4.
- Kranti, A., Rashmi, S. Burignat, J.P. Raskin and G.A. Armstrong, 2010. Analog/RF performance of sub-100 nm SOI MOSFETs with non-classical gate-source/drain underlap channel design. *Proceeding of the Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*. New Orleans, USA, Jan. 11-13, pp: 45-48.
- Lee, J.W., H.K. Kim, J.H. Oh, J.W. Yang, W.C. Lee, Kim, J.S., M.R. Oh and Y.H. Koh, 1998. A new soi mosfet for low power applications. *Proceeding of the International SOI Conference*. Stuart, USA, Oct. 5-8, pp: 65-66.
- Mack, C.A., 2003. Using learning curve theory to redefine Moore's law. *Solid. State. Technol.*, 46(7): 51-58.
- Mack, C.A., 2011. Fifty years of Moore's law. *IEEE T. Semiconduct. M.*, 24(2): 202-207.
- Marufuzzaman, M., M.B.I. Reaz, M.S. Rahman and A.M.A. Mohd, 2010. Hardware prototyping of an intelligent current dq PI controller for FOC PMSM drive. *Proceedings of the 6th International Conference on Electrical and Computer Engineering*. Dhaka, Bangladesh, Dec. 18-20, pp: 86-88.
- Mohd-Yasin, F., A.L. Tan and M.I. Reaz, 2004. The FPGA prototyping of Iris recognition for biometric identification employing neural network. *Proceedings of the International Conference on Microelectronics, ICM*, pp: 458-461.
- Moore, G.E., 1998. Cramming more components onto integrated circuits. *Proc. IEEE*, 86(1): 82-85.
- Mueller, C.W. and P.H. Robinson, 1964. Grown-film silicon transistors on sapphire. *Proc. IEEE*, 52(12): 1487-1490.

- Pellella, M.M. and J.G. Fossum, 2002. On the performance advantage of PD/SOI CMOS with floating bodies. *IEEE T. Electron Dev.*, 49(1): 96-104.
- Reaz, M.B.I., F. Choong and F. Mohd-Yasin, 2006. VHDL modeling for classification of power quality disturbance employing wavelet transform artificial neural network and fuzzy logic. *Simulation*, 82(12): 867-881.
- Reaz, M.B.I., M.I. Ibrahimy, F. Mohd-Yasin, C.S. Wei and M. Kamada, 2007. Single core hardware module to implement encryption in TECB mode. *Informacije MIDEM*, 37(3): 165-171.
- Reaz, M.B.I., M.T. Islam, M.S. Sulaiman, M.A.M. Ali, H. Sarwar and S. Rafique, 2003. FPGA realization of multipurpose FIR Filter, *Proceedings of the 4th International Conference on Parallel and Distributed Computing, Applications and Technologies (PDCAT)*, pp: 912-915.
- Saha, S., 2009. Device considerations for ultra-low power analog integrated circuits. *Proceeding of the International Conference on Computers and Devices for Communication*. Kolkata, India, Dec. 14-16, pp: 1-6.
- Saha, S.K., 2008. Scaling considerations for sub-90 nm split-gate flash memory cells. *IET Circ. Device. Syst.*, 2(1): 144-150.
- Seng, Y.K. and S.S. Rofail, 1998. Design and analysis of a 71V CMOS four-quadrant analogue multiplier. *IEE P-Circ. Dev. Syst.*, 145(3): 148-154.
- Sugii, N., R. Tsuchiya, T. Ishigaki, Y. Morita, H. Yoshimoto, K. Torii and S. Kimura, 2008. Comprehensive study on  $V_{th}$  variability in Silicon on Thin BOX (SOTB) CMOS with small random-dopant fluctuation: Finding a way to further reduce variation. *Proceeding of the IEEE International Electron Devices Meeting (IEDM 2008)*. San Francisco, USA, Dec. 15-17, pp: 1-4.
- Tarim, T.B. and M. Ismail, 1999. A low voltage CMOS square law analog multiplier. *Proceeding of the Southwest Symposium on Mixed-Signal Design, (SSMSD '99)*. Tucson, USA, Apr. 11-13, pp: 5-8.
- Tuomi, I., 2002. The lives and death of Moore's law. *First Monday*, 7(11): 1-35.
- Vitale, S.A., J. Kedzierski, P.W. Wyatt, M. Renzi and C.L. Keast, 2010. FDSOI metal gate transistors for ultra low power subthreshold operation. *Proceeding of the IEEE International SOI Conference (SOI)*. San Diego, USA, Oct. 11-14, pp: 1-2.
- Warner, R.M.J. and B.L. Grung, 1999. *MOSFET Theory and Design*. Illustrated Edn., Oxford University Press, New York.
- Wei, L., Z. Chen and K. Roy, 1998. Design and optimization of double gate SOI MOSFETs for low voltage low power circuits. *Proceeding of the IEEE International SOI Conference*. Stuart, USA, Oct. 5-8, pp: 69-70.
- Wong, J.M.C. and H.C. Luong, 2002. A 1.5-V 4-GHz dynamic-loading regenerative frequency doubler in a 0.35- $\mu$ m CMOS process. *Proceeding of the IEEE Radio Frequency Integrated Circuits Symp.* Seattle, USA, June 2-4, pp: 463-466.
- Zhang, R. and K. Roy, 2002. Low-power high-performance double-gate fully depleted SOI circuit design. *IEEE T. Electron Dev.*, 49(5): 852-862.