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Research Article

A Low Power Op Amp for 3-Bit Digital to Analog Converter in 0.18 µm CMOS Process

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Abstract: Digital to (DAC) is used to get analog voltage corresponding to input digital data in VLSI circuit design with greater integration levels. However, providing linear current and voltage outputs with the use of strictly CMOS devices presents the need for a low power operational amplifier (op-amp) circuit. In this research, the analysis of op-amp circuit for 3-bit DAC is illustrated. In order to reduce the power dissipation, weighted resistor is utilized in the proposed design. To design the op-amp circuit for 3-bit DAC, the design has been implemented in CEDEC 0.18 µm CMOS process. The simulated result shows that, under 8 V as the supply voltage the total power dissipation for the proposed DAC is 43.6 nW. Moreover, 143.17 µm is found as the total chip area of the designed op-amp circuit for 3-bit DAC.

Keywords: CMOS, DAC, op-amp, weighted resistor

INTRODUCTION

Signal processing and storage are the key component in most modern electronic systems and in the digital domain. However, to interface with the real world, conversions between analog signals and digital signals are necessary (Akter *et al*., 2008a, b; Reaz *et al*., 2007a, b; Marufuzzaman *et al*., 2010; Reaz *et al*., 2003; Reaz *et al*., 2005). The advance in complementary Metal-Oxide-Semiconductor (CMOS) technologies has dramatically improved the system performance. Moreover, the requirement of a corresponding increase in data-converter performance is important. In the design of mixed-signal ASICs, it is often very expedient to have small calibration circuits, which can be used repetitively throughout the chip. Though, it is very important to make the calibration circuits as small as possible. As a result, in the layout the internal circuitry remains virtually unchanged.

Most of the electronic devices require two converters, which are Analog to Digital Converter (ADC) and Digital to Analog Converter (DAC). However, both the converters are equally important in CMOS design. DACs are often used in digital systems to provide complete interface with analog sensors and output devices for control systems such as those used in automotive engine controls (Reaz *et al*., 2006; Reaz and Wei, 2004; Mohd-Yasin *et al*., 2004; Mogaki *et al*., 2007). In addition, designing circuits with low voltage supplies is becoming necessary into the age of portable electronic devices. The low voltage introduces some limitations like the lack of headroom present for providing output currents from the DAC.

In this study, the analysis of op-amp circuit for 3-bit DAC is presented. The design includes a weighted resistor and an op-amp circuit. The proposed design is implemented in CEDEC 0.18 µm CMOS process. The pre-simulation of DAC and post layout simulation is done with the same process under low supply voltage. Moreover, the proposed design is able to decrease the power dissipation of the overall circuit.

DAC architecture: There are several research has been done on DAC structure. Fu *et al*. (2011) worked on a 12-bit CMOS current steering DAC with a fully differential voltage output as shown in Fig. 1. The proposed DAC has adopted a segmented architecture in order to achieve a minimized die area and optimized performance. However, the design dissipates more power of 13.4 mW under 0.72~1.2 V as the supply voltages.

Zhu *et al*. (2011) also describe a DAC circuit, which utilize the optimized circuit matching technique as shown in Fig. 2. During the design process, the working frequency band varies from 10 MHz to 200 MHz with a Spurious-Free Dynamic Range (SFDR) attenuating from 61dB to 40dB. Moreover, the measurement results of the differential nonlinearity and integral nonlinearity is 0.16 LSB and 0.4 LSB, respectively. The circuit also fabricated in a 0.5 µm single poly three-metal 5 V CMOS standard process. However, the whole chip occupies about 2.822 mm^2

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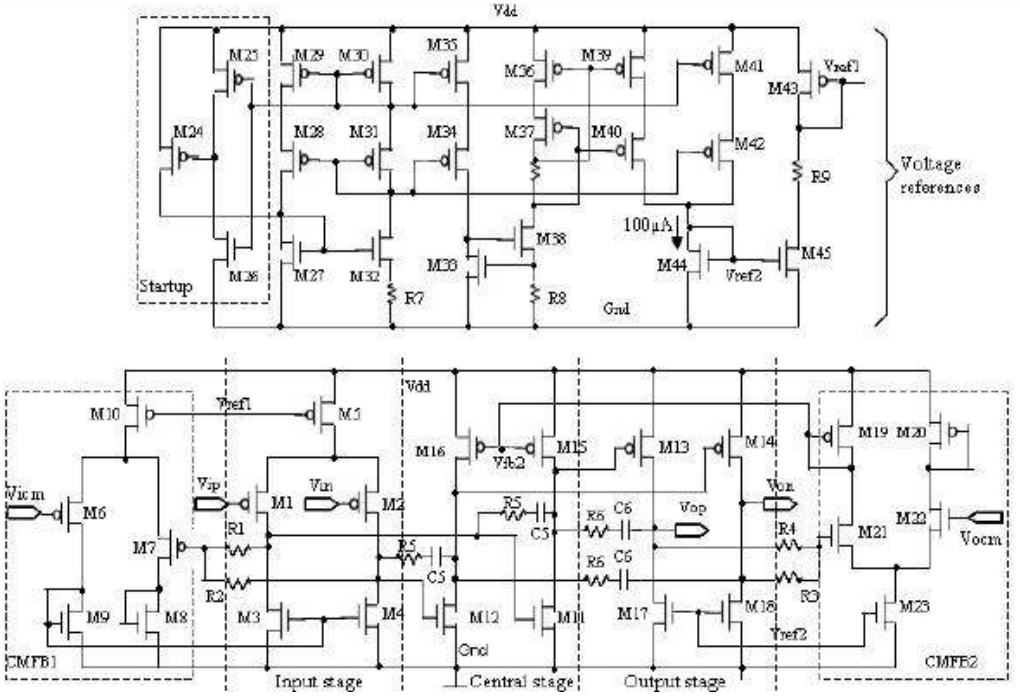

Fig. 1: Block diagram of the DAC design proposed by Fu *et al*. (2011)

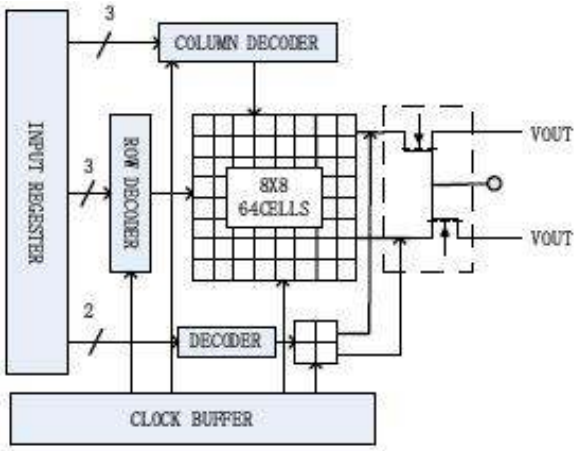

Fig. 2: Block diagram of the DAC design proposed by Zhu *et al*. (2011)

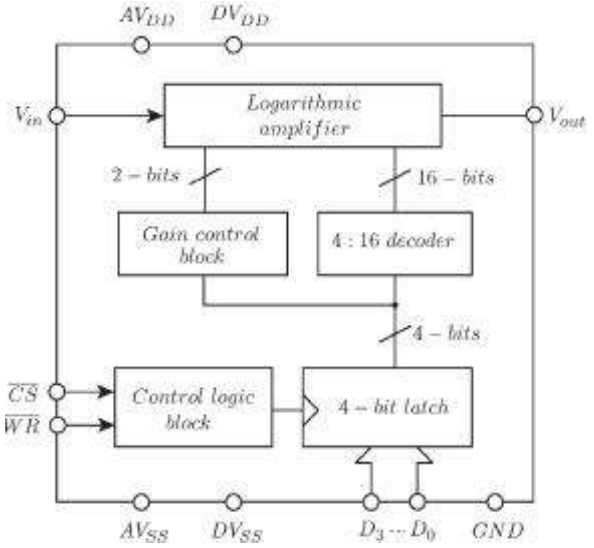

Fig. 3: Block diagram of the proposed DAC of Purighalla and Maundy (2011)

and the sampling rate is 200 MHz with the power consumption is about 113 mW.

On the other hand, Purighalla and Maundy (2011) has proposed a logarithmic DAC structure, which is shown in Fig. 3. The design presents an 84-dB dynamic range true logarithmic amplifier. Logarithmic ordering in the output is achieved as a function of control parameter X, which in turn is tuned digitally. However, the design produced power consumption as 13.2 mW with supply voltage as 1.65 V.

The DAC design as shown in Fig. 4 is proposed by Namburu *et al*. (2010), which includes CMOS drivers to switch the gates of a set of binary-weighted PMOS current sources. Temperature-insensitive operation is achieved by biasing the PMOS current sources at Zero Temperature Coefficients (ZTC) voltage. The proposed DAC has been laid out assuming a 0.5 μm silicon-on-insulator technology with approximate die dimensions of 495 μm×135 μm with operating voltage at 3 V.

Wu and Steyaert (2010) proposed a 5-bit 2GS/s current-steering D/A converter for Ultra-Wideband (UWB) transceivers. The DAC is based on a full-binary weighted architecture and achieves better than 10-bit

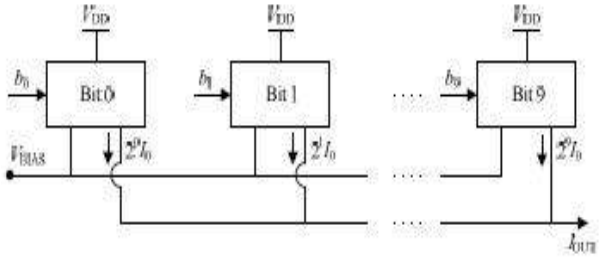

Fig. 4: Block diagram of the DAC proposed by Namburu *et al*. (2010)

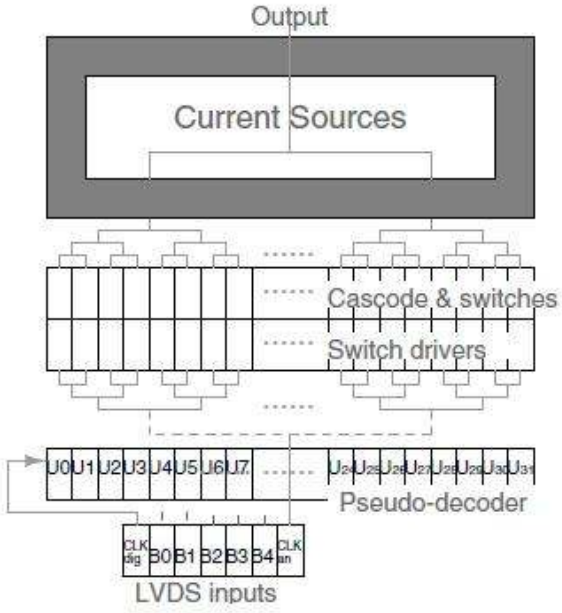

Fig. 5: Proposed block diagram of Wu and Steyaert (2010)

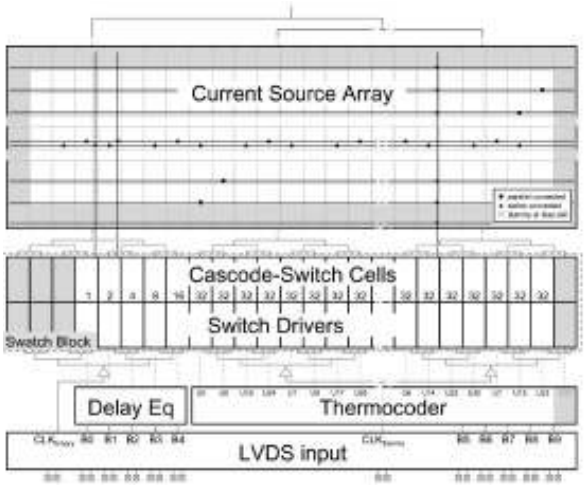

Fig. 6: Block diagram of the DAC proposed by Palmers and Steyeart (2010)

static linearity without calibration. The DAC occupies 0.5 mm × 0.75 mm in a standard 90 nm CMOS

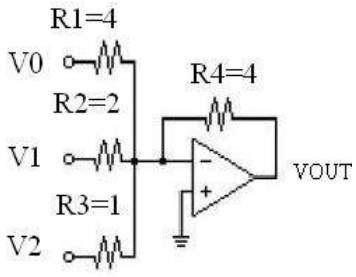

Fig. 7: Conventional circuit of summing amplifier proposed by Boylestad and Nashelsky (2002)

technology. A Spurious-Free Dynamic Range (SFDR) of more than 30 dB has been measured over the complete Nyquist interval at sampling frequencies of 2 GS/s. The power consumption at a 2 GHz clock frequency for a near-Nyquist sinusoidal output signal equals only 12 mW. The block diagram of the proposed DAC is shown in Fig. 5.

In addition, Palmers and Steyeart (2010) describes a 10-bit 5-5 segmented current steering DAC, which is implemented in a standard 130 nm CMOS technology. It achieves full-Nyquist performance up to 1 GS/s and maintains 54-dB SFDR over a 550-MHz output bandwidth up to 1.6 GS/s. The power consumption for a near-Nyquist output signal sampled at 1.6 GS/s equals 27 mW. To enable the presented performance a design strategy is proposed that introduces a switch-driver power consumption aware analysis of the switched current cell. The proposed DAC block diagram is shown in Fig. 6.

In this research, the design is employed weighted resistor and operational amplifier in order to develop as a 3-bit low power of DAC in CEDEC 0.18 µm CMOS process, which produces the lowest power consumption, compared to prior research studies.

PROPOSED METHODOLOGY

The proposed DAC design is based on conventional circuit of weighted summing amplifier as shown in Fig. 7. In this research, an op-amp is designed using the method proposed by Kumar and Kolhe (2011).

Though, the op-amp is designed for ADC design implementation, but in this research, the design method is followed to use it in DAC structure without capacitor and current with high voltage and low power consumption as shown in Fig. 8. From the schematic diagram it is shown that, M1, M2, M3 are PMOS transistors with the W/L = 1.4 µm/0.18 µm. On the other hand, M4, M5, M6, M7 and M8 are NMOS with the W/L = 0.9 µm/0.18 µm. In the schematic diagram, M4 is connected to Input Negative (INN) and M5 is

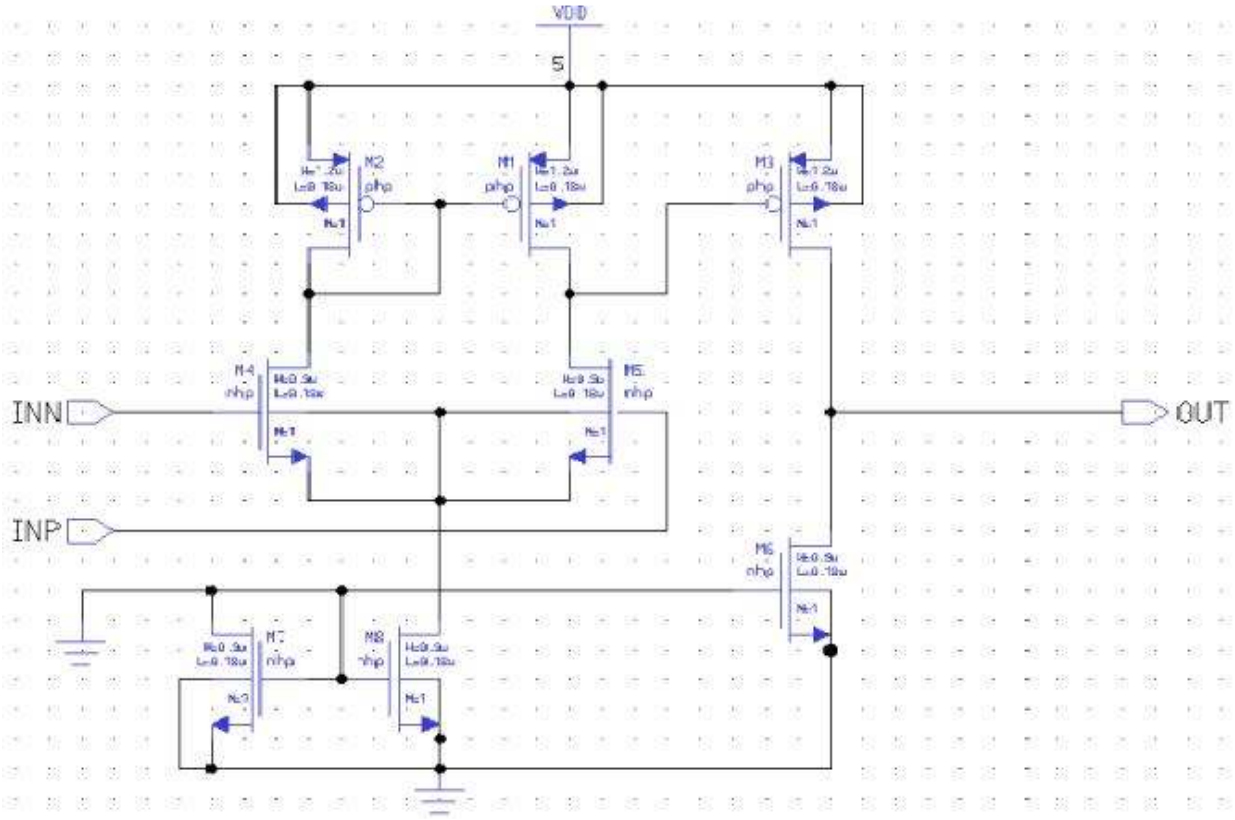

Fig. 8: Schematic diagram of the proposed op-amp for DAC

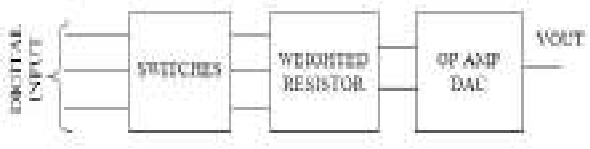

Fig. 9: Block diagram of proposed 3-bit of DAC design

connected to Input Positive (INP). Drain of M3 and M6 is connected to VOUT of the schematic.

The block diagram of the proposed 3-bit DAC circuit design is shown in Fig. 9. It is clear from the Fig. 9 that, the proposed design required switches, weighted resistor and op-amp circuit for the DAC. Digital inputs are driven throughout switches, resistor and op-amp to produce the output signal.

RESULTS AND DISCUSSION

27°C operating condition and CEDEC 0.18-µm CMOS process has been used to design the modified op-amp circuit. Simulations are executed to evaluate the circuit performance of the proposed op-amp. The design of DAC is simulated using ELDONET simulator of CEDEC 0.18 µm CMOS process. For simulation, a test-bench file is also required, which is shown in Fig. 10. A switch connects an input to a common ground. The supply voltage is 8 V for the test-bench schematic.

Table 1: Truth table of weighted resistor for DAC

V2	V1	V0	V_{OUT} (V)
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Table 2: Transistor sizing for PMOS and NMOS

P MOS (W/L)	N MO (W/L)	Delay (ns)	Power dissipation (nW)
1.4 µm/0.18 µm	1.4 µm/0.18 µm	149.75	48.93
1.4 µm/0.18 µm	0.9 µm/0.18 µm	149.75	47.83
1.2 µm/0.18 µm	0.9 µm/0.18 µm	149.75	43.60

A switch connects an input either to a common voltage V or to a common ground. The inputs are weighted in a 4:2:1 relationship, so that the sequence of values 4 V0+2 V1+V2 is formed a binary-coded decimal number, which is illustrated in Table 1. The digital inputs control the switches and the amplifier provides the analog output.

The generated waveform for 3-bit weighted sum of DAC shown in Fig. 11, which is similar as the values mentioned in Table 2. When the input = 000, then VOUT = 0V and if input = 111, then the output VOUT = 7 V.

Moreover, the layout diagram of the proposed circuit is done with the CEDEC 0.18 µm CMOS

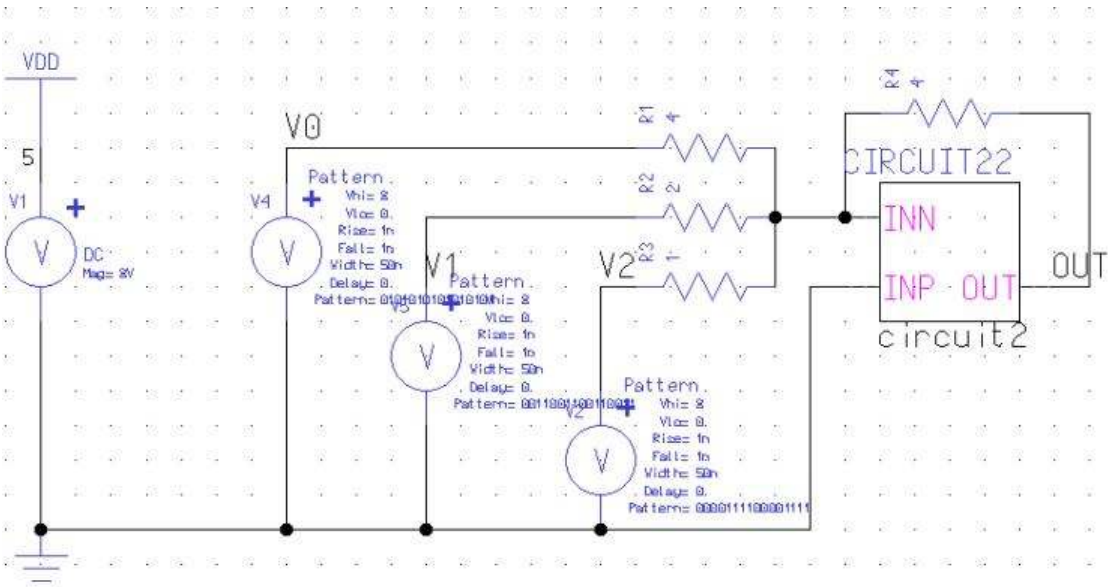

Fig. 10: Simulated schematic of 3-bit weighted sum of DAC

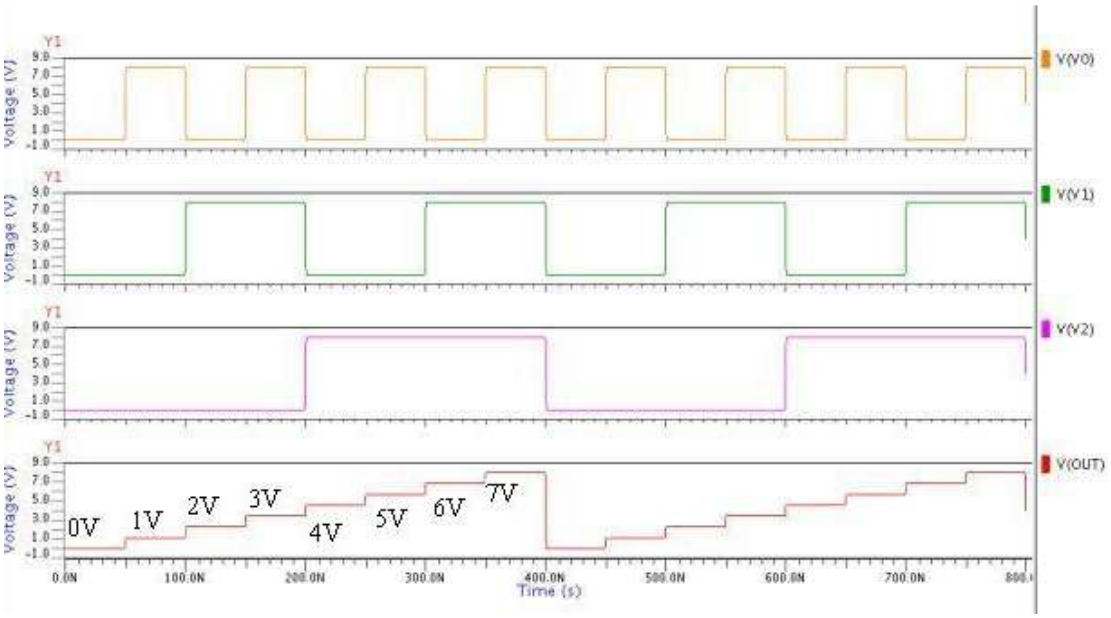

Fig. 11: Waveform of 3-bit weighted sum of DAC

Table 3: Comparison study on DAC performance among different research works

Research work	Technology	Resolution	Supply voltage	Power consumption	Active area
This work	0.18 µm	3-bit	8V	43.6 nW	143.17µm
Fu *et al*. (2011)	0.13 µm	12-bit	0.72-1.2V	13.4 mW	0.074 mm²
Zhu *et al*. (2011)	0.5 mm	8-bit	5V	117 mW	-
Purighalla and Maundy (2011)	0.18 µm	4-bit	1.65V	13.2 mW	1.5 mm²
Namburu *et al*. (2010)	0.5 µm	10-bit	3V	-	0.067mm²
Wu and Steyaert (2010)	90 nm	5-bit	-	12 mW	0.375 mm²
Palmers and Steyeart (2010)	130 nm	10-bit	1.2/1.8V	23.6 mW	0.5 mm²

process IC station tool. Figure 12 shows the layout of op amp for DAC which is successfully processed with the post layout simulation.

Besides that, the analysis of the W/L ratio for both PMOS and NMOS has done in order to get better power consumption and delay, which is generated for each range. Table 2 shows the value of delay and power dissipation for different sizes of PMOS and NMOS. From the Table 2, it is obvious that the delays are remaining same for each range of W/L for both PMOS

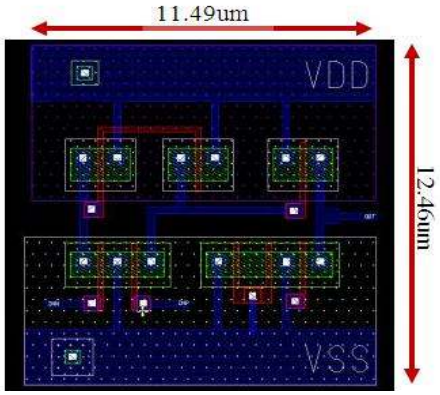

Fig. 12: Layout op amp for DAC

and NMOS. However, different values of power consumption are achieved, for the lowest size of W/L of PMOS and NMOS. Therefore, for the proposed design size of the W/L for both PMOS and NMOS are set to 1.2 µm/0.18 µm and 0.9 µm/0.18 µm, respectively. The transistors involved in the design method are listed in Table 2.

A performance evaluation study among different design methods and this study on the low voltage functionality with power consumption are listed in Table 3. Based on the comparison study, it is found that the proposed design is able to produce low power consumption only 43.6 nW than the other research studies. However, it operates at high power supply voltage, which is 8 V. In addition, the designed DAC is required only 143.17 µm as the layout area, which is also less than the previous research studies. Moreover, the designed DAC is able to perform in a better way in terms of power consumption, lower supply voltage, active layout are, etc. So it is obvious from the Table 3 that, the designed DAC can be applicable to low power applications.

CONCLUSION

An improved design and a comparative study of low power op-amp circuit for 3-bit DAC presented in this research. The modified circuit has been designed by using the CEDEC 0.18-µm CMOS process. According to the performance evaluation results, it has been proven that, the circuit is capable of consuming low power 43.60 nw under supply voltage as 8 V. Furthermore, the measured results confirm that this low power op-amp is free from the power delineation caused by the temperature change. Additionally, the circuit size reduced significantly with the active area 143.17 µm.

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