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Research Article

Fast Real-Time Digital Monitoring of Signal Waveform Quality Using an FPGA

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Abstract: The real-time or offline monitoring of signal waveform quality is important in many applications, such as electrical power quality monitoring, measurement of waveform distortion in recording systems and monitoring of electrical excitation in active measurement systems. This study presents a signal monitoring system based on a Field-Programmable Gate Array (FPGA), which receives digitized samples of analogue voltage developed across a sense resistor and performs signal processing in real time. The symmetry of the signal in both amplitude and time are calculated and used to form an overall symmetry parameter that quantifies the 'quality' of the signal, which ought to be sinusoidal. In addition, the signal frequency and amplitude are calculated. The value of the overall symmetry parameter as well as the signal amplitude are checked against predefined limits and accordingly flagged. The results show an optimum compromise among three parameters: code execution time, usage of FPGA resources and accuracy of results. The principles and implementation of the system discussed here may find application in fields where FPGA-based detailed waveform analysis is high priority.

Keywords: FPGA, monitoring, quality, symmetry, waveform

INTRODUCTION

The monitoring of signal waveform quality in both amplitude and time is important for many applications, such as electrical power quality monitoring, distortion control in audio and video recording systems and the electrical excitation of active measurement systems. The variables to be monitored, whether in real time or offline, include signal symmetry in amplitude and time, as well as signal frequency and amplitude. There is substantial literature on the monitoring of waveform symmetry by digital techniques in several areas of electrical engineering. For its practical implementation, the FPGA technology is becoming one of the techniques of choice, esp. for fast embedded applications. This study presents a fast FPGA-based signal monitoring system, which carries out the following functions in real time:

- Signal frequency and amplitude are measured
- Signal waveform quality is quantified by calculating an overall symmetry parameter that incorporates measured symmetry properties in both amplitude and time
- Rapidly ceases current supply (i.e., within about 4 μs after data acquisition), with data flagging, if any of the limits pre-set for the values of amplitude and symmetry parameter are violated

It is important that the above three features are achieved by firmware rather than hardware, thus allowing reconfiguration for many applications.

The system presented in this study has been incorporated into the fEITER (Functional Electrical Impedance Tomography of Evoked Responses) system developed at the University of Manchester UK (Davidson *et al*., 2010; McCann *et al*., 2011), in order to monitor the injected current in real time. The design of the current synthesis and drive circuitry for fEITER has been reported elsewhere (Rafiei-Naeini and McCann, 2008). The principles and implementation of the system discussed here may find application in fields where FPGA-based detailed waveform analysis is high priority.

LITERATURE REVIEW

Quantification of sinusoidal waveform 'quality': One way of quantifying 'quality' of the signal is to measure the waveform symmetry, as indicated schematically in Fig. 1. The idea of waveform symmetry in both amplitude and time has been discussed in many papers due to its importance in various fields, such as electrical power quality monitoring and waveform distortion in recording systems. Yongli *et al*. (2004) present a method to compare the waveforms of two different current signals

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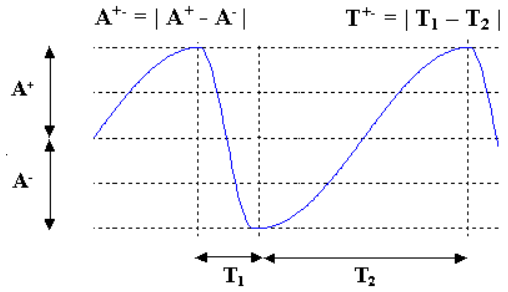


Fig. 1: Schematic of an arbitrary signal waveform, indicating basic temporal and amplitude properties and candidate symmetry parameters

to enable their identification and ultimately to protect transformers. This comparison is based on a 'waveform longitudinal symmetry coefficient', defined as the normalized difference between two areas on the waveform time-plot, which is expected to differ significantly in value between the two currents. For an ideal sine wave, the value of this parameter is zero, since the two areas are equal. A simulation of this method is presented in Yongli *et al*. (2004), but the results of its practical application have not been reported.

Comer (1968) discusses the use of waveform asymmetry, defined as the difference in magnitude between the positive and negative peaks of signal waveforms (A^{+-} in Fig. 1), to analyze various aspects of speech. Various measurements of waveform asymmetry have been suggested in the study of recording systems. Feng (1996) discusses the capability of a magneto resistive head to recover data from recorded tracks as a function of distortion in the read back signal waveform. This distortion is measured as 'peak amplitude asymmetry', which is the difference in peak amplitudes of two isolated pulses divided by the maximum of the two peak amplitudes. In a similar application, Takayama *et al*. (1992) study magnetic head readout waveform asymmetry defined as the magnitude of the difference between the durations of two half cycles, indicated as T^{+-} in Fig. 1. To study high-density digital VCR recording systems, Shimotashiro *et al*. (1995) discuss 'waveform asymmetry' which is similar to the ratio $T_2/ (T_1 + T_2)$ in Fig. 1.

In a power quality monitoring application, Liu and Heydt (2005) discuss the even harmonic components of power system voltages and currents, which cause waveform asymmetry due to the inequality of positive and negative waveform peak values. They define a power quality index Asymmetry Factor (AF) as the magnitude of the difference between positive and negative peak-magnitudes (A^{+-} in Fig. 1, divided by the rated circuit voltage (or current). They then compare AF with the power quality index based on Crest Factor, defined as the maximum of A^+ or A^-, divided by the rms voltage (with value $\sqrt{2}$ for a perfect sine wave).

Some papers have suggested more sophisticated waveform symmetry properties. Hajimiri and Lee (1998) discussing the modelling of phase noise in electrical oscillators, present an Impulse Sensitivity Function (ISF) related to the symmetry properties of the output waveform of the oscillator. For example, the average value of ISF represents the degree of difference between the rise and fall times of the waveform. Post *et al*. (1998) suggest the use of this ISF to understand the effect of waveform symmetry on phase noise present in oscillators.

Digital implementation of quality monitoring: In the power quality monitoring field, fast digital monitoring of signal waveforms has been explored. For example, Naidoo and Pillay (2007) present a technique of rapid detection of variations in rms voltage over limited time durations. This technique is implemented in a DSP chip (TMS320F240) and detects the decrease in rms voltage (i.e., sag) within 4 ms, which is fast in the context of a power system frequency of 60 Hz. Similarly, Yang and Wen (2006) present a device for power quality monitoring. In this device, a DSP chip (TMS320F2812) is used for data processing and power quality analysis. There are other instances of real-time digital monitoring of signal waveforms using microprocessors and/or DSP, e.g., (Zou *et al*., 2009; Xian-Min and Hong-Ting, 2010; Yi *et al*., 2010).

In recent years, there has been an increase in the use of FPGA technology for measurement or monitoring of signal quality. For example, Lara-Cardoso and Romero-Troncoso (2008) present a real-time standalone power quality monitoring system, implemented in a low-cost FPGA. Gallo *et al*. (2010) perform real-time FPGA-based frequency response compensation of current transformers. Other recent examples of the use of FPGA in real-time power quality monitoring are Cardenas *et al*. (2010), Ruiz-Llata *et al*. (2011) and Liang and Da (2011).

METHODOLOGY

The system input is 50 digitized samples of the voltage developed across a Sense Resistor (R_S) through which the current flows, as shown in Fig. 2. The 16-bit unipolar ADC samples at 500 kS/s. (More details of the set-up are given in the next section) The FPGA-based signal processing system calculates the current's amplitude, frequency and a 'symmetry parameter' (S), which quantifies the 'quality' of the waveform. S is based on the symmetry of both the temporal and amplitude aspects of the waveform. If the resulting values of amplitude and/or S violate pre-defined limits, the system generates a binary signal (denoted 'cutoff' in the discussion below) to shut off the current supply, along with two further binary signals to report the reason for cut-off.

The FPGA code applies a series of processing steps to the digitized data of the raw voltage signal, as shown in Fig. 3. First of all, peak detection is performed, in

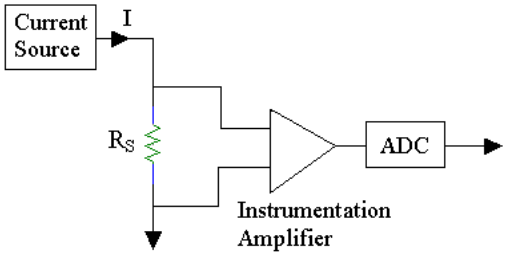


Fig. 2: Schematic diagram of the set-up, which gives input samples to the signal monitoring system in real time

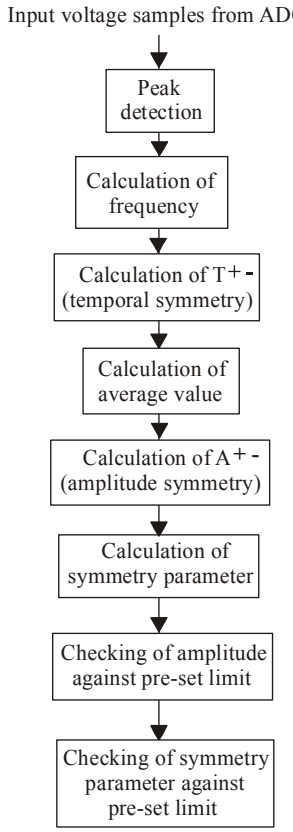


Fig. 3: Flow diagram of the signal processing taking place in the real-time signal monitoring system

order to determine the maxima and minima of the signal. The signal frequency f is calculated by counting positive and negative peaks and recording their time location within the 50 samples. Then, the durations of two half-cycles are calculated, viz. between successive positive and negative peaks, T_1 and between successive negative and positive peaks, T_2 (Fig. 1). Their difference, T^{+-}, characterizes the temporal symmetry of the waveform and is zero for an ideal sine wave. It is found empirically that T^{+-} can frequently be zero. Therefore $T' = (1 + T^{+-})$ is used in the calculation of S below. The average value of the entire input signal is calculated, to set a baseline. The positive and negative amplitudes A^+ and A^- (Fig. 1) of the measured voltage waveform are determined with respect to the average. The magnitude of the difference between these two amplitudes (A^{+-}) characterizes the amplitude symmetry of the waveform; for an ideal sine wave, A^{+-} is zero. It is found empirically that A^{+-} is never equal to zero. The value of the symmetry parameter $S = A^{+-} * T'$ is computed, to quantify the 'quality' of the waveform, in units of V-sec. S is zero for an ideal sine wave and its range depends on many practical parameters of the overall system, such as ADC sampling rate, current amplitude and the amplifier gain in the current sensing circuit. The limits of S are therefore set empirically.

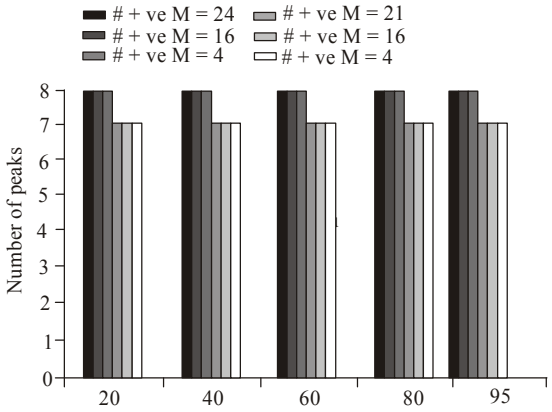
Finally, checks against pre-set limits are performed. First the measured signal amplitude is compared with the frequency-dependent pre-set limit, taking account of the necessary calibration parameters (R_s, amplifier gain, etc.) to carry out the comparison in the current domain; in this process, the frequency value used is that calculated from the measured data as described above. The value of S is checked to be within a pre-specified range to ensure that a sinusoidal current of acceptable quality is being applied. When either of the above limits is violated, current cut-off is flagged, along with the recorded data element 'Cex' (Current in excess) in the case of amplitude violation or 'Bad-sine' for symmetry violation.

SYSTEM DEVELOPMENT AND IMPLEMENTATION

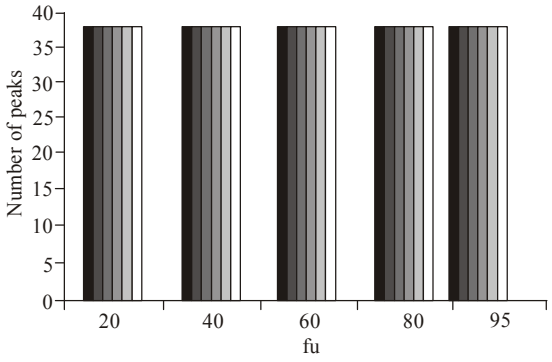
Offline version: Initially, an offline version of the system was developed, which took 256 samples as input. This version also incorporated moving average filtering of the measured signal (with sample size M), prior to the steps of peak detection and frequency calculation. All other signal processing calculations, shown in Fig. 3, were directly performed on the measured raw waveform. Filtering is required if the input signal has poor Signal-to-Noise Ratio (SNR), in order to avoid counting noise peaks as signal peaks, thus resulting in wrong frequency calculations.

The signal processing code was developed first in MATLAB and evaluated using MATLAB-generated sinusoids of different frequencies, f. These signals were corrupted with various levels of Gaussian noise, quantization noise and/or unwanted contamination frequency (fu). The Gaussian noise signal had zero mean and highest amplitude in the range 5-10% of the amplitude of the principal sinusoidal signal. The amplitude of the fu signal was in the range of 10-20% of the amplitude of the principal sinusoidal signal. These high levels of corruption of the simulated signal were used in order to test the signal monitoring system under extreme conditions.

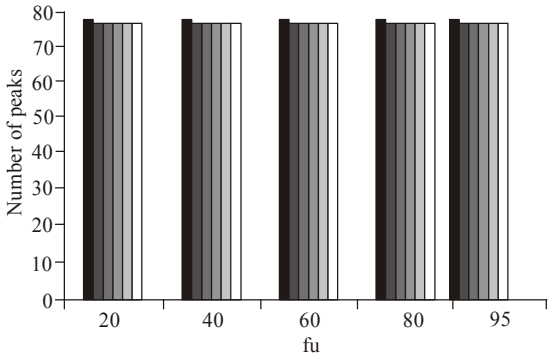
The different values of M were considered at length. In the first instance, M was considered analytically in the frequency domain, in terms of the frequency spectrum of the input signal and the frequency response of the moving-average filter



(a) f = 10 kHz



(b) f = 50 kHz



(c) f = 100 kHz

Fig. 4: Numbers of positive and negative peaks detected, as a function of fu, for signals with three different values of principal sinusoidal frequency, f. Results are given for three different M values

(Proakis and Manolakis, 1996). This showed that coverage over a wide frequency range of input signal (1 kHz-100 kHz here) would require more than one value of M. The final selections of M values (24, 16 and 4) were based on an empirical approach, as described immediately below.

Figure 4 shows examples of simulation results for simulated signals at three frequencies, each having been contaminated with Gaussian noise and unwanted contamination frequencies at various values of fu; the Gaussian noise had its highest amplitude set at 5% of that of the principal sinusoidal signal and the amplitude of the contamination signal was set at 10% of that of the principal sinusoidal signal. The figure is in the form of bar charts of the number of positive and negative peaks detected, for each different M value.

Table 1: Results from the offline version of signal monitoring system, for real experimental signals; S threshold for 'Badsine' flag is pre-set at 15 nV-sec

	f (Hz)	S (nV-sec)	Flags		
			Bad-sine	Cex	Cut-off
f = 10 kHz					
FPGA-board	9870	28	1	0	1
ISE simulator	9870	28	1	0	1
f = 50 kHz					
FPGA-board	50008	6	0	0	0
ISE simulator	50008	6	0	0	0
f = 100 kHz					
FPGA-board	100674	28	1	0	1
ISE simulator	100674	28	1	0	1

These examples show that the peak count is almost independent of fu and M; only small variations occur in peak count, due to the contamination. The peak count values are almost exactly as expected. Data were generated for many combinations of different contamination frequencies and noise levels. Upon analysis of those results, it was decided that three different M values were necessary to give adequate performance over the principal sinusoidal frequency range, 1 to 100 kHz and that the values M = 24, 16, 4 gave optimal performance.

In the experiment set-up shown in Fig. 2, the current generation sub-system used was that already developed for testing various options before building the complete fEITER system. This current source gives approximately 80 dB SNR in the generated current and has excellent output impedance performance (Rafiei-Naeini and McCann, 2008), thus ensuring negligible influence by the Sense Resistor (R_S). For practical experiments on the current monitoring system, the current was passed through a 10 kΩ Sense Resistor (R_S), giving 1 V rms, which was digitised using an AD7686 ADC sampling at 500 kS/s. The empirical criteria developed in the simulation process were used to judge the signal quality, giving the results in Table 1. No easy access was available to a controllable current source of poor SNR for experiments.

Synthesizable VHDL code for the offline version was written, its bit file generated and downloaded onto the Xilinx Virtex-4 SX Evaluation Kit for further testing. The same VHDL code was run on the Xilinx ISE Simulator for comparison of its results with those from the Evaluation board. Table 1 shows this comparison for the same three principal signal frequencies as used for the MATLAB tests in Fig. 4, for real signals obtained through the above experiment set-up. The Xilinx ISE simulator was used with clock frequency set to 50 MHz, as used on the real FPGA

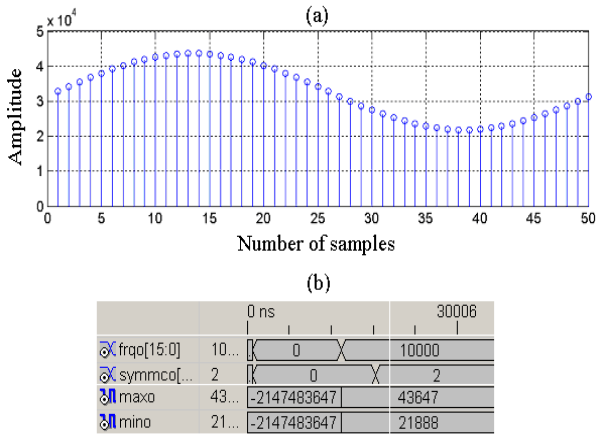


Fig. 5: (a) MATLAB-generated symmetric input for the signal monitoring system (b) result of the Xilinx ISE simulator, showing the values of f (frqo) in Hz, S (symmco) in nV-sec, maxima (maxo) and minima (mino)

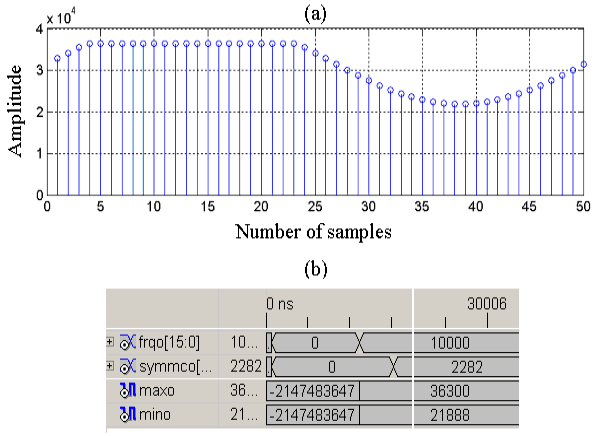


Fig. 6: (a) MATLAB-generated positive-clipped asymmetric input for the signal monitoring system (b) result of the Xilinx ISE simulator, showing the values of f (frqo) in Hz, S (symmco) in nV-sec, maxima (maxo) and minima (mino)

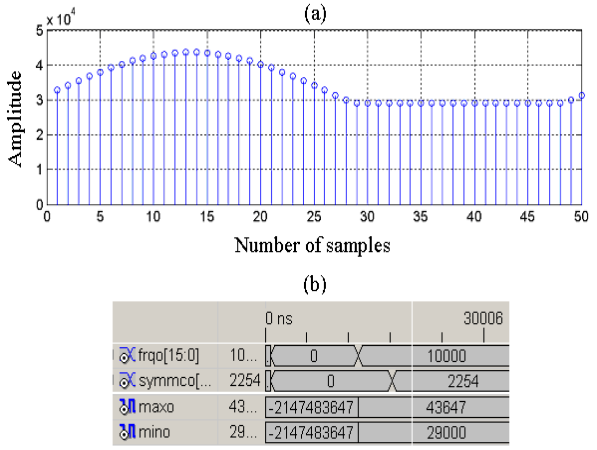


Fig. 7: (a) MATLAB-generated negative-clipped asymmetric input for the signal monitoring system (b) result of the Xilinx ISE simulator, showing the values of f (frqo) in Hz, S (symmco) in nV-sec, maxima (maxo) and minima (mino)

board in the test system and in the fEITER system. The whole code of the offline version takes about 45 µs to complete processing.

Real-time system: Having established the functioning of the required signal processing, the following modifications were made in the offline version of the signal monitoring system to produce its real-time version. The main purpose of these modifications was to minimise the FPGA resources required, since the fEITER system was to be implemented on the same FPGA. The modifications implemented were:

- Number of input samples was reduced from 256 to 50
- Moving-average filtering was removed, as it was found not to be required for a high-SNR input signal. Thus the real-time signal monitoring system implemented the signal processing steps exactly as shown in Fig. 3

The input signal of the real-time signal monitoring system was simulated in MATLAB and 50 of its samples (Fig. 5a) were first processed with the MATLAB-version of the code. The resulting calculated value of frequency was 10000 Hz; it is discussed in the next section on experimental results. The value of the Symmetry parameter (S) was calculated by the MATLAB-code to be 0, as it should be for an ideal sine wave. These 50 samples were used as the input to test the VHDL-version of the signal monitoring code in the Xilinx ISE simulator. Fig. 5b shows the result of the Xilinx ISE simulator, with the calculated value of the frequency as 10000 Hz. In this case, S is calculated to be 2 nV-secs; the deviation from zero is due to factor that FPGA-based signal processing here implemented fixed-point integer-based calculations, resulting in rounding off of results. After data acquisition, the whole code of the real-time version takes about 4 µs to complete processing.

The above testing was performed for the normal symmetric sinusoidal signal. Two asymmetric sinusoidal signals were also tested in simulation (and later in the actual system as well, whose results are presented in the next section). These asymmetric signals were half-wave clipped sine-waves of 10 kHz frequency, as shown in Fig. 6a and 7a. Again, 50 samples of each waveform were used as the input to the VHDL code in the Xilinx ISE simulator. Figure 6b and 7(b) show the results of the simulator for the positive-clipped and negative-clipped sine waves respectively. The calculated value of the frequency in both cases is 10000. The values of S for the positive-clipped and

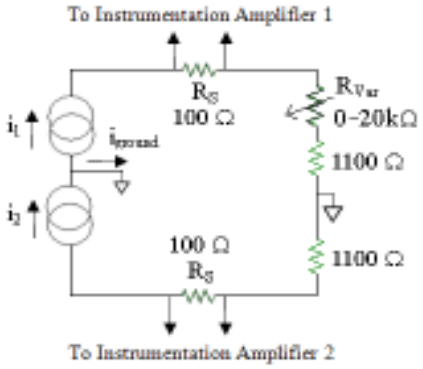


Fig. 8: Test set up to generate the asymmetric input signal for the real-time signal monitoring system

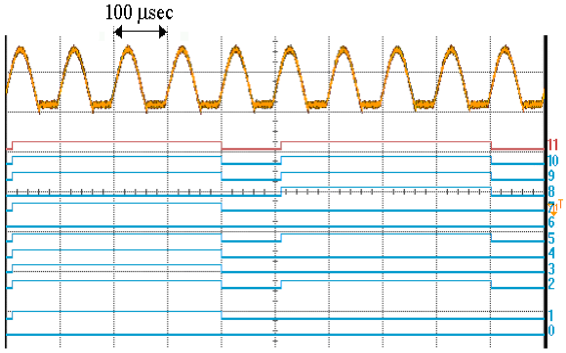


Fig. 9: Mixed signal oscilloscope's screen capture showing the asymmetric signal (analog waveform) and its S value (debug port signals) calculated by the signal monitoring system for two different cycles of the input signal

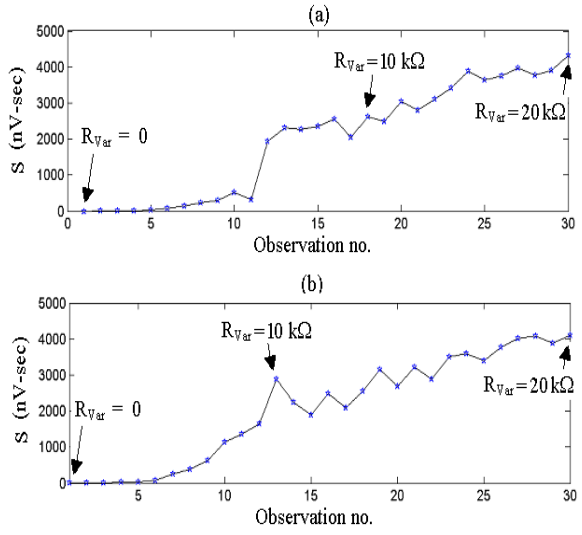


Fig. 10: Plots of S for the various asymmetric signals, generated from the two current sources

negative-clipped sine waves are 2282 nV-sec and 2254 nV-sec, respectively. These values are large, as expected, compared to the result of 2 nV-secs for the symmetric sine-wave. The values of maxima and minima determined by the VHDL code exactly matched with those of the MATLAB-generated signals, in all of the above three examples.

EXPERIMENTAL RESULTS OF REAL-TIME SYSTEM

The real-time signal monitoring system was incorporated into the fEITER system, running at f = 10 kHz with current amplitude 1 mA peak-to-peak. The current is passed through a 100 Ω Sense Resistor (RS), giving approx. Thirty five mV rms, which is first amplified by an instrumentation amplifier with a gain of 10 and then digitized using an AD 7686 ADC sampling at 500 kS/s. Thus 50 samples going into the signal monitoring system comprise one full cycle of the 10 kHz sinusoidal signal. The current source in the fEITER system is dual, i.e., it is a balanced pair of single-ended current sources producing a pair of mirror-imaged current signals. Hence two current monitoring systems have been instantiated in FPGA to monitor the sense resistor signals coming from both of the instrumentation amplifiers through subsequent ADCs.

Accuracy of results:

Symmetry parameter (S): The value of S was tested with two types of current given as input to the signal monitoring system. The first was the normal symmetric sinusoidal signal (similar to that shown in Fig. 5a delivered by the current generation sub-system of fEITER. When observed over 100 different measurements, the calculated value of S was 2 nV-secs for 26 measurements and 0 for the rest. This reflects the fact that a sequence of measurements are being made on real currents, which are subject to noise variation. This result matches with that given in previous section. Thus the current sinusoid is almost an ideal sine wave as far as its overall symmetry is concerned. An asymmetric signal, i.e., a half-wave clipped waveform, was given to the signal monitoring system. This asymmetric signal was produced at the output of the instrumentation amplifier, using the set-up shown in Fig. 8.

The variable resistor R_{var} was initially set to 0 Ω; as R_{var} was changed to higher values, the gross mismatch between the loads of the two current sources as well as the very high load resistance in the path of the current i_1 resulted in a half-wave clipped signal at the output of instrumentation amplifier 1. An example of this asymmetric signal is shown in Fig. 9 (analogue waveform). In the same figure, the digital signals of the debug port are the 12-bits of the calculated symmetry parameter S. The two values of S shown, calculated for two different sets of 50 input samples each, are 3774 nV-sec (hex EBE) and 3876 nV-sec (hex F24).

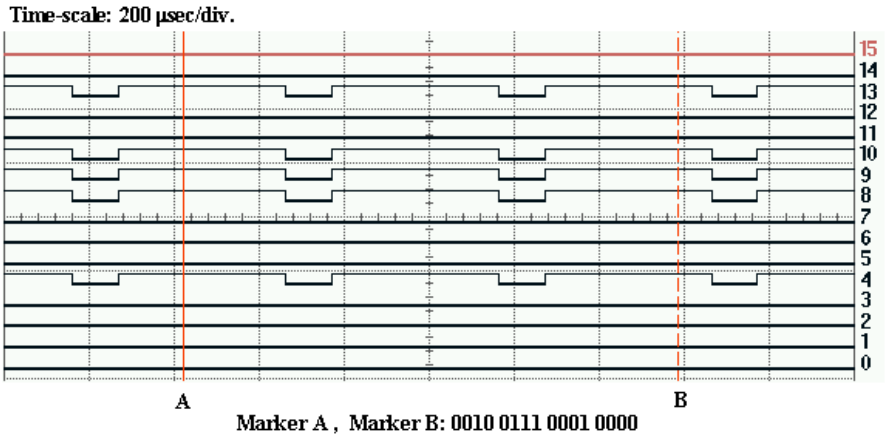


Fig. 11: Mixed signal oscilloscope screen capture showing 16 bits of frequency value, calculated every 500 µsec for each newly acquired set of 50 samples from ADC, in the real-time version. The frequency value shown is hexadecimal 2710 corresponding exactly to the input sinusoidal frequency of 10 kHz

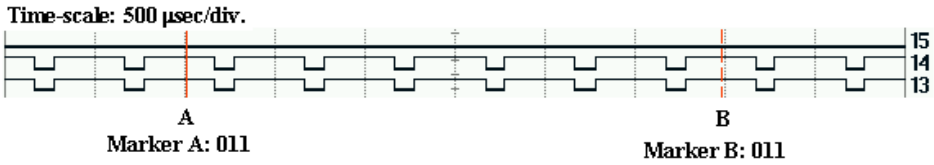


Fig. 12: Mixed signal oscilloscope screen capture showing the three binary flags, bad-sine (bit 15), Cex (bit 14) and cut-off (bit 13), evaluated every 500 µsec for the newly acquired set of 50 samples from ADC, in the real-time version. In this example, the current amplitude is higher than the safety threshold, and hence Cex is set to '1'

Figure 10 shows the plots of calculated S obtained during the period when the variable resistance R_{var} was changing: Fig. 10a is for the set-up shown in Fig. 8; Fig. 10b shows the equivalent results when R_{var} was introduced into the path of current i_2 and the digitized samples are taken from the output signal from instrumentation amplifier 2. Both of these plots show generally an increase in the value of S, as R_{var} is increased from 0 to 20 kΩ causing an increase in the degree of clipping, i.e., asymmetry.

The operation of the current cut-off due to asymmetry being in excess of the S threshold was tested by setting the S threshold limit in the VHDL code to various values, e.g., 15 nV-sec (Table 1), 100 nV-sec etc.

Frequency: The frequency value calculated (Fig. 5, 6, 7 and 11) is exactly identical (within 1 Hz) to that of the principal input sinusoid, viz. 10000 Hz. The improvement in frequency measurement compared with that in the offline version (Table 1) comes about for a specific reason: An integral number of cycles of input signal are captured (1 in this case) and the calculation does not include division by a measured time interval, which, if included, would require the approximation of the divisor to be a power of 2.

Signal amplitude violation and cut-off: The activation of signal cut-off caused by the current amplitude exceeding the pre-set limit was tested by reducing the allowed value in firmware to a threshold lower than the limit (Fig. 12). In this particular case, the current flowing through the sense-resistor was 343 µA rms, whereas the threshold was set at approx. 100 µA rms for the purpose of testing the VHDL code. This caused 'Cex' and 'cut-off' to be set to '1' and consequently the current injection was stopped.

Resource utilization in FPGA: After the acquisition of 50 samples in 100 µs, the execution time of the real-time signal monitoring code is about 4 µs (for a clock frequency of 50 MHz). About 14% of the Virtex4 SX35 FPGA resources are used. For the offline version, the execution time was 45 µs with a silicon space usage of 21%. This increased usage of resources in the offline version was predominantly due to the moving-window average calculations.

CONCLUSION

This study has presented a fast FPGA-based real-time signal monitoring system with potential for use in many fields, such as electrical power quality monitoring, measurement of waveform distortion in recording systems and monitoring of electrical excitation in active measurement systems. This system

does not assume that the input waveform is a pure sinusoid, nor does it assume that there is no dc component. It quantifies the 'quality' of the sinusoidal waveform, using a symmetry parameter that combines both temporal and amplitude symmetry. Moreover, it calculates the frequency and amplitude of the measured waveform, rather than using any user-set parameters. It then applies checks on the values of symmetry parameter as well as amplitude against pre-set limits and generates flags accordingly.

An optimum compromise has been identified concerning three parameters:

- FPGA code execution time
- usage of Virtex4 FPGA space
- Accuracy of results

The system parameters have been chosen to give full-code execution time of about 4 μs; this is of the order of one-twenty-fifth of the acquisition time of all the waveform samples. The accuracy of the calculated signal parameters is excellent, as discussed in last two sections. About 14% of the FPGA resources are used which leaves sufficient FPGA resources unused and available.

ACKNOWLEDGMENT

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ABBREVIATIONS USED

ADC : Analogue to Digital Converter
AF : Asymmetry Factor
DSP : Digital Signal Processor
fEITER : Functional Electrical Impedance Tomography of Evoked Responses
FPGA : Field Programmable Gate Array
ISE : Integrated Software Environment
SNR : Signal-to-Noise Ratio
VHDL : VHSIC Hardware Description Language

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