

Research Article

Design and Implementation of Digital Signal Transmission Performance Analyzer Based on FPGA

¹Guoping Zhang and ²Mande Xie

¹Department of Information Science and Technology, Zhejiang Sci-Tech University,

²Department of Computer and Information Engineering, Zhejiang Gongshang University, Hangzhou, Zhejiang, 310018, China

Abstract: Digital signal transmission analyzer is mainly used for testing the transmission quality of digital communications signal and it usually composed of digital signal generator, pseudo-random signal generator, low-pass filter and digital signal analysis circuit. This study adopts FPGA to implement the digital signal generator and pseudo-random signal generator, as well as to implement the shift register to generate the required M sequence. By changing the low-pass filter cutoff frequency and the amplitude of the pseudo-random signal to analog transmission environment and signal analysis portion consists of the digital signal analysis circuit. The digital signal analysis module extracts the sync signal and produces synchronization scan signal by using the synchronous clock, as the outside trigger signal of oscilloscope to display the eye diagram of the digital signal stably. To analyze the degree of interference and the strength of inter-symbol interference by observing the eye diagram, thus this study implements the performance test for digital signal transmission.

Keywords: DSP builder, eye diagram, FPGA, low-pass filter, M sequence

INTRODUCTION

With the rapid development of communication and computer technology, digital signal transmission has been more widely used. Digital signal transmission analyzer is the most important and basic test equipment in digital communication, mainly used for testing digital communication signal transmission quality, whose main test parameters include errors, alarms, jitter and drift and so on, which is widely used in digital communication equipment development, production, maintenance and measurement of test and can also be used in the construction of the digital communication network, acceptance of opening and maintenance testing. General digital transmission analyzer is more complicated and expensive, modularization and integration has become the major trends of the product. This study presents a simple FPGA-based digital transmission performance analyzer, simply visually learning the impact of inter symbol interference and noise by an oscilloscope eye diagram, in order to achieve the goal of testing the digital signal transmission performance.

LITERATURE REVIEW

In academia, about the digital signal transmission analyzers, there are a lot of papers (Yuan and Feng,

2011; Zhao, 2011; Liu *et al.*, 2011; Hong *et al.*, 2011) published in recent years. They are mainly complemented through a relatively simple circuit, but overall, all the implementations are only focused on someone aspect. In business community, the domestic manufacturers of digital transmission analyzer mainly include: the 41st Institute of China Electronics Technology Group Corporation, Beijing COMTEST CO., LTD, Beijing Zhong Chuang Telecom Test Co., Ltd and other companies. Domestic digital transmission analyzers are mainly the PCM analyzer and the low speed of SDH/PDH digital transmission analyzer. The 41st Institute's products are typical representatives of the domestic digital transmission analyzer, having all types except OTN tester, the highest rate of 2.5 Gbps. At present, only a few manufacturers are developing higher speed digital transmission analyzer, most of which trend to miniaturization. High-end digital transmission analyzer is dominated by large foreign companies, including companies such as JDSU, EXFO, Anritsu, Acterna etc., the latest generation of OTN tester rate reached 43 Gbps.

OVERALL DESIGN OF THE DIGITAL TRANSMISSION PERFORMANCE ANALYZER

The block diagram of simple digital signal transmission performance analyzer is shown in Fig. 1.

Corresponding Author: Mande Xie, Department of Computer and Information Engineering, Zhejiang Gongshang University, Hangzhou, Zhejiang, 310018, China, Tel.:86057128008286

This work is licensed under a Creative Commons Attribution 4.0 International License (URL: <http://creativecommons.org/licenses/by/4.0/>).

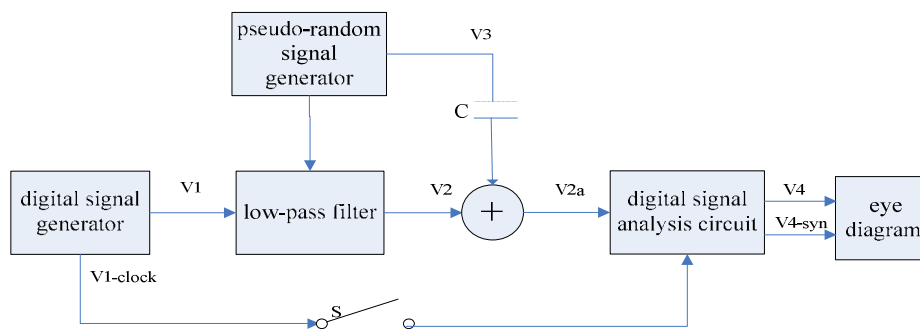


Fig. 1: The block diagram of simple digital signal transmission performance analyzer

In the Fig. 1 V1 and V1-clock are the digital signal produced by the digital signal generator and corresponding clock signal. V2 is the output signal after the filter. V3 is a pseudo-random signal generated by the pseudo-random signal generator. V2a is the Mixed-signal of V2 and V3 after the capacitor C, as input of the digital signal analysis circuit; V4 and V4-syn are output of the digital signal analysis circuit and the extracted sync signal.

In this study, FPGA is used to build a shift register to generate sequence M and pseudo-random signal, allowing the system to have fast and flexible features in this way. After through filter, the digital signal generator amplify the signal with the separate adjustable gain circuit, making the system gain adjustment flexible and fast. In order to simulate a real work environment, the system has joined the man-made noise and therefore also designs a voltage comparator circuit to reduce noise interference. Signal analysis circuit amplifies the superimposed input signal amplification and extracts the sync signal, to generate the eye diagram, thus for intuitively understanding impact of the inter-symbol interference and noise, implementing test to the digital signal analysis circuit.

THE HARDWARE DESIGN OF DIGITAL SIGNAL TRANSMISSION PERFORMANCE ANALYZER

The hardware design of digital signal transmission performance analyzer includes: low-pass filter, the adder circuit, scaling circuit, voltage comparator circuit, the DAC circuit module. Low-pass filter is the most important and critical component and therefore, we will elaborate on its concrete realization.

Design specifications of low-pass filter: The low-pass filter of digital signal transmission performance analyzer should meet the following indicators:

- Low-pass filter band attenuation at least 40 db/decade

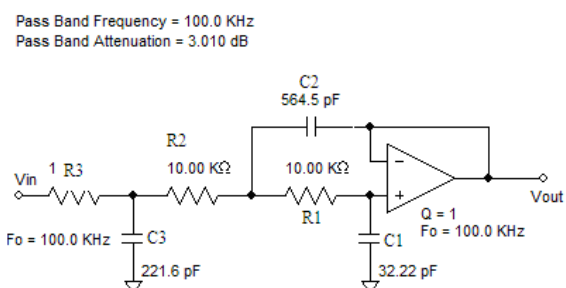


Fig. 2: The schematic of active low-pass filter

- Three low-pass filters, their cutoff frequency are 100, 200, 500 kHz, respectively the absolute value of the cutoff frequency error is not greater than 10%
- Filter pass band gain A is adjustable in the range of 0.2 to 4.0

Hardware design of the low-pass filter: In general, the transition zone of first-order circuit is wide, but the maximum attenuation slope of amplitude-frequency characteristics is only -20 db/decade. If the filter with the attenuation to be less than 40 db/decade, theoretically using second-order low-pass filter can meet the requirements, but actually 3-order low-pass filter has to be used in order to meet the requirements. For the three low-pass filter design, the basic idea is first using Filter Solution to determine the theoretical parameter values of the corresponding cut-off frequency low-pass filter under the ideal amplitude-frequency characteristics. But the actual device is unable to meet the requirements of the theory parameter values, according to the actual conditions and the component configuration for that purpose and constantly adjust the device and its parameter values, to approximate the ideal amplitude-frequency characteristic curve infinitely. For the situation of $F_0 = 100$ kHz, the theoretical parameter values for each device can be determined by Filter Solution, as shown in Fig. 2 and the corresponding ideal amplitude-

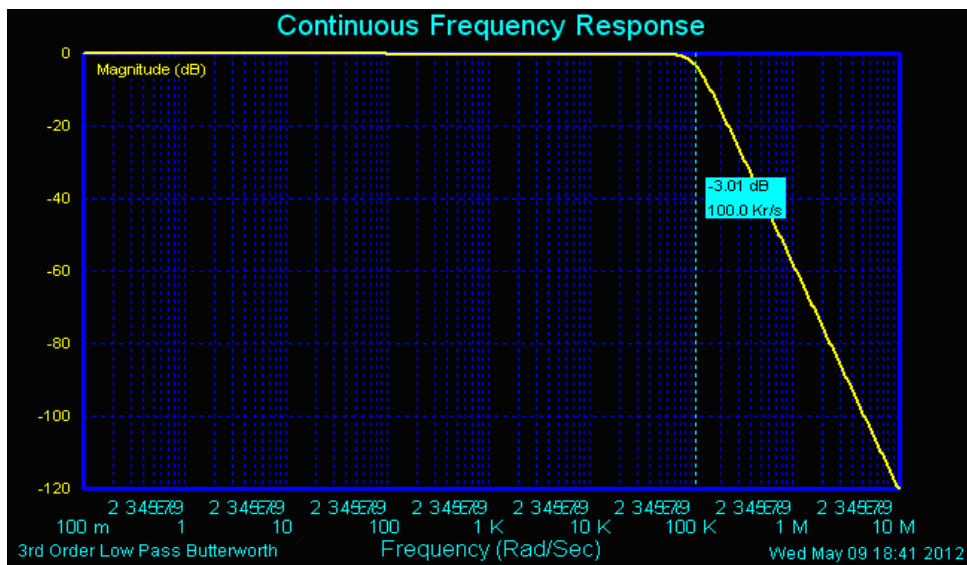


Fig. 3: The amplitude-frequency characteristics of active low-pass filter

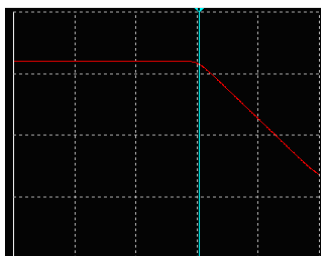


Fig. 4: The amplitude-frequency characteristics when $F_0 = 100$ kHz

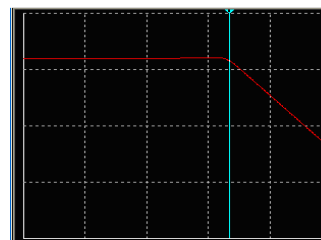


Fig. 5: The amplitude-frequency characteristics when $F_0 = 200$ kHz

frequency. Characteristics curve are shown in Fig. 3. When $F_0 = 100$ kHz, the attenuation is -3 db, which means 100 kHz is the filter cut-off frequency.

Depending on actual conditions and configuration of components, through repeated experiments, the actual parameter values determined when $F_0 = 100$ kHz are: R1, R2, R3 all $10k\Omega$, C1, C2 and C3, respectively: 30, 560 = and 200 pF. According to simulation by Multisim, the amplitude-frequency characteristics are shown in Fig. 4. As shown, when 108 kHz the attenuation is -3.2 db, which means that cutoff frequency, is near 100 kHz, meeting the design goals of what the error does not exceed 10%.

Based on the same method, when $F_0 = 200$ kHz the actual parameter values can be determined as follows: R1, R2, R3 respectively: $10k\Omega$, $10k\Omega$ and $8.2k\Omega$, C1, C2 and C3, respectively: 15, 300 and 120 pF. According to simulation by Multisim, the amplitude-frequency characteristics are shown in Fig. 5. As shown, when the frequency is 220 kHz, the attenuation

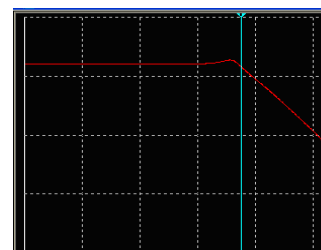


Fig. 6: The amplitude-frequency characteristics when $F_0 = 500$ kHz

is -2.8 db, which means cutoff frequency is near 200 kHz, meeting the design goals of what the error does not exceed 10%.

Based on the same method, when $F_0 = 500$ kHz, the actual parameter values can be determined as follows: R1, R2, R3 respectively: $10k\Omega$, $10k\Omega$ and $2.4k\Omega$. C1, C2 and C3, respectively: 10, 120 and 47 pF. According to simulation by Multisim, the amplitude-frequency characteristics are shown in Fig. 6.

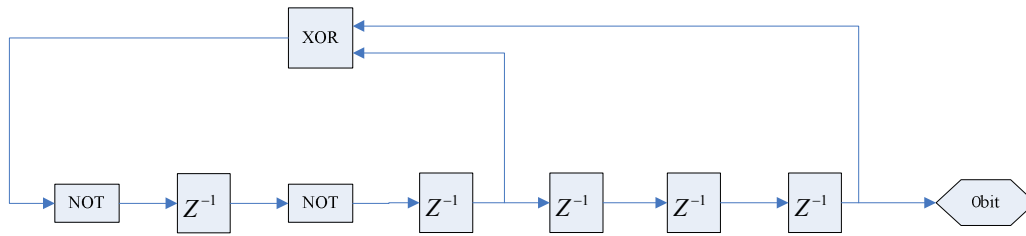


Fig. 7: The model of M sequence generator

As shown, when 220 kHz the attenuation is -2.5 db, which means cutoff frequency, is near 500 kHz, meeting the design goals of what the error does not exceed 10%.

In addition, the target that the pass band gain A can be adjusted in the range of 0.2 to 4.0 can be realized mainly by adjusting the sliding rheostat.

THE FPGA CIRCUIT DESIGN OF DIGITAL SIGNAL TRANSMISSION PERFORMANCE ANALYZER

The FPGA design mainly includes the design of digital signal generator, pseudo-random signal generator and synchronized signal extraction circuit.

Design of digital signal generator: The digital signal in the digital signal transmission performance analyzer is mainly sequence M. This study adopts the sequence M model in $F1(x) = 1 + x^2 + x^3 + x^4 + x^8$, as shown in Fig. 7. It uses the tool which is called DSP Builder to design.

By using the DSP Builder, the realization diagram in FPGA is shown in Fig. 8. The output sequence M data rate can be changed by changing the Clock in its input end. As shown in Fig. 9, Clock 14 is the clock and the Output 15 which we called M sequence can be produced.

Design of the pseudo-random signal generator: The pseudo-random signal also requires the sequence M and the data rate is 10 Mbps, absolute value of an error can not more than 1%. However, the general microcontroller hardly achieves 10 Mbps and the timer cannot reach the 1% precision. The FPGA has absolute advantage in high speed digital signal processing and it can call the DSP builder to combine MATLAB and Simulink to give a full play of the MATLAB. Thus we can put this theory into practice. Meanwhile, the FPGA has many IP nuclear, like FFT, FIR and IIR, thus can reduce the design difficulty of users and shorten the development cycle. The FPGA model of M sequence for the Pseudo-random signal is shown in Fig. 10. The

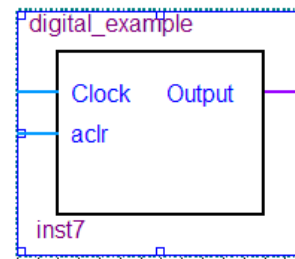


Fig. 8: The realization diagram of digital signal generator in FPGA

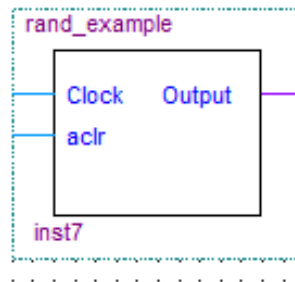


Fig. 9: The realization diagram of pseudo-random signal generator in FPGA

clock16 is the clock and it can produce the pseudo random signal shown in Fig. 11.

Manchester code generator circuit: Manchester coding is a self-synchronizing coding method, that is to say, the clock sync signal is hidden in the data waveform. In the Manchester coding, in the middle of every digit has a jumping, that is the clock signal and can also be called as data signal. "1" refers to the jumping from high to low and "0" refers to the jumping from low to high. There is another differential Manchester encoding, in which the jump in the middle of each digit just provides the setting of clock time. "0" refers to the jumping at the beginning of the digit; otherwise, it will be referred as "1". This module can transform the sequence M to Manchester code. The Manchester code generation circuit model in FPGA is

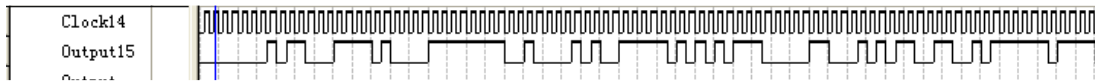


Fig. 10: The simulation wave of digital signal generator in FPGA

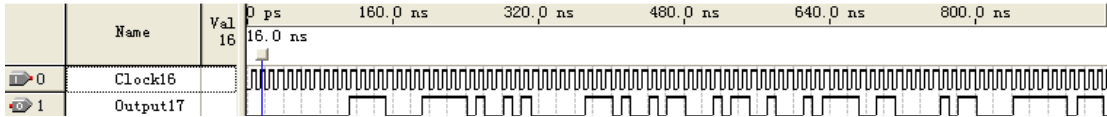


Fig. 11: The simulation wave of pseudo-random signal generator in FPGA

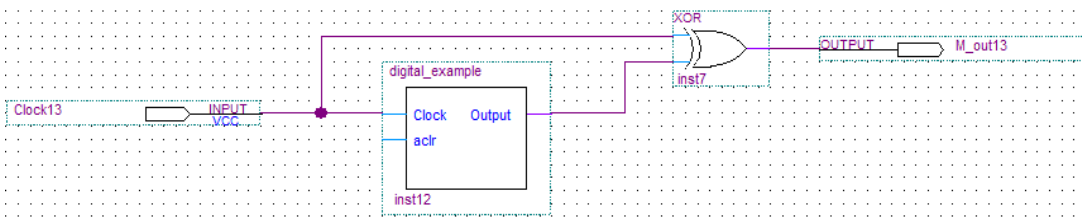


Fig. 12: The realization diagram of Manchester code generator in FPGA

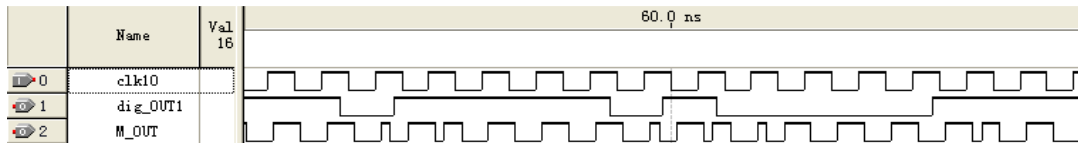


Fig. 13: The simulation wave of manchester code generator in FPGA

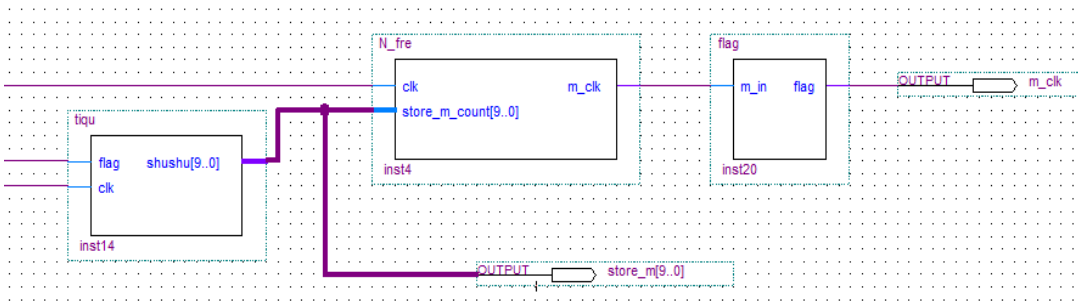


Fig. 14: The realization diagram of synchronized signal extraction in FPGA

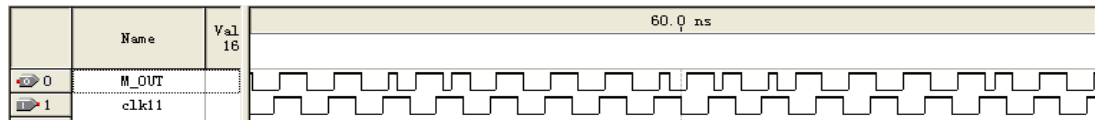


Fig. 15: The simulation wave of synchronized signal extraction in FPGA

shown in Fig. 12. As shown in Fig. 13, the Manchester M-out is produced based on the xor of clk and M sequence.

Synchronized signal extraction circuit: This module adopts the FPGA internal counting method to realize

the synchronized signal extraction. Put the Manchester code through this module, the synchronous clock signal can be obtained. The synchronized signal extraction model in FPGA is shown in Fig. 14. As shown in Fig. 15, the clock signal clk can be extracted from M_out.

Table 1: The real value and output voltage of digital signal under different data rate

Data rate /db/dec	Measure of data rate		Output voltage/V
	Actual data rate/ $V_{1-clock}$	Data rate error (%)	
10	9.950	0.5	3.3
20	19.98	0.1	3.3
30	29.90	0.3	3.3
40	39.92	0.2	3.3
50	49.80	0.4	3.3
60	59.60	0.6	3.3
70	69.60	0.5	3.3
80	80.20	0.2	3.3
90	90.50	0.5	3.3
100	100.70	0.7	3.3

SYSTEM TESTING AND PERFORMANCE EVALUATION

Testing results of sequence M digital signal: The digital signal V1 is the M sequence of $F1(x) = 1 + x^2 + x^3 + x^4 + x^8$, its clock signal is V1-clock; the data rate is 10~100 kbps. The tunable stepping can be 10 kbps, the absolute value of an error of the data rate is not more than 1% and the output signal is TTL electrical level. The testing results are shown in Table 1.

Performance testing of low-pass filter:

Test method: Input a sine signal to the low-pass as test signal, adjust the input signal and observe the method of producing the corresponding output Signal, thus the various performance indicators of the filter can be got. The parameters under the laboratory condition are shown in Table 2, 3 and 4, the input signal is 1 V.

From the table, it can be seen that the cut-off frequency is accurate basically; the attenuation is far more than 40 db/dec. It indicates that the filter has superior performance. Especially, the low-pass filters which $F_0 = 100$ kHz can reach 60 db/dec or so.

Test of eye frequency: By using the eye diagram, put the clock signal $V_{1-clock}$ and the digital signal $V_{2-clock}$ produced by the digital signal generator into the oscilloscope, the waveform produced is shown in Fig. 16. The open size of the "eyes" in eye diagram reflects the crosstalk intensity between codes. The "Eyes" that are bigger and more regular indicate that the crosstalk intensity is smaller, vice versa. When there is noise, the noise will impose on the signal, the observed diagram will be blurred. If it exists between codes, the "eyes" will open smaller. Compared with the original diagram, the clear thin line mark becomes fuzzy ribbon line and regular. The greater the

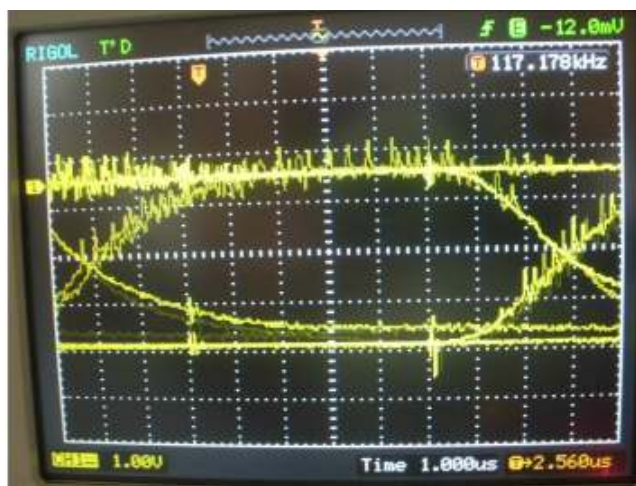


Fig. 16: Eye diagram

Table 2: The experiment results of the low-pass filter when $F_0 = 100$ KHz

$f/V_{2-clock}$	20 k	50 k	80 k	90 k	100 k	110 k	120 k	150 k	200 k
Voltage/v	1.04	1.06	0.92	0.81	0.70	0.60	0.48	0.32	0.20

Table 3: The experiment results of the low-pass filter when $F_0 = 200$ KHz

$f/db/dec$	20 k	50 k	100 k	150 k	200 k	250 k	300 k	400 k	500 k
Voltage/v	1.02	1.06	1.04	0.96	0.71	0.48	0.33	0.22	0.17

Table 4: The experiment results of the low-pass filter when $F_0 = 500$ KHz

f/V_1	20 k	100 k	200 k	400 k	450 k	500 k	550 k	600 k	800 k
Voltage/v	1.00	1.02	0.85	0.80	0.73	0.70	0.67	0.63	0.52

noise, the wider and fuzzier the line mark will be. The bigger the crosstalk, the less regular the eye diagram will be. Figure 16 shows that the eye diagram is regular, thus the crosstalk will be relatively small. At the same time, it can be seen that the noise imposes on the signal and make the eye diagram blurred. The noise tolerance $db/dec = 3.06/3.4 = 0.9$. V_1 is the peak voltage, V_2 is the maximum voltage signal.

CONCLUSION

The study designs three modules: digital signal generator, low-pass filter and digital signal circuit. Based on the digital signal generator implementation scheme of this study, the simulation of each function modules is done by using the MATLAB software. Then, it combines the principle diagram and the VHDL to finish the FPGA digital signal generator. Meanwhile, the Filter solution software is used to design the low-pass filter and focus on the problems, such as, the irregular waveform, bigger ripple, cut-off frequency and less than 40 db/dec and so on. As for digital signal circuit, this study filters the Manchester waveform and reshapes the waveform by using the voltage comparator. As for the synchronization problem, the

waveform is produced in the moment of clock jumping, so as to realize the phase synchronization.

ACKNOWLEDGMENT

This study was partially supported by Grant No. SB1105001-E from the Construction Project of Experimental Teaching Demonstration Center of Zhejiang Province.

REFERENCES

- Hong, H.Y., Z.J. Li and L.Y. Li, 2011. Design of a simple digital signal transmission performance analyzer. *J. Changzhou Institute Technol.*, 24(6): 23-26.
- Liu, S.J., W.M. Ran, X.J. Wang and D.Z. Tan, 2011. Design of transmission property analyzer for digital signals. *J. Hubei Univ. Nationalities Natural Sci. Edn.*, 29(4): 382-385.
- Yuan, L.C. and J. Feng, 2011. Design and construction of the simple digital signal transmission performance analyzer. *J. Huanggang Normal Univ.*, 31(6): 72-74.
- Zhao, L.J., 2011. Implement of simple signal transmission performance analyzer. *Comput. Knowl. Technol.*, 7(31): 7747-7748.