Research Journal of Applied Sciences, Engineering and Technology 6(12): 2277-2282, 2013
DOI:10.19026/rjaset.6.3859
ISSN: 2040-7459; e-ISSN: 2040-7467

Submitted: December 17, 2012 Accepted: January 19, 2013 Published: July 30, 2013

Research Article

A Comparative Study of SPWM on A 5-Level H-NPC Inverter

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Abstract: This study presents a comparative study of Sinusoidal Pulse Width Modulation (SPWM) techniques in a five level H-bridge/Neutral Point Clamped (H-NPC) inverter. Past research on H-NPC inverter used In-Phase Disposition (IPD) to realize the output voltage of the inverter. This study shows that other SPWM techniques could also be used. Simulation results of Alternative Phase Opposition Disposition (APOD), Phase Disposition (PD) and the modified In-Phase Disposition (IPD) are compared based on their harmonic contents.

Keywords: H-bridge/Neutral Point Clamped (H-NPC), Sinusoidal Pulse Width Modulation (SPWM), Total Harmonics Distortion (THD)

INTRODUCTION

The advancement in semiconductor devices like Insulated Gate Bipolar Transistors (IGBTs), Integrated Gate-Commutated Thyristors (IGCTs) allow the development of high-power converters and medium voltage drives due to their superior switching characteristics, low-power losses and simple gate control (Rodriguez *et al*., 2007). Even with their superiority, a single semiconductor switch could not be connected directly to a medium voltage grid. This is where multilevel inverter comes to play (Rodriguez *et al*., 2002). Multilevel inverters have the advantages of producing good power quality, low switching losses, reduced output (rate of change of voltage) dv/dt and high voltage capability. Both amplitude and pulse width modulation are used in controlling the switches (Urmila and Subbarayudu, 2010). The main topologies of multilevel inverters are the Neutral Point Clamped (NPC) inverter, Flying Capacitor (FC) inverter and Cascaded H-Bridge (CHB) inverter. Several switching techniques have been developed to switch different topologies. Multilevel Sinusoidal Pulse Width Modulation (SPWM) has been extended to Level-Shifted PWM (LS-PWM) and Phase-Shifted PWM (PS-PWM). The Alternative Phase Opposition Disposition (APOD), Phase Opposition Disposition (POD) and Phase Disposition (PD) fall into the LS-PWM that have carrier disposition variants, are used in producing the gate signals of NPC inverters through relating each carrier with the gate. The PS-PWM is used in CHB and FC inverters where pair of carriers is related to each cell of the inverter and phase shifting the carriers of the different cell introduces a synchronism, which generates the stepped waveform (Kouro *et al*., 2010). This study compares the harmonic distortion produced by some of the SPWM techniques on five-level H-NPC inverter proposed by Wu *et al*. (1999).

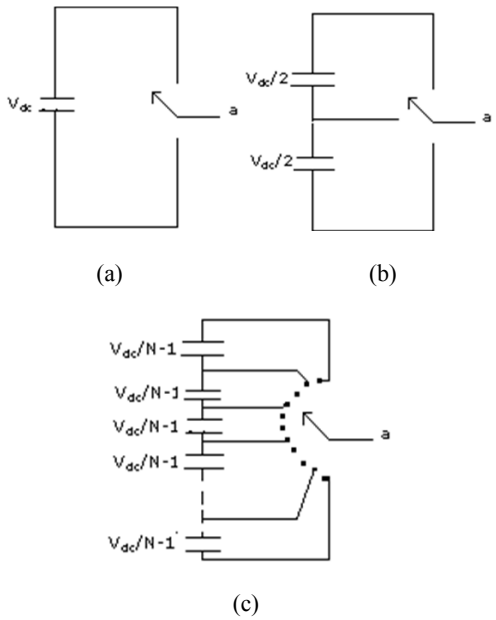

Fig. 1: Multilevel inverter topologies, (a) two-level, (b) three-level and (c) N-level

Multilevel inverter: The two-level inverter produces output voltage of either 0 or $\pm V_{dc}$ operating at high switching frequency along with PWM technique enables it to produce a voltage or current output waveform that has appreciable harmonic contents. Semiconductor device rating constraints and switching losses make two-level inverter less acceptable in high power and high voltage applications. The topologies of

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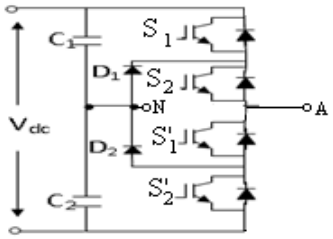

Fig. 2: Three-level NPC phase leg topology

multilevel inverter as shown in Fig. 1 make it easy to attain higher voltage and power without much stress on the switching devices (Rashid, 2004).

Neutral Point Clamped (NPC) inverter: The diode clamped inverter also called Neutral Point Clamped (NPC) inverter as shown in Fig. 2 has its DC-bus voltage split into three levels by two capacitors C_1 and C_2. The midpoint of the capacitors is referred to as the neutral point. The three level output voltage stages are $V_{dc}/2$, 0 and $-V_{dc}/2$. The clamping diodes D_1 and D_2 are the key components that differentiate the NPC inverter from the two-level inverter. The diodes clamp the switch voltage to half the level of the DC bus voltage. The NPC inverter allows fast dynamic response and higher output frequency at upper power range (Rodriguez *et al*., 2007; Colak *et al*., 2011; Rodriguez *et al*., 2002).

Multilevel inverter SPWM techniques: Carrier strategies similar to those employed for conventional two-level three-phase inverter's SPWM can be readily extended to the three phase multilevel case. Various type of single-edged (i.e., saw-tooth) waveform could be used, thus double-edge triangular carrier have superiority in cancellation of harmonic contents (Holmes and Lipo, 2003).

Double-edge modulation can be achieved by increasing the number of triangular carrier to L-1 where L is the number of voltage levels comprising the DC-link (Carrara *et al*., 1992). These carriers are arranged so that they fully occupy contiguous bands in the range of - (L - 1) $V_{dc}/2$ to (L - 1) $V_{dc}/2$ for L odd. A single sinusoidal reference is then compared with these carriers to determine the switched voltage to be obtained. These alternative PWM strategies with differing phase relationship have been developed in Carrara *et al*. (1992).

Alternative Phase Opposition Disposition (APOD), where carriers in adjacent band are phase shifted by 180° are shown in Fig. 3.

Phase Opposition Disposition (POD), where carriers above the reference zero point are out of phase with those below zero by 180° are depicted in Fig. 4.

Phase Disposition (PD), where all carriers are in phase across all bands is shown in Fig. 5.

A modified in phase disposition by Wu (2006) has two modulating waves Vm_1 and Vm_2 with the same

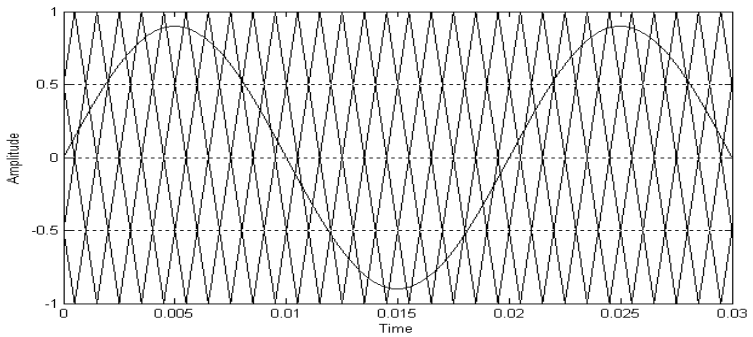

Fig. 3: Alternative Phase Opposition Disposition (APOD)

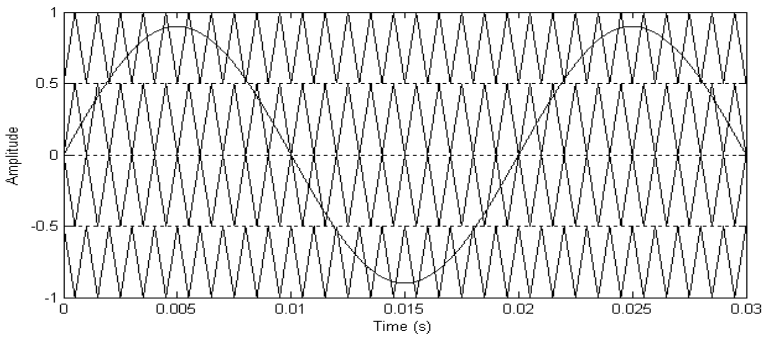

Fig. 4: Phase Opposition Disposition (POD)

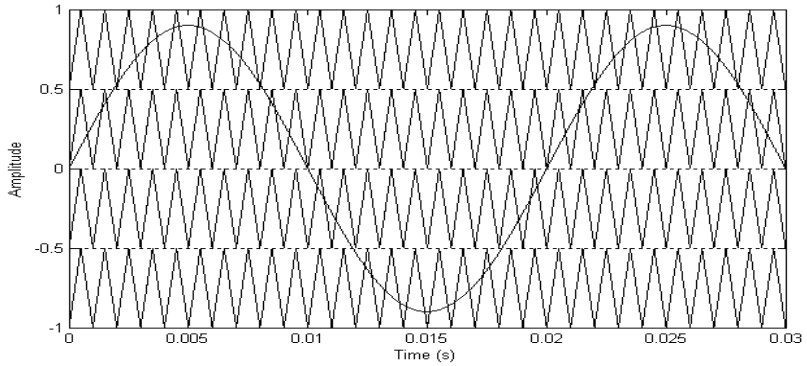

Fig. 5: Phase Disposition (PD)

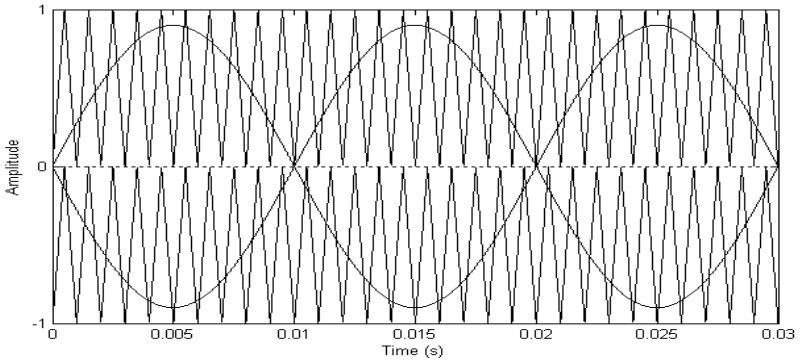

Fig. 6: In-Phase Disposition (IPD)

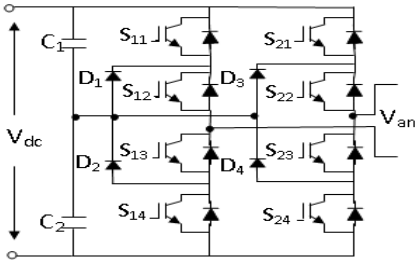

Fig. 7: Five-level H-NPC inverter phase leg topology

frequency and amplitude but are 180° out of phase. The triangular carriers Vcr_1 and Vcr_2 are in phase but vertically disposed as shown in Fig. 6.

Analysis of five-level H-NPC inverter: Five-level H-NPC inverter is composed of H-bridge connection of two classic three-level NPC phase to form the inverter phase leg as shown in Fig. 7. The inverter phase voltage contains five voltage levels instead of three levels for the NPC inverter leading to lower dv/dt and THD. It requires an isolated DC source for each H-bridge to avoid short-circuit of the DC link (Wu, 2006; Kouro *et al*., 2010). The H-bridge of each phase of the inverter has each switch constituting of four complimentary switch pairs (S_{11}, S_{13}), (S_{12}, S_{14}), (S_{21}, S_{23}) and (S_{22}, S_{24}). Therefore, the modulation scheme needs to generate only four independent gate signals for the top and bottom four switches.

Table 1: Simulation parameters

Parameter	Value
DC voltage V_d	100 V
Reference freq. f	50 Hz
Carrier freq. f_c	1000 Hz
Modulation index m	0.9

This study uses Total Harmonic Distortion (THD) as the modeling characteristics to compare the SPWM methods used on the five-level H-NPC.

SIMULATION RESULTS AND DISCUSSION

MATLAB/Simulink was used to implement the different SPWM techniques simulation of the inverter. Table 1 provides the parameters used for all the simulations.

Figure 8 to 11 show the phase, line voltage and their THD obtained through using APOD. Figure 9 shows that the phase voltage has a THD of 33.46% with triplen sideband harmonics which cancel out in the line voltage as indicated in Fig. 11. The THD of the line voltage is 29%.

The waveform of the phase, line voltage and their THD obtained using PD as the modulating technique are shown in Fig. 12 to 15. The phase voltage has a 33.27% THD and a 17.40% THD of the line voltage as shown in Fig. 13 and 15, respectively.

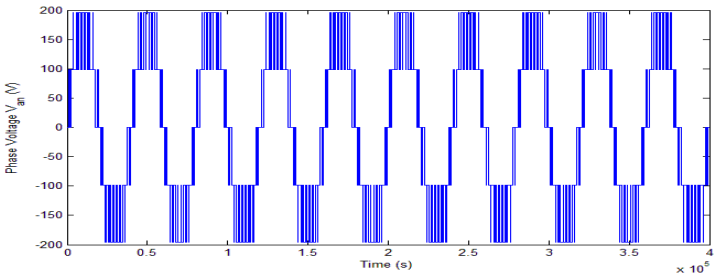

Fig. 8: Phase voltage V_{an} for APOD

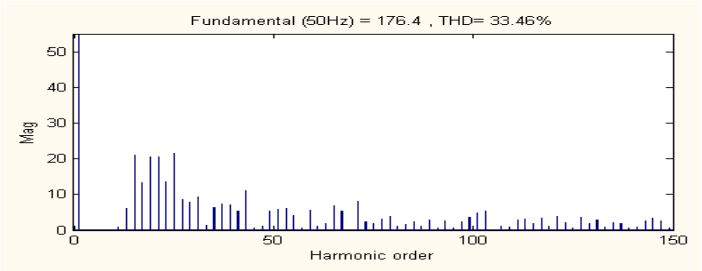

Fig. 9: THD for the phase voltage of APOD

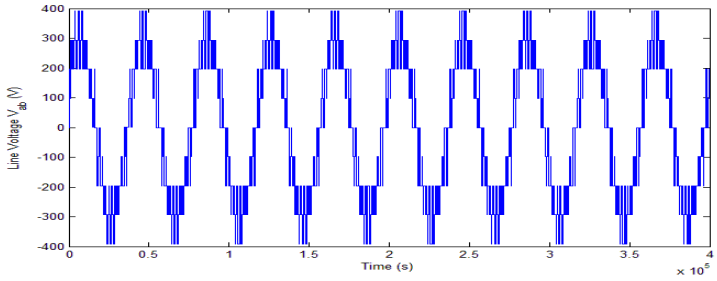

Fig. 10: Line voltage V_{ab} for APOD

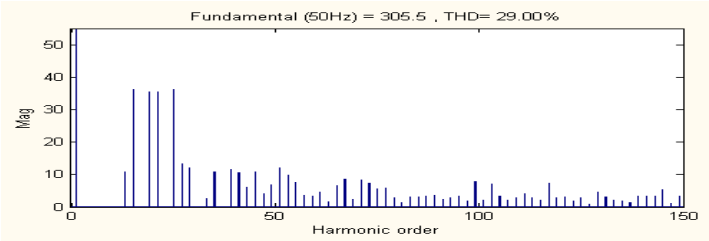

Fig. 11: THD for the line voltage of APOD

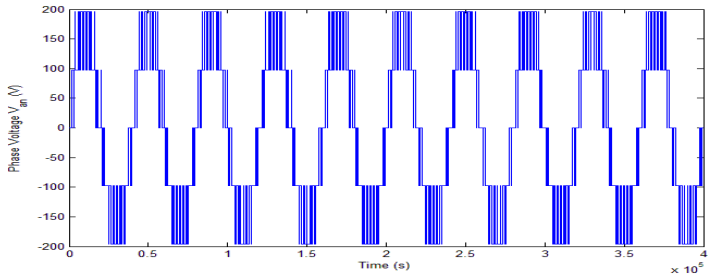

Fig. 12: Phase voltage V_{an} for PD

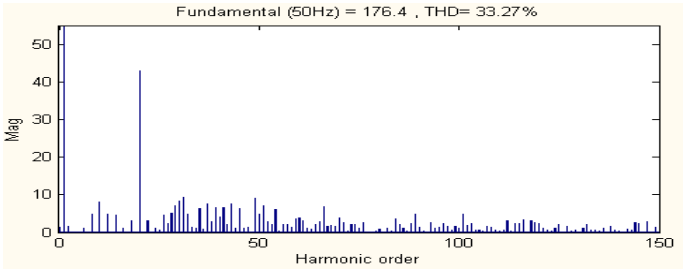

Fig. 13: THD for phase voltage of PD

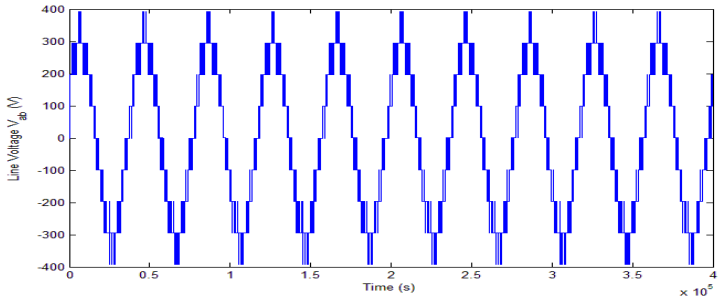

Fig. 14: Line voltage V_{ab} for PD

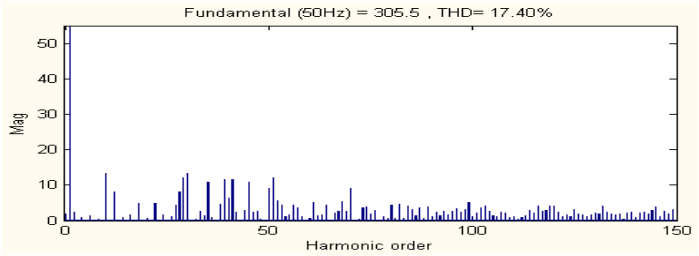

Fig. 15: THD for line voltage of PD

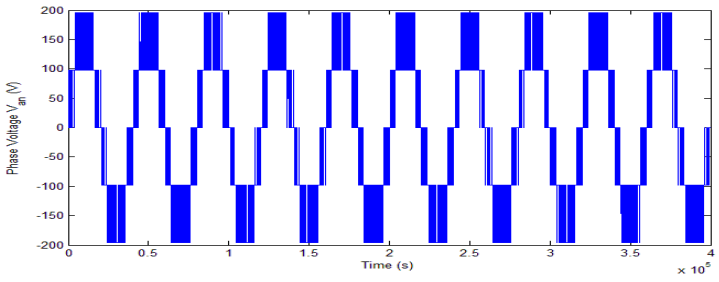

Fig. 16: Phase voltage V_{an} for IPD

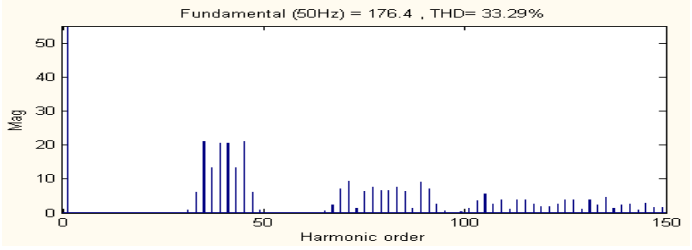

Fig. 17: THD for phase voltage of IPD

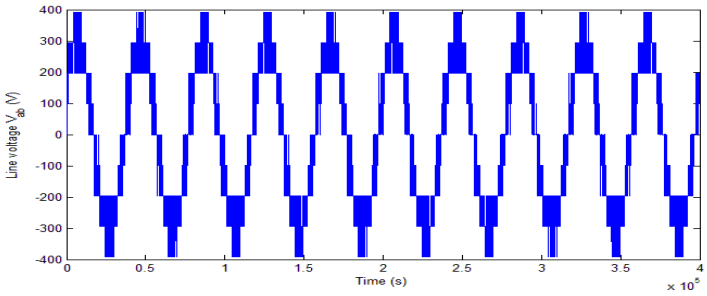

Fig. 18: Line voltage V_{ab} for IPD

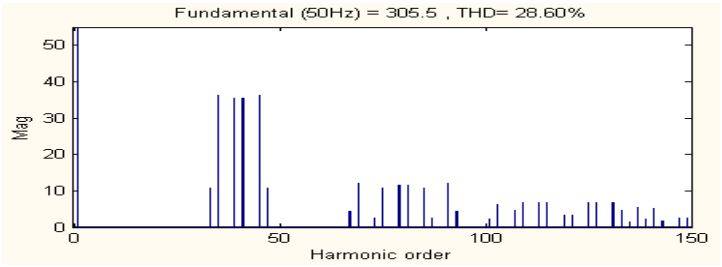

Fig. 19: THD for line voltage of IPD

Figure 16 to 19 shows the IPD simulations of the phase voltage, line voltage waveform and their THD. 33.29% THD in the phase voltage with the harmonic content push to higher order. Triplen sideband harmonics are also cancelled in the line voltage resulting to 28.60% THD.

CONCLUSION

This study shows that modulation strategies based on multilevel SPWM like APOD and PD can be used in five-level HNPC inverter as IPD could. PD had the best line-to-line harmonics performance as the most significant harmonics is the fundamental component and other carrier harmonics cancel on common mode between the inverter phase legs, as shown in Fig. 15. IPD and APOD had almost similar THD performance with IPD being slightly better.

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