Research Journal of Applied Sciences, Engineering and Technology 7(3): 559-564, 2014
DOI:10.19026/rjaset.7.290
ISSN: 2040-7459; e-ISSN: 2040-7467

Submitted: November 10, 2012 Accepted: January 07, 2013 Published: January 20, 2014

Research Article

Digital Decimation Filter of ADSL: Design and Implementation

Hassan Fathabadi
Azad University (Ezeh Branch), Khozestan Iran

Abstract: In this study four proposed structures for the digital decimation filter which is used in $\sum\Delta$ A/D converters of Asymmetrical Digital Subscriber Line (ADSL) are presented. Single multi rate (Finite Impulse Response) FIR, single multi rate (Infinite Impulse Response) IIR, three stages comb-FIR-FIR and comb-IIR-FIR are the four proposed structures. The hardware minimization is considered for each structure. The simulation results and the implementation of each structure are presented. Finally, a comparison between the four proposed structures is done to choose the best proposed structure based on the hardware cost.

Keywords: FIR filter, IIR filter, multi rate filter

INTRODUCTION

Asymmetrical Digital Subscriber Line (ADSL) is very important facility used in many homes and other internet connection centers. It is an application of the digital signal processing techniques which enables home users and consumers to access the high speed applications of internet such as video-on-demand. ADSL provides a downstream capability up to 4 Mbit/s over the existing telephone wires, within a distance up to a few kilometers. Analog signal transmission of ADSL requires high speed and high resolution Analog-to-Digital (A/D) converters. A/D converters can be implemented using ΣΔ modulators which allow high sampling rate meanwhile minimize the hardware (Hauser, 1991; Bourdopoulos *et al*., 2006; Aboushady *et al*., 2001). High resolution can be achieved through by filtering and decimating a high rate bit stream (Crochirer and Rabiner, 1983; Hongzhi *et al*., 2006). Recently, single multi rate FIR, single multi rate IIR, decimation filter, three stages comb-FIR-FIR and comb-IIR-FIR are the subjects of many interesting researches (Shahana *et al*., 2008; Johansson and Wanhammar, 1999; Barrak *et al*., 2007; Ciric and Radonjic, 2011; Soo-Chang *et al*., 2012; Dong and Ya, 2011; Tseng and Lee, 2008a, b). In this study, these are the topics which will be used to present four proposed structures.

ADSL STRUCTURE

Figure 1 shows a schematic diagram of the ADSL. Data conversion in ADSL requires 12 bits of resolution at 4 MHz Brambilla and Guidi (2005). The decimation filter highlighted in Fig. 1 is used for reducing the sampling rate from 64 MHz to 4 MHz and also achieving the appropriate resolution which is necessary.

Table 1: Decimation filter specifications

Output word resolution	12 bit
Output word rate	4 MHz
Pass band	0 MHz-2 MHz
Transition band	2 MHz-2.4 MHz
Decimation factor	16
Stop band attenuation	-66 dB
Pass band ripple	0.2 dB

The specifications of the decimation filter are shown in Table 1.

SINGLE STAGE ARCHITECTURE OF THE DECIMATION FILTER

A single stage realization of the decimation filter can be done using either a multi rate FIR or IIR filter.

Single stage multi rate FIR decimation filter: The frequency response and unit step response of the proposed single stage multi rate FIR decimation filter are shown in Fig. 2 and 3, respectively. The order of the proposed FIR filter is 152, so the filter requires many numbers of coefficients (153 coefficients). The implementation of the proposed single stage FIR decimation filter can be done by choosing one of the following methods:

- A RAM is used to store the input samples and a ROM is used to store the coefficients.
- Reduction in hardware complexity and power consumption can be done using Signed Digit (SD) representation. SD representation of A is as the form of $A=\sum_{k=-M}^{+N} a_k 2^k$ where $a_k \in \{-1,0,1\}$, M and N are positive integer number. The minimal SD representation uses only two non-zero digits, for

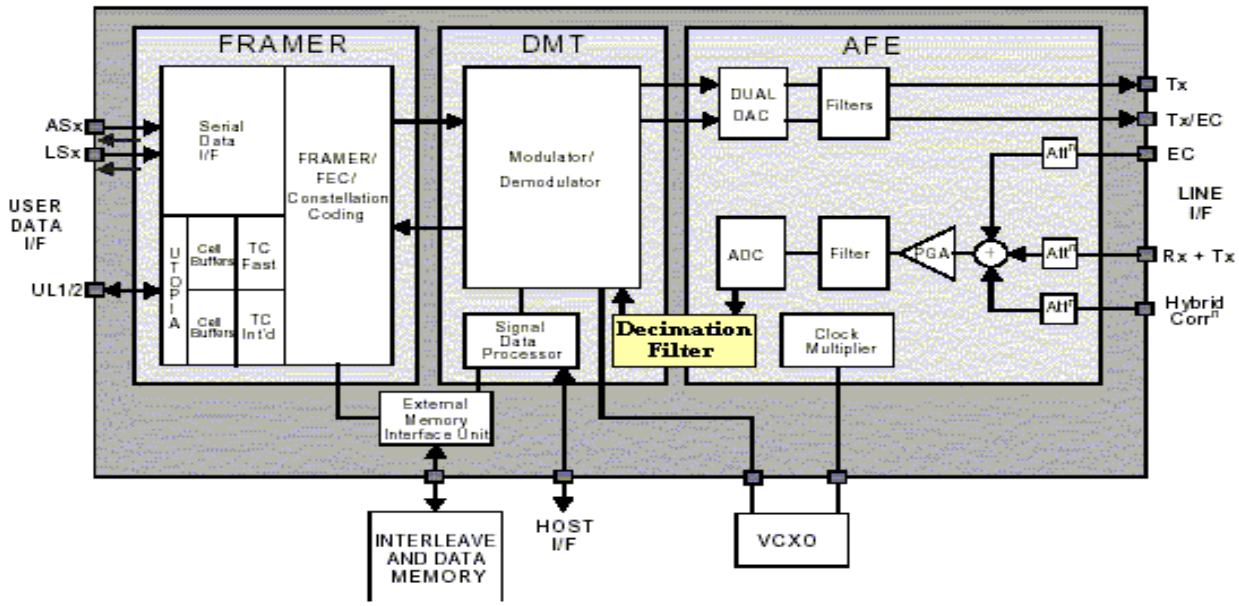

Fig. 1: Schematic diagram of the Asymmetrical Digital Subscriber Line (ADSL)

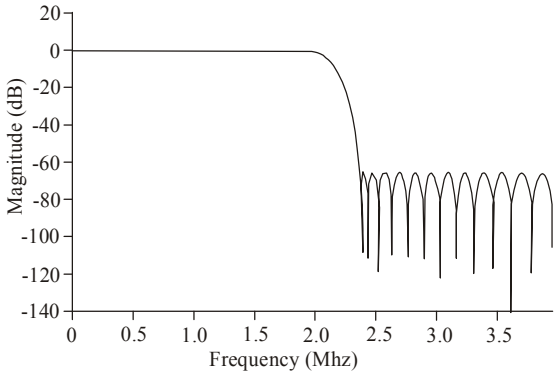

Fig. 2: Frequency response of the single stage multi rate FIR decimation filter. Magnitude (vertical axis) vs frequency (horizontal axis)

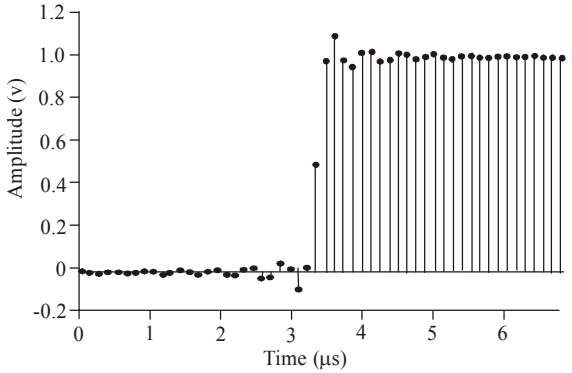

Fig. 3: Step response of the single stage multi rate FIR decimation filter. Amplitude (vertical axis) vs time (horizontal axis)

example minimal SD representation of 0.484375 is $+ 2^{-1} - 2^{-6}$, so only two right shifts of the input sample and only one "ADD" are required to perform the multiplication. As a result, the implementation of the filter is done using only some shift registers (instead of the RAM and the ROM mentioned in the first method). In fact, minimal SD representation of the coefficients allows that the implementation of the normalized coefficients ($|C_k| \leq 1$) can be done with only right shifters subsequently wasting area and power is effectively reduced (Brambilla and Guidi, 2005; Abed *et al*., 2005).

Based on the method 2 and by exploiting the symmetry of filter coefficients, the implementation of the proposed single stage multi rate FIR decimation filter can be done using 307 right shift registers (153 right shift registers are used to store input samples and 154 right shift registers are used for filter coefficients according to the SD representation) (a similar case is shown in Fig. 8).

Single stage multi rate IIR decimation filter: The frequency response and unit step response of the proposed single stage multi rate IIR decimation filter are shown in Fig. 4 and 5, respectively. The order of the proposed IIR filter is 7 and converting the IIR to non-recursive form results that the number of the effective normalized coefficients ($10^{-6} \leq |c_k| \leq 1$) is 205, so the filter really requires a huge number of coefficients to realize. Similar to the FIR decimation filter, the implementation of the proposed single stage IIR decimation filter can be done using a RAM and a ROM or some replaced shift registers when minimal SD representation of the coefficients is applied. In this case similar to the FIR filter presented in previous section, the implementation of the IIR filter can be done using 411 right shift registers.

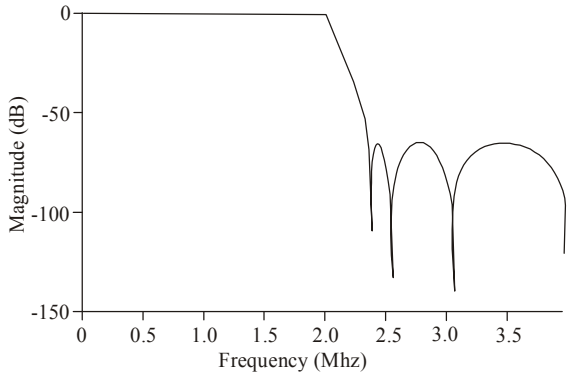

Fig. 4: Frequency response of the single stage multi rate IIR decimation filter. Magnitude (vertical axis) vs frequency (horizontal axis)

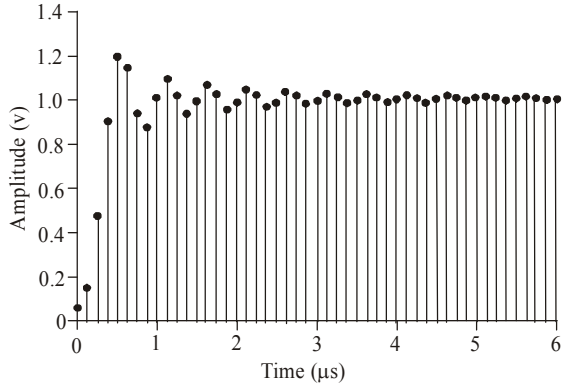

Fig. 5: Step response of the single stage multi rate IIR decimation filter. Amplitude (vertical axis) vs time (horizontal axis)

MULTISTAGE ARCHITECTURE OF THE DECIMATION FILTER

Single stage FIR and IIR implementations of the decimation filter, which were presented in section 3, require so many coefficients that results to occupy a large area of the silicon chip. To solve this problem a multistage architecture is a good solution. It is clear that an anti-aliasing filter is necessary in order to reduce the sampling rate. There are two appropriate multistage architectures that are comb-FIR-FIR and comb-IIR-FIR. The comb-FIR-FIR architecture consists of the following stages:

- A pre-filter with the comb behavior and subsequently a frequency response as the form of $H(z)=\sum_{n=0}^{N-1} z^{-n}$.
- A FIR equalizer to compensate the attenuation in the band pass region done by the pre-filter.
- A FIR filter as third stage with very steep transition behavior for making a suitable stop-band attenuation.

The comb-IIR-FIR architecture has similar architecture with the exception of the second stage is implemented with one IIR filter. Sampling rate in the input of the two architectures (64 MHz) can be reduced with the factor of 2^n in the first and other stages. This results the factorization of the decimation factor and subsequently reducing the very huge computation tasks. In the proposed decimation filter, the sampling frequencies in the first, the second and the third stage are chosen as 16 MHz, 8 MHz and 4 MHz, respectively. It is clear that sub-sampling factors for the first, the second and the last stage are 4, 2 and 2, respectively.

IMPLEMENTATION OF THE MULTISTAGE DECIMATION FILTER

In this section the implementations of the three-stage comb-FIR-FIR and comb-IIR-FIR decimation filters are presented. The block diagram of the filter is shown in Fig. 6 and the implementations of each stage of the proposed filter are separately presented in following three sections.

Implementation of the first stage (comb filter): The first stage of the proposed decimation filter is a comb filter because this stage of the filter must work at very high sampling frequency Maity and Das (2012). A comb filter of length N is a FIR filter which all its N coefficients are one, so its transfer function is:

$$H(z)=\sum_{n=0}^{N-1} z^{-n} \quad (1)$$

Eq. (1) can be rewritten as:

$$H(z)=\frac{1-z^{-N}}{1-z^{-1}}=\left(\frac{1}{1-z^{-1}}\right)(1-z^{-N})=G_I(z).G_D(z) \quad (2)$$

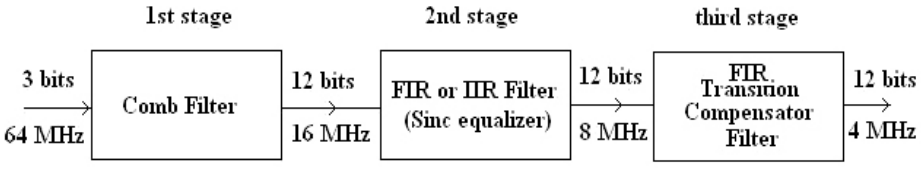

Fig. 6: Block diagram of the three-stage comb-FIR-FIR and comb-IIR-FIR decimation filters

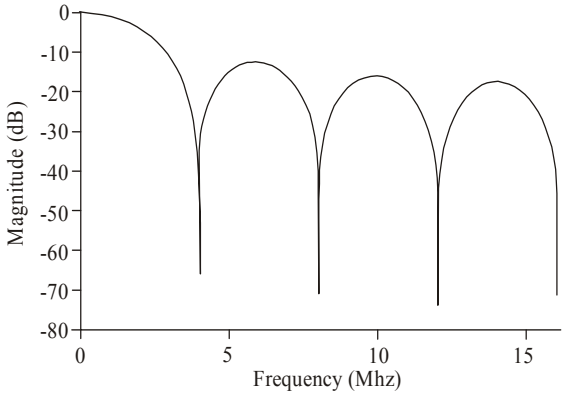

Fig. 7: Frequency response of the first stage (comb filter). Magnitude (vertical axis) vs frequency (horizontal axis)

where $G_I(z)$ and $G_D(z)$ are the transfer functions of the integration and differentiation parts of the comb filter, respectively. The integration and differentiation parts act as accumulator and differentiator, respectively. Since the comb filter is a first stage of the decimation filter, so differentiation function ($G_D(z)$) can be done at the lower rate. It is clear that this stage (comb filter) of the proposed decimation filter has following properties:

- No storage is required for filter coefficients
- No multipliers are required
- Intermediate storage is reduced by integrating ($G_I(z)$) at high sampling rate (64 MHz and 3 bit) and differentiating ($G_D(z)$) at the low sampling rate (16 MHz and subsequently 12 bit)

Now, we consider comb filter function with N = 8 as following equation:

$$H(z) = \frac{1}{8}\sum_{n=0}^{7} z^{-n} \tag{3}$$

And subsequently:

$$H(z) = \frac{1}{8}.\frac{1-z^{-8}}{1-z^{-1}} = \frac{1}{8}.(\frac{1}{1-z^{-1}})(1-z^{-8}) \tag{4}$$

So, the accumulator transfer function can be expressed as:

$$G_I(z) = \frac{1}{8}.(\frac{1}{1-z^{-1}}) \tag{5}$$

And also the differentiator transfer function is written as:

$$G_D(z) = 1-z^{-8} \tag{6}$$

The frequency response of the comb filter is shown in Fig. 7. A single comb filter does not have appropriate ripple in band pass and enough stop band attenuation, so two other stages rare required. Second stage (FIR or IIR equalizer) is required to provide appropriate band pass response and third stage is necessary to provide a good transition response and enough stop band attenuation.

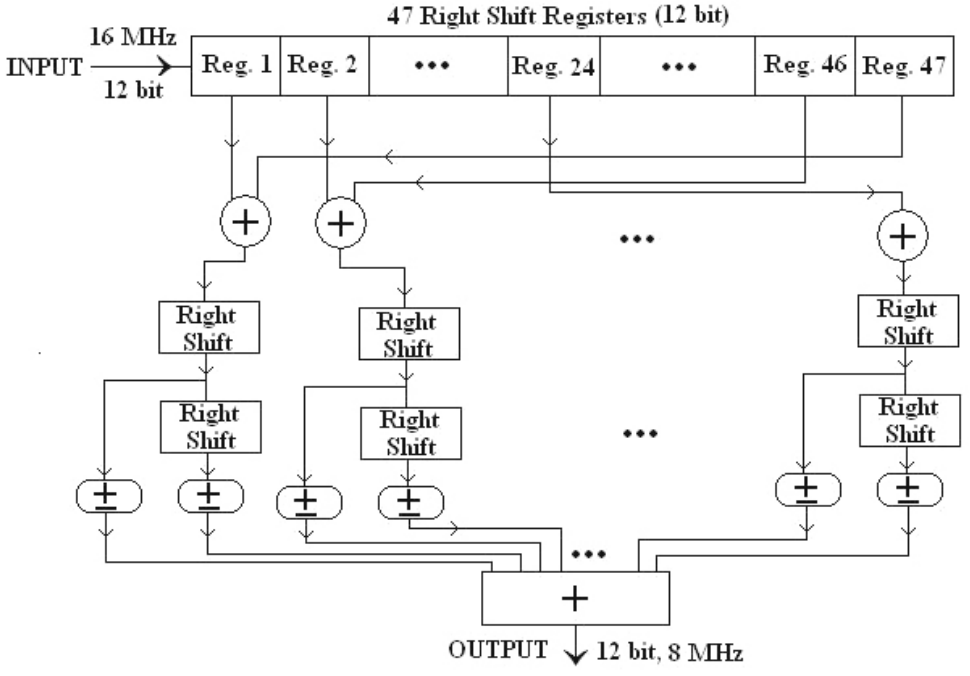

Fig. 8: Implementation of the second stage (FIR equalizer)

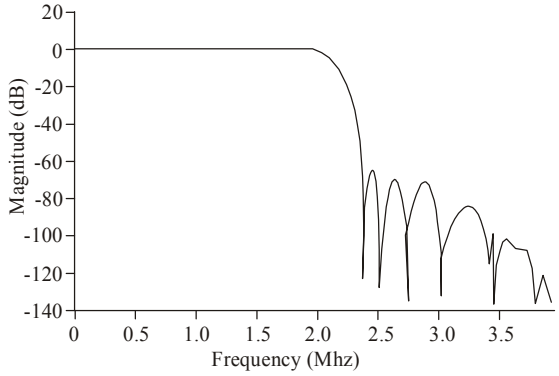

Fig. 9: Frequency response of the whole comb-FIR-FIR decimation filter. Magnitude (vertical axis) vs frequency (horizontal axis)

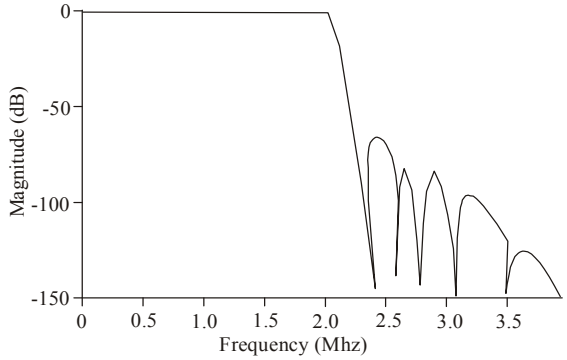

Fig. 10: Frequency response of the whole comb-IIR-FIR decimation filter. Magnitude (vertical axis) vs frequency (horizontal axis)

Implementation of the second stage (FIR and IIR equalizer): The SD representation of the coefficients results a simple implementations of FIR or IIR equalizer. Input samples are stored in the right shift registers (instead of RAM) and coefficients are provided with right shift registers (instead of ROM). It is clear that the implementation of this stage is simple with an effective structure that requires minimum hardware. The order of the FIR equalizer filter is 46, consequently the implementation is done using only 95 right shift registers as shown in Fig. 8. Similarly, the IIR equalizer is done using 117 right shift registers.

Implementation of the last stage (transition FIR filter): The last stage of the decimation filter is a FIR filter which is implemented using only shift registers because of using SD representation of the coefficients. This FIR filter improves the transition response of the final decimation filter. The order of this filter is 86, so it can be implemented using 175 right shift registers. It can be seen that the output of the last stage is a data as the form of 12 bits with the sampling rate of 4 MHz while the input of this stage has the sampling rate of 8 MHz.

Table 2: A comparison between four proposed structures

Structure	Number of Right Shift Registers Used in Implementation
Multi rate FIR decimation filter	307
Multi rate IIR decimation filter	411
Three-stage comb-FIR-FIR decimation filter	95+175 = 270
Three-stage comb-IIR-FIR decimation filter	117+175 = 292

Frequency response of the multistage decimation filter: The frequency responses of the comb-FIR-FIR and comb-IIR-FIR decimation filters are shown in Fig. 9 and 10, respectively. Comparing two three stages filters shows that the hardware of the comb-FIR-FIR is lass than the comb-IIR-FIR hardware.

A COMPARISON BETWEEN FOUR PROPOSED STRUCTURES

Four structures of the digital decimation filter which is used in ΣΔ *A*/*D* converters of ADSL were presented in previous sections. Based on the SD representation of the coefficients, a comparison between the four structures is done in Table 2. The comparison shows that the three-stage comb-FIR-FIR decimation filter requires the hardware which is less than the other three structures.

CONCLUSION

In this study, four structures of the digital decimation filter used in ΣΔ *A*/*D* converters of ADSL were presented. These four structures were single multi rate FIR, single multi rate IIR, three stages comb-FIR-FIR and comb-IIR-FIR. The hardware minimization was done using the minimal SD representation of the coefficients. The simulation and implementation results were presented. A comparison between the four proposed structures was done to choose the best structure which has the minimal hardware cost.

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