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Research Article

CDMA Technique with Inter-process Communication

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Abstract: A novel implementation of Inter process communication in CDMA NOC is proposed. In this study, the orthogonality properties of a Walsh code are used to route data packets between the IP-Cores.The asynchronous circuit design with combinational logic (Gate level design) is used for transmission and receiving circuits, along with ip-cores and reduces the processing time and resource utilization. The use of asynchronous pipelined core design process increases the operating frequency as well. The data transfers over IP-Core based interconnect is implemented on gate level. The latency and throughput values are obtained for variable payload size. The performance of asynchronous and synchronous communication are measured and analyzed.

Keywords: Asynchronous and synchronous communication, CDMA NOC NoC, inter-process communication, walsh codes

INTRODUCTION

System-on Chip (SoC) applications can utilize a large number of Processing Elements (PEs), such as processor cores, DSP cores, memory units, dedicated hardware units and/or programmable hardware units. The conventional bus based SoC architectures use high performance buses AMBA, IBM' score connect, ST Microelectronic's STB us etc. However, there is need for more powerful and effective communication techniques to link large numbers of core units since the traditional bus based architecture may not meet the requirements of future SoC designs in terms of scalability, higher throughput and reliability. In this study, a novel Network-on-Chip (NoC) architecture for Code Division Multiple Access (CDMA) technique is proposed. Future, System-on-Chip (SoC) architectures are predicted to become communication-bound. The System-on-Chips (SoCs) utilize topologies based on shared buses. It proposes design specific wires with general purpose, (packet-switched) network, hence, marking the beginning of Network-on-Chip (NoC) era.

Goals of network-on-chip paradigm: The basic principles of NoC paradigm have various seminal articles. The basic properties of the NoC are follows:

- It separates communication from computation
- It avoids global, centralized controller for communication
- It provides optimize routing
- It offers support for system testing

However, there is no commonly-agreed definition for the minimum network configuration that is still a real "NoC". There are quite a few circuit-switched approaches dubbed as NoCas well. However, the opposite goal is not meaningful anyway. It must be possible to measure the desired properties, either numerically or with Boolean values (true/false). For example, if scalability, flexibility, or simplicity is taken as requirement, some exact criteria or measuring unit must also be explicitly defined. Consequently, it adopts a simple and neutral, although loose, definition that "network-on-chip is a communication network targeted for on chip".

Shandhag (2004) presented reliable and efficient system-on-chip design. The system bus is the simplest example of as hared communication architecture topology and is commonly found in many commercial SoCs. Several masters and slaves can be connected to a shared bus.

In a typical SoC with inter connecting multiple nodes, each node execute and independently attempt to simultaneously share the same components. Hence, to ensure that the individual nodes complete in the same appropriate manner and provide correct results, synchronization is required.

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LITERATURE REVIEW

Jongsun *et al*. (2007) proposed design of an interconnect architecture and signaling technology for parallelism in communication. The conventional Time-Division Multiplexing (TDM) protocol-based inter-connects has been brought on by the continued increase of required communication bandwidth and concurrency of small-scale digital systems. Xin *et al*. (2007) presented applying CDMA technique to Network-on-Chip. An on-chip packet switched communication network that applies the CDMA technique and supports the GALS communication scheme was also proposed. Ankur *et al*. (2009) proposed survey of Network on Chip (NoC) architectures and contributions. It analyzed the state-of-the-art in the field of Network-on-Chip (NoC) benchmarking and comparison. Dally and Towles (2001) presented route packets, Not Wires: On-Chip Interconnection Networks. The large Systems-on-Chip (SoC) can employ packet-switched Networks on-Chip (NoC). Typically, NoC is based on module connection via a mesh-type network of routers. Benini and De Micheli (2004) presented Network-on-chip architectures and design methods.

The NoC is an emerging interconnection design methodology, which is seen as a promising solution to provide scalable, energy efficient and reliable communication for System on Chip. Shandhag (2004) presented reliable and efficient system-on-chip design. The system bus is the simplest example of a shared communication architecture topology and is commonly found in many commercial SoCs. Several masters and slaves can be connected to a shared bus. Kim *et al*. (2008) proposed CDMA based network-on-chip architecture. It reduces power consumption while securing cost optimization and efficient router architectures have evolved for the NoC. Bell *et al*. (2001) proposed using PN sequences to route packets between processors in a multi-processor network.

However, it used only one large central switching element to perform all of the routing and did not consider issues such as buffering and packet contention. Pande *et al*. (2003) proposed design of switch for network on chip applications. A switched network architecture using traditional binary signaling and includes capabilities for packet buffering and contention resolution that are targeted specifically for NoC applications. A star network topology is well matched to the CDMA switching element and which can be hierarchically scaled to handle a large number of IP blocks. Lahiri *et al*. (2005) presented design of communication architectures for high-performance and energy-efficient systems-on-chip. In numerous applications, ring based applications are widely used, such as network processors, ATM switches. Lai *et al*. (2004) proposed CT-bus: A Heterogeneous CDMA/TDMA Bus for Future SOC. CDMA has been proposed as an alternative way for interconnect of IP cores in a SoC design, or as a solution for interconnecting modules within a system realized in several PCBs.

METHODOLOGY

System design: In this study, focus on NoC and its actual operation and performance with dependency on the granularity of the configuration is studied. This relates to the synchronization needed among the various nodes of NoC that execute simultaneously (both coarse and medium granularity require synchronization). The transportation of data packets among various cores in a NoC can be performed by the use of either serial or parallel connections. Parallel links make use of a buffer-based architecture and can be operated at a relatively lower clock rate in order to reduce power dissipation. This can also reduce the impact of expensive DRAM and remote cache accesses. However, these parallel links will incur high silicon cost due to inter-wire spacing, shielding and repeaters. This can be minimized up to a certain limit by employing multiple metal layers. On the other hand, serial links allow savings in wire area, reduction in signal interference and noise and further eliminate the need for having buffers. On the demerit side, serial links would need serializer and de-serializer circuits to convert the data into the right format to be transported over the link and back to the cores. However, in this study, no such circuits are required. Serial links sometimes suffer from Inter-Symbol Interference (ISI) between successive signals while operating a thigh clock rates. Such drawbacks are addressed by encoding with asynchronous communication protocol wherever applicable. The technique is using for transmission and receiving circuits along with ip-cores and achieve reduction in the processing time and recourse utilization.

NoC architecture: The NoCs consist typically of routers, network adapter (network interface) and connections:

- **Router:** Directs the data according to the protocol selected. It contains the routing strategy
- **Network adapters:** Provide a bridge between the router and the element attached to them. Their main task is to separate calculation (IPs) of the communication (network). This consists of two operations, protocol conversion and packages construction
- **Connections:** Are the channels of transmission of data between the various circuit elements to the network

Globally asynchronous locally synchronous (gals) principle: The CDMA NoC is a packet switched network that consists of "Network Node," "CDMA Transmitter," and "Network Arbiter" blocks as shown in Fig. 1. The functional IP blocks (functional hosts) are connected to the CDMA NoC through individual "

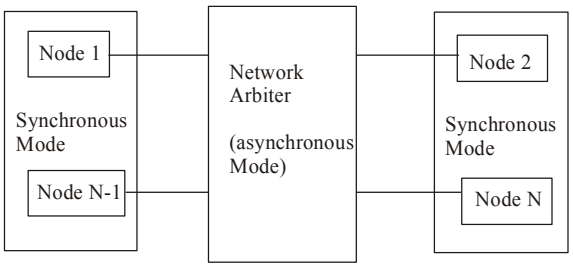

Fig. 1: GALS structure

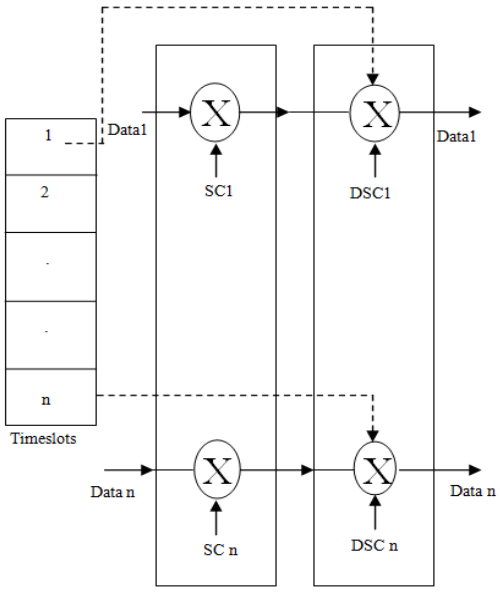

Fig. 2: Modulation and demodulation

Network Node" blocks. "CDMA Transmitter" and "Network Arbiter" blocks perform the CDMA communications in the network. Because the different functional hosts may work at different clock frequencies as given in Fig. 1 coordinating the data transfers among different clock domains would be a problem. A Globally Asynchronous Locally Synchronous (GALS) scheme is proposed as a solution for this problem. Applying the GALS scheme to the CDMA NoC means that the communications between each functional host and its network node use local clock frequency, while the communications between network nodes through the CDMA network are asynchronous. In the GALS scheme, both synchronous and asynchronous circuits are applied in the design.

Asynchronous circuits consume low power due to fine-grain clock gating and zero standby power consumption. They can operate at higher speeds since the operating speed is determined by actual local latencies rather than global worst-case latency. The emission of electromagnetic noise is less and is robust towards variations in supply voltage, temperature and fabrication process parameters (since timing is based on matched delays). These circuits do not face clock distribution and clock skew problems since; there is no global signal that has to be distributed with minimal phase skew across the circuit.

Merits of proposed NOC:

- Gates Based Lu T-Less Structure
- **Serial communication:** Serial links offer the advantages of:
  - Simpler layout and simpler timing verification
  - Savings in wire area
  - Reduction in signal interference and noise,
  - Further eliminate the need for having buffers
- **Asynchronous design:** Reduces ISI (Inter-symbol Interference) between successive signals while operating at high clock rates
- Clock based on Channel Characteristics [BW/ Processing Time etc.]
- Single pipelined block:
  - Reduced delay
  - Increases the operating frequency

Motivations for using CDMA technique: A consequence of shrinking transistor dimensions, a complexity of VLSI ICs, from the aspect of number of transistors, increases at faster rate than designer's possibilities. To use these benefits the design-space exploration for SoCs has been mainly focusing on the computational aspects of the problem, i.e., increasing microprocessor and peripheral chip performance. However, as the number of IP blocks on a single chip and their performance continue to increase, a shift from computation based to communication-based designs becomes mandatory. In order to increase system performance it is necessary to design high speed and high bandwidth data transfer buses. In contrary, further performance increase of computer constituents will be without an effect on overall system performance. The data from different senders are encoded using a set of orthogonal spreading codes, at the end of sending data. The encoded data from different senders are added together for transmission without interfering with each other because of the orthogonal property of spreading codes. The orthogonal property means that the normalized autocorrelation value and the cross-correlation value of spreading codes are 1 and 0, respectively. Because of the orthogonal property, at the receiving end, the data can be decoded from the received sum signals by multiplying the received signals with the spreading code used for encoding. This is illustrated in Fig. 2.

Network node structure in the CDMA NOC: The block diagram of the network node structure of the CDMA NoC is shown in Fig. 3 where the arrows represent the flows of data packets. In Fig. 3, the "network if" block which belongs to the functional host is an interface block for connecting a functional host with a "network node." The GALS scheme is applied in

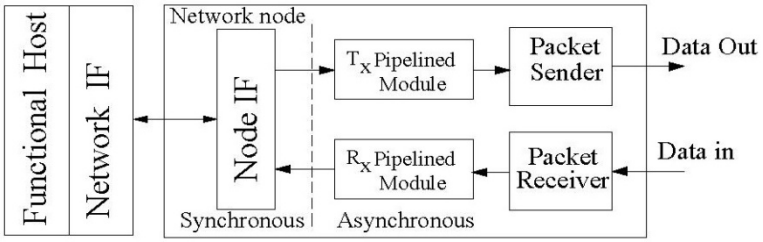

Fig. 3: Network node structure of the CDMA NoC

"network node" block of the CDMA NoC by using synchronous design in the "node if" sub-block and using asynchronous design in the other sub-blocks.

The network interface standards supported in the CDMA NoC also include the VCI and OCP standards. The sub-blocks in the network node will be addressed in the following four paragraphs:

- **Node if:** This block is used to assemble the data from "functional host" into packets and send the packets to "Tx packet buffer" or disassemble the received packet from "Rx packet buffer" and send the extracted data to "functional host".
- **Tx/Rx packet buffer:** "Tx packet buffer" is used to store the data packets from "node if," and then deliver the packets to "packet sender." The "Rx packet buffer" stores and delivers the received packets from "packet receiver" to "node if".
- **Packet sender:** If "Tx packet buffer" is not empty, "packet sender" will fetch a data packet from the buffer by an asynchronous handshake protocol. Then it will extract the destination information from the fetched packet and send the destination address to "network arbiter." After "packet sender" gets the grant signal from the arbiter, it will start to send data packets to "CDMA transmitter".
- **Packet receiver:** After system reset, this sub block will wait for the sender information from "network arbiter" to select the proper spreading code for decoding After the spreading code for decoding is ready, the receiver will send an acknowledge signal back to "network arbiter" and start to receive data from "CDMA transmitter," and then send the decoded data to "Rx packet buffer" in the packet format.

Inter process communication: This process mechanism enables processes to convert data that is normally formatted into message according to some predefined protocol and involved different communication processes.

Asynchronous communication: In the asynchronous Communication, two nodes of NoC communicate

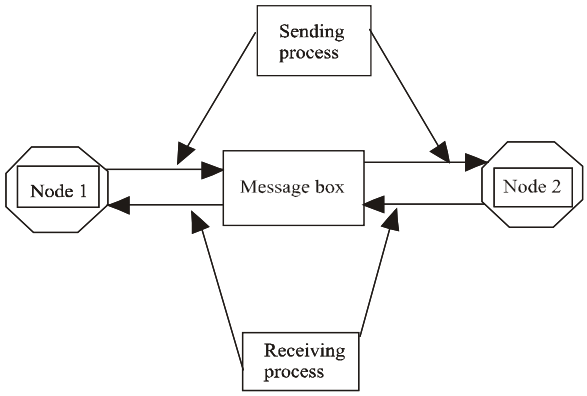

Fig. 4: Two node communication via message box

indirectly via a intermediate that holds the message temporarily. It has no direct interaction between the sender node and receiver node. A system in which the sender node sends the message is placed in a slot of the intermediate node, the receiver node gets the message from the intermediate node. A two node communications via a intermediate node is shown in Fig. 4.

The sender/receiver data has to wait if intermediate node is full or empty. If there is no free slot left, the sender node may have to wait until a space is available. Similarly, the receiver node also has to wait, if the slots are empty. Several methods that insert a message in the intermediate node, where message is defined the following attributes:

- Time stamp
- Sender
- Receiver
- Data in the message

This model includes the important issue of when to carry out the context switch to the newly selected node of NoC.

Synchronous communication: This implies that the communication of a message between two nodes of NoC involve a stronger synchronization than with a synchronous communication. If a sender node attempts to send a message, it gets suspended if the receiver node is not ready to receive a message. The structure

needed for direct communication between sender and receiver is shown in Fig. 5.

RESULTS AND DISCUSSION

Performance of asynchronous communication: The statistical results for the asynchronous communication model are shown in Fig. 6a. The performance measure i.e., the period for each of the process times pent and every process in attempting communication is shown in Fig. 6b.

Synchronous communication: The statistical results for the synchronous communication model are shown in the performance measures i.e., the period for each of the process time spent is shown in Fig. 7a and b and also, the results comparison are tabulated in Table 1.

Transfer latency values: The data transfers over ip-core based interconnect, which used CDMA technique are given in Table 2. This method is implemented on gate level, with modulation and demodulation using VHDL code on FPGA circuit xc3s100e-5vq100.

An efficient system for data transfers using CDMA coded system bus is proposed in this study. It is implemented for 2 cell 64 bit data packets using CDMA coding technique with reduced data transfer latency is obtained and the tabulated in Table 2.

Throughput: Network throughput represents the average rate of successful message delivery over the channel and is synonymous to digital bandwidth consumption. Throughput is measured in bits/sec or data packets/sec or data packets/time slot. In this study, the system throughput or the aggregate throughput is

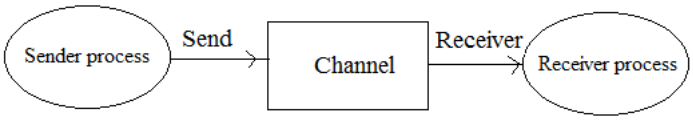

Fig. 5: Synchronous communication between two nodes

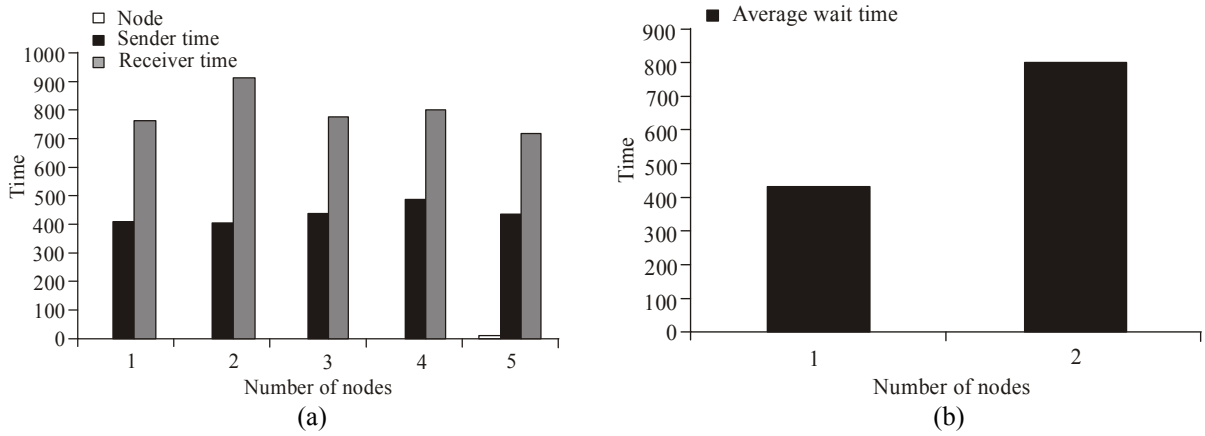

Fig. 6: a) Asynchronous communication, b) average asynchronous communication

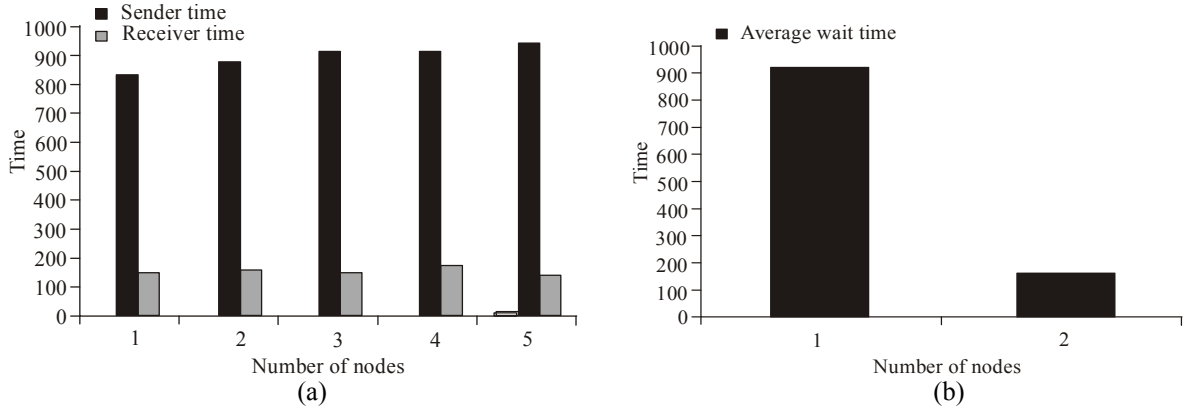

Fig. 7: a) Synchronous communication, b) average synchronous communication

Table 1: Average waiting time in asynchronous and synchronous communication

Type of communications	Average Waiting Time (AWT) for sender (ms)	Average Waiting Time (AWT) for receiver (ms)
Asynchronous communication	424.7577	792.8494
Synchronous communication	900.1414	151.3149

Table 2: Extracted transfer latency values

		Latency		
Blocks	Process	Existing	Proposed	Improvement (%)
Tx/Rx packet buffer	Read/write	22.4 ns	N.A	100
Packet sender	Data processing 2 cell 64 bit data packets	99.2 ns	59.1 ns 32 ns	7
Packer receiver	2 cell 64 bit data packets data processing	192 ns	44 ns 59.1 ns	80
Network processing	After transmission before Rxx processing	64	32 ns	50

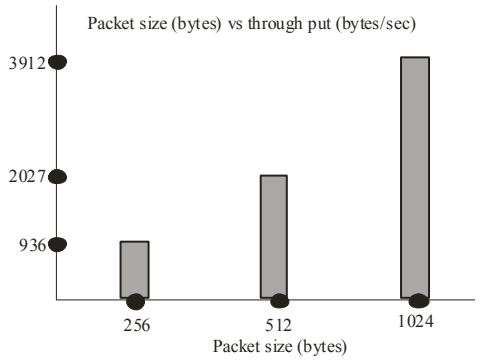

Fig. 8: Throughput for three different packet sizes

obtained. This is defined as the sum of the data rates that are delivered to all the nodes in a NoC and is plotted in Fig. 8 for three different packet sizes with the same length of data handled by the node. The y-axis represents the actual bytes sent and received from the selected node of NoC.

CONCLUSION

We detailed in this study inter-process communication with network on chip using CDMA Technique. In this study, focus on NoC and its actual operation and performance with dependency on the granularity of the configuration is studied. This relates to the synchronization needed among the various nodes of NoC that execute simultaneously.

After system design, we work on the performance of asynchronous and synchronous communication with Code Division Multiple Access code.

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