

Research Article

A Comparative Study on Various Unipolar PWM Strategies for Single Phase Seven Switch Asymmetric 15-Level Inverter

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Abstract: This study presents a modified single phase cascaded 15 level inverter with reduced switch count that operates in asymmetric mode. The proposed multilevel inverter produce DC voltage levels similar to other topologies with less number of semiconductor switches. This study also presents various modulating techniques include sinusoidal pulse width modulation, advance modulating technique. i.e., Trapezoidal reference with triangular carrier waves. Different performance measures like THD, VRMS and CF have also been evaluated by simulation. The simulation of proposed circuit is carried out using MATLAB/SIMULINK and the result for the same are presented in this study.

Keywords: Crest factor, form factor, THD, unipolar carrier overlapping, unipolar phase disposition

INTRODUCTION

The concept of a multilevel inverter is to use a series of connected semiconductor switches in order to reduce the voltage and consequently power that flows through each individual device. The multilevel inverters unique structure allows reaching high voltages and power levels without the use of transformers. They are specially suited to high voltage vehicle drives where low output voltage Total Harmonic Distortion (THD) and Electromagnetic Interference (EMI) are needed. The general function of the multilevel inverter is to synthesize a desired output voltage from several levels of DC input voltages. As the number of levels increases, the synthesized output waveform has more steps, which produces a staircase wave that approaches the desired waveform. Babaei *et al.* (2012) proposed reduced switch multilevel inverter with two independent DC sources. Babaei *et al.* (2007) developed asymmetrical multilevel converter with reduced source and switches. Cascaded multilevel converters with reduced number of switches were introduced in Babaei and Hosseini (2009) and Babaei (2008). Bensraj *et al.* (2010) introduced unipolar PWM using Trapezoidal amalgamated reference. Bensraj and Natarajan (2010) proposed multicarrier Trapezoidal PWM strategies for a single phase five level cascaded inverter. Ceglia *et al.* (2006) introduced simplified multilevel inverter topology. Murugesan *et al.* (2011) proposed reduced switch multilevel inverter for

induction motor drive. Murugesan *et al.* (2012) proposed sinusoidal PWM based modified cascaded multilevel inverter. Malinowski *et al.* (2010) developed various cascaded inverter topologies. McGrath and Holmes (2012) discussed multicarrier PWM technique for multilevel inverter. Urmila and Subbarayudu (2010) proposed various modified reference modulating techniques. This study presents a single phase seven switch asymmetrical 15 level inverter topology for investigation using unipolar sine and trapezoidal reference PWM switching techniques. Simulations were performed using MATLAB-SIMULINK. Harmonic analysis and evaluation of different performance measures for various modulation indices have been carried out and presented.

PROPOSED REDUCED SWITCH MULTILEVEL INVERTER

The proposed inverter consists of less number switches compared to conventional cascaded H bridge inverter. The general structure of a proposed cascaded multilevel inverter is shown in the Fig. 1. This inverter consists of three conversion cell and One H Bridge. Conversion cell consist of only one active switching element and one bypass diode and three separate voltage sources (V_1 , V_2 , V_3), each source connected in cascade with other sources, this make the output voltage in only positive polarity. H bridge circuit makes the output voltage in positive and negative polarity. The

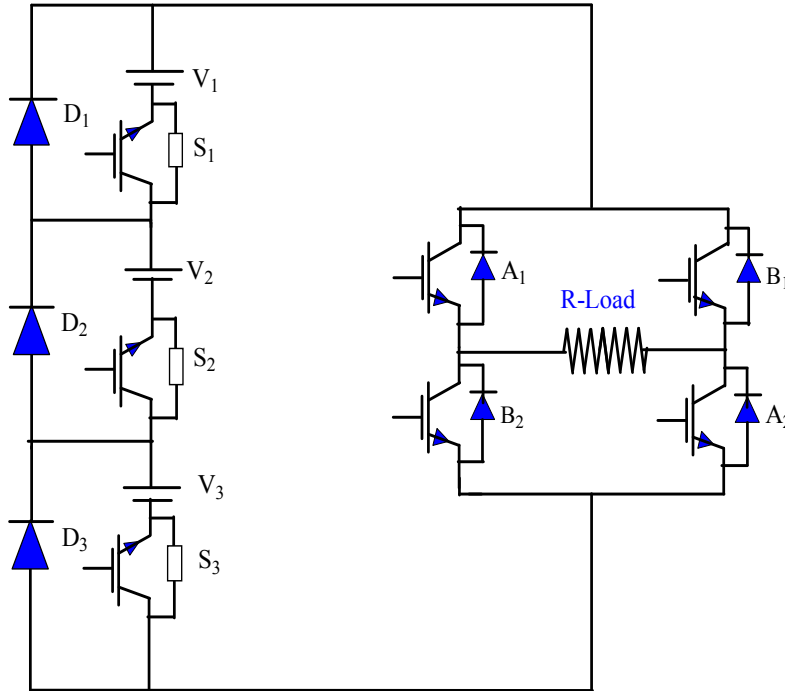


Fig. 1: Proposed reduced switch MLI

inverter consists of seven switches and three separate unequal DC sources with a load.

PWM CONTROL STRATEGIES

In this proposed study a unipolar Sine and Trapezoidal reference wave with a triangular carrier is used to generate firing pulses for a 15 level inverter. For an m-level inverter using unipolar multi-carrier technique, (m-1)/2 carriers with the same frequency f_c and same peak-to-peak amplitude A_c are used. The reference waveform has amplitude A_m and frequency f_m and it is placed at the zero reference. The reference wave is continuously compared with each of the carrier signals. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched on. Otherwise, the device switches off. There are many alternative strategies are possible, some of them are tried in this study and they are:

- Unipolar Phase Disposition PWM strategy (UPDPWM)
- Unipolar Alternate Phase Opposition Disposition PWM strategy (UAPODPWM)
- Unipolar Carrier Overlapping PWM strategy (UCOPWM)

The formulae to find the Amplitude of modulation indices are as follows:
For UPDPWM, UAPODPWM:

$$m_a = 2A_m / (m-1)A_c \quad (1)$$

UCOPWM:

$$m_a = A_m / 4A_c \quad (2)$$

The frequency ratio mf is as follows:

$$m_f = f_c / f_m \quad (3)$$

Unipolar phase disposition PWM: In UPDPWM strategy the carriers of same amplitude and frequency are disposed such that bands they occupy are contiguous. Carrier arrangement for UPDPWM strategy having Sine reference and Trapezoidal are illustrated in Fig. 2 and 3, respectively.

Unipolar alternate phase opposition and disposition PWM: In UAPODPWM strategy the carriers of same amplitude are phase displaced from each other by 180 degrees alternately. Carrier arrangement for UAPODPWM strategy having Sine reference and Trapezoidal are illustrated in Fig. 4 and 5, respectively.

Unipolar carrier overlapping PWM: In carrier overlapping technique, (m-1)/2 carriers are disposed such that the bands they occupy overlap each other; the overlapping vertical distance between each carrier is $A_c/2$. Carrier arrangement for UCOPWM strategy having Sine reference and Trapezoidal are illustrated in Fig. 6 and 7, respectively.

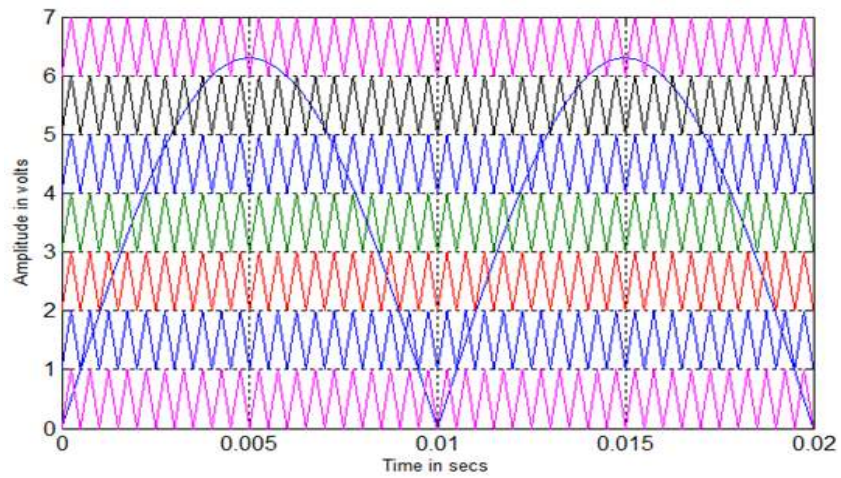


Fig. 2: Carrier arrangement for unipolar sine reference UPDPWM technique ($m_a = 0.9$, $m_f = 40$, $A_c = 1$ and $A_m = 7$)

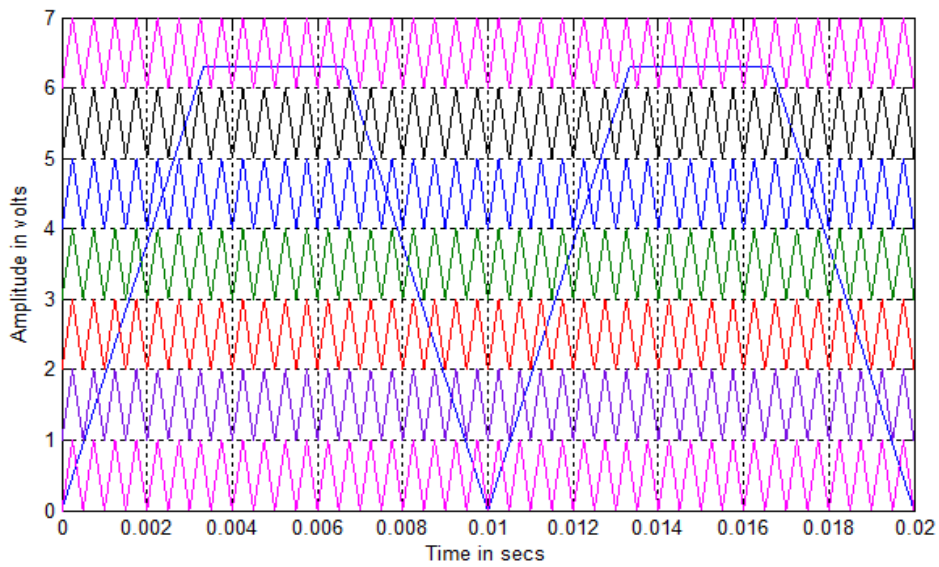


Fig. 3: Carrier arrangement for unipolar trapezoidal reference UPDPWM technique ($m_a = 0.9$, $m_f = 40$, $A_c = 1$ and $A_m = 7$)

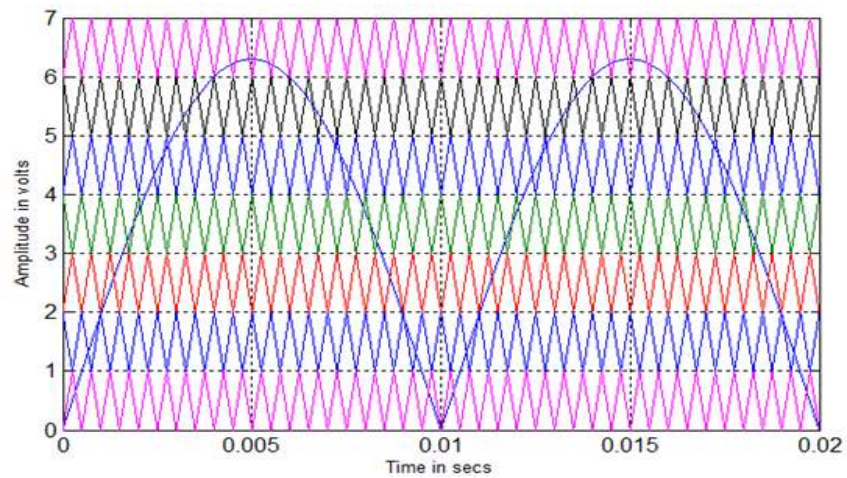


Fig. 4: Carrier arrangement for unipolar sine reference UAPODPWM technique ($m_a = 0.9$, $m_f = 40$, $A_c = 1$ and $A_m = 7$)

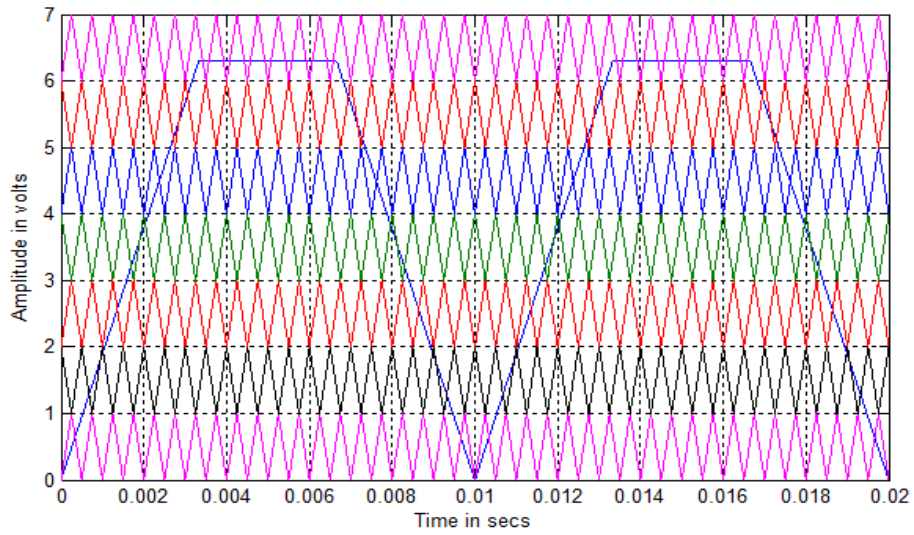


Fig. 5: Carrier arrangement for unipolar trapezoidal reference UAPODPWM technique ($m_a = 0.9$, $m_f = 40$, $A_c = 1$ and $A_m = 7$)

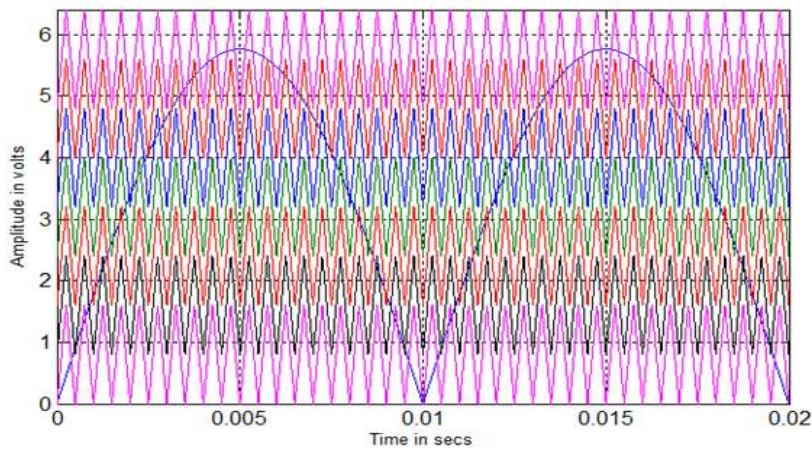


Fig. 6: Carrier arrangement for unipolar sine reference COPWM technique ($m_a = 0.9$, $m_f = 40$, $A_c = 1.6$ and $A_m = 6.4$)

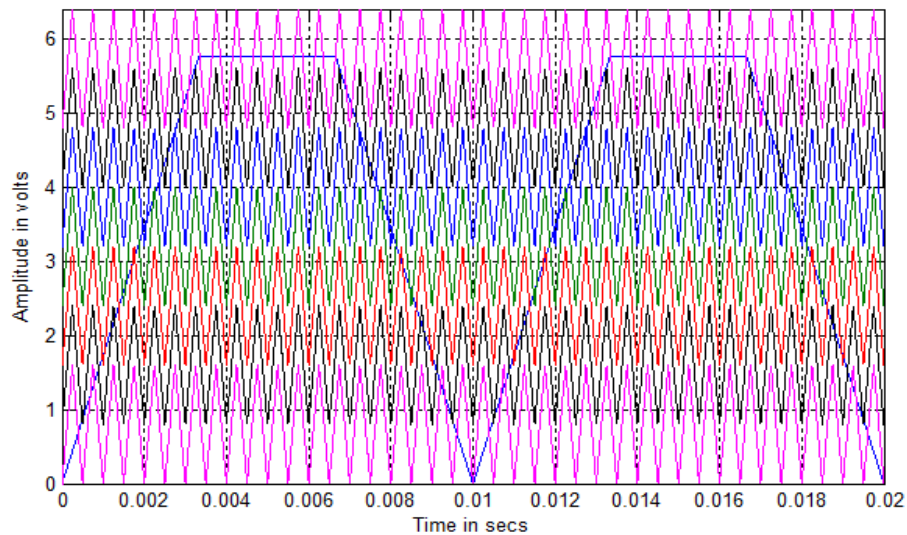


Fig. 7: Carrier arrangement for unipolar trapezoidal reference COPWM technique ($m_a = 0.9$, $m_f = 40$, $A_c = 1.6$ and $A_m = 6.4$)

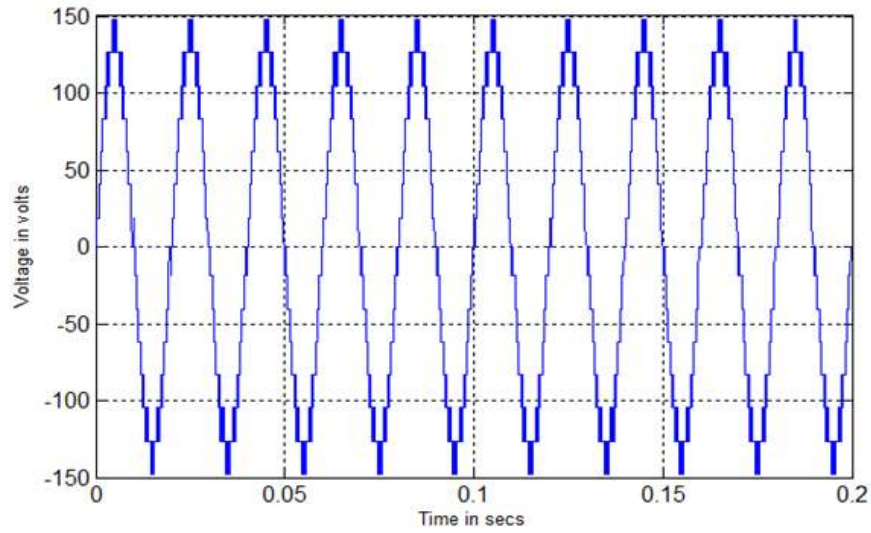


Fig. 8: Simulated fifteen level output voltage generated by unipolar sine reference with UPDPWM technique

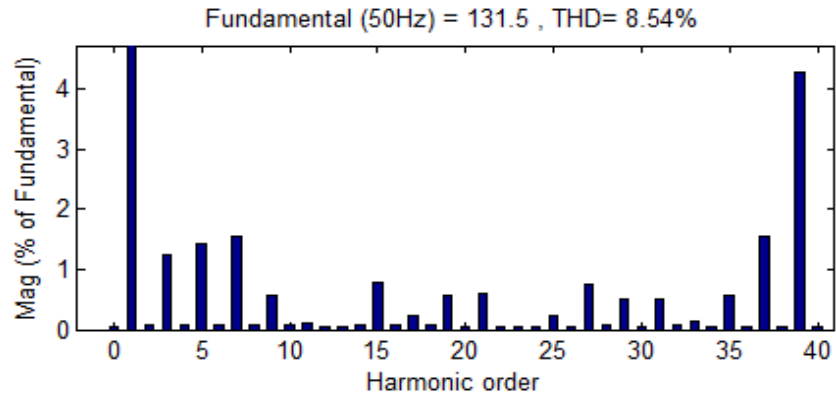


Fig. 9: FFT-harmonic spectrum of output of UPDPWM technique

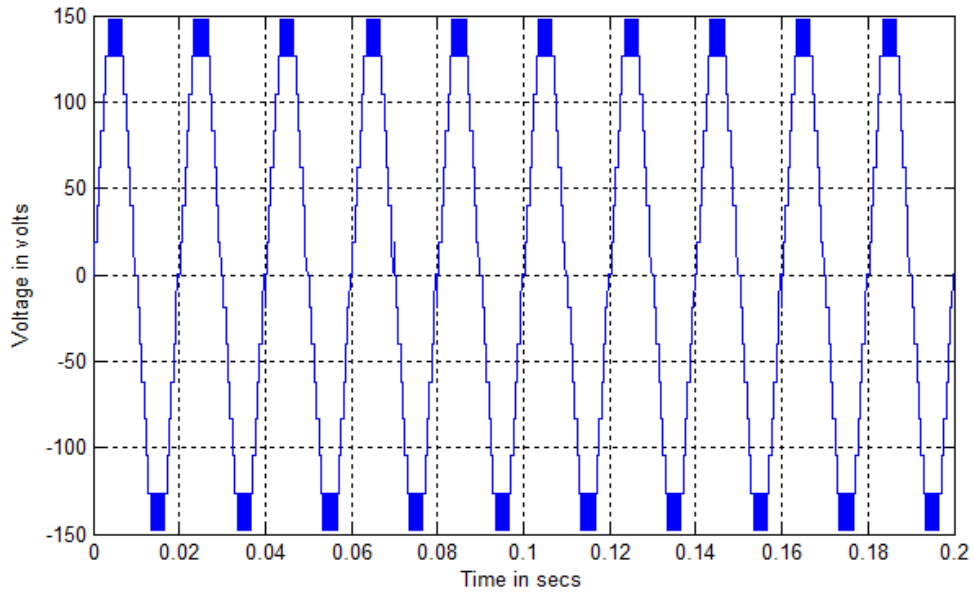


Fig. 10: Simulated fifteen level output voltage generated by unipolar trapezoidal reference with UPDPWM technique

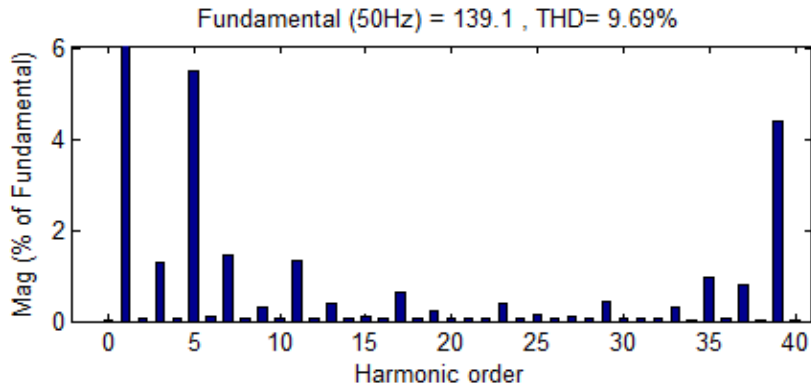


Fig. 11: FFT-harmonic spectrum of output of UPDPWM technique

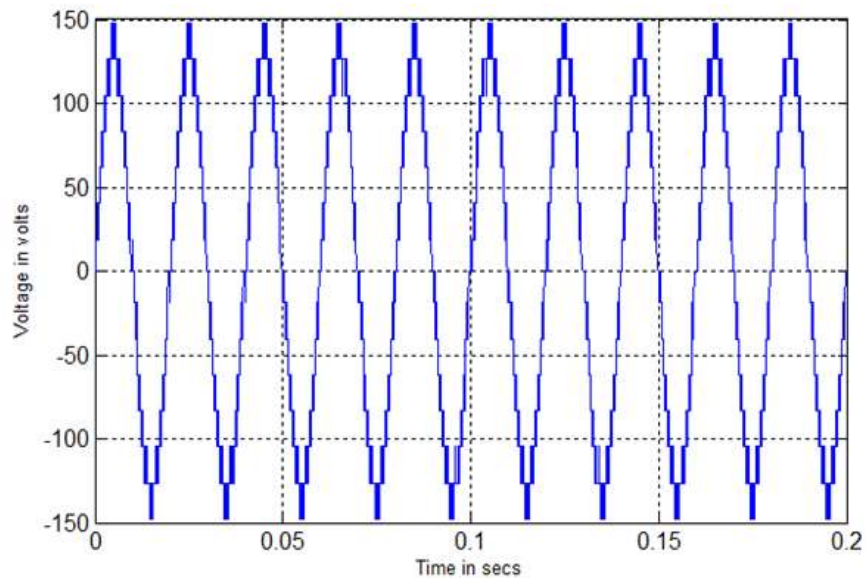


Fig. 12: Simulated fifteen level output voltage generated by unipolar sine reference with UAPODPWM technique

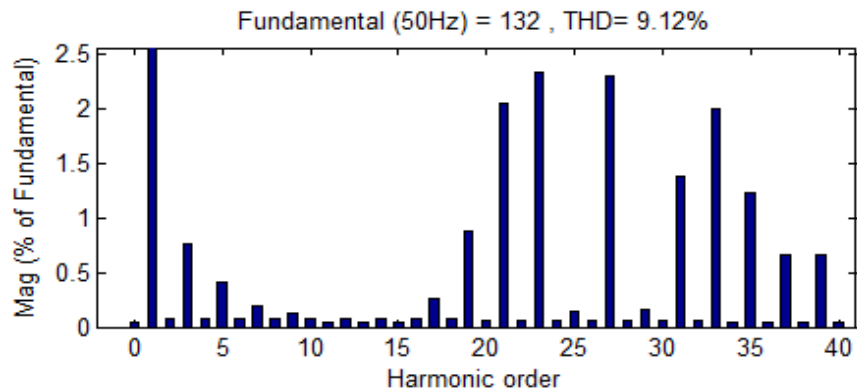


Fig. 13: FFT-harmonic spectrum of output of UAPODPWM technique

SIMULATION RESULTS

The Proposed 15 level inverter is modeled in SIMULINK using power system block set. Switching

signals are developed using various unipolar PWM techniques discussed previously. The simulation is carried out for a fundamental frequency of 50 Hz and a carrier frequency of 2000 Hz. Simulations are

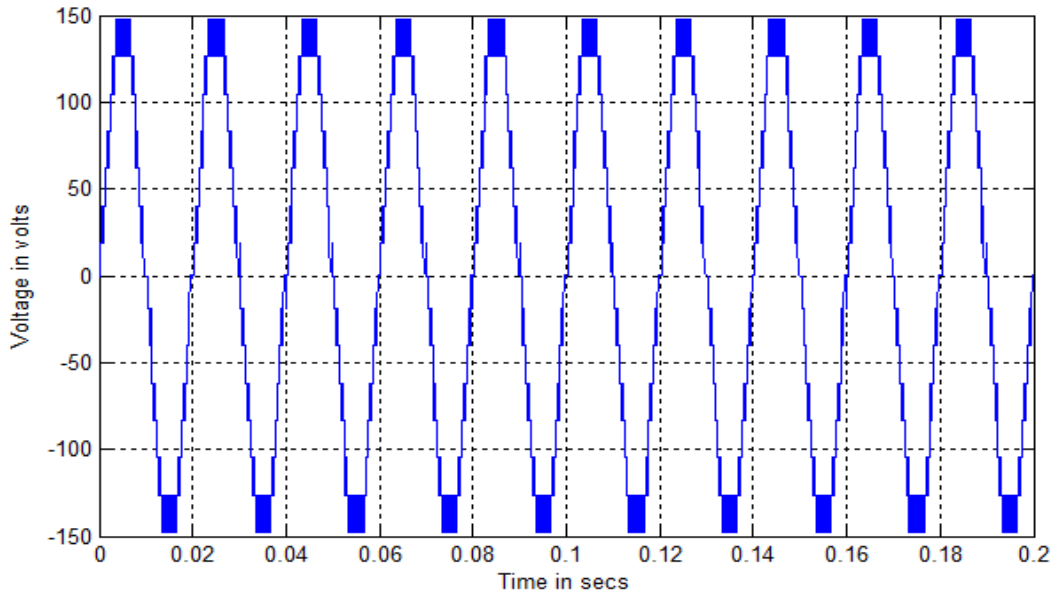


Fig. 14: Simulated fifteen level output voltage generated by unipolar trapezoidal reference with UAPODPWM technique

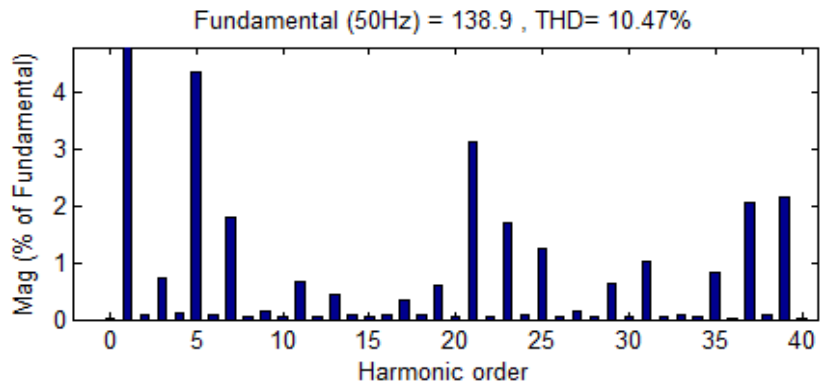


Fig. 15: FFT-harmonic spectrum of output of UAPODPWM technique

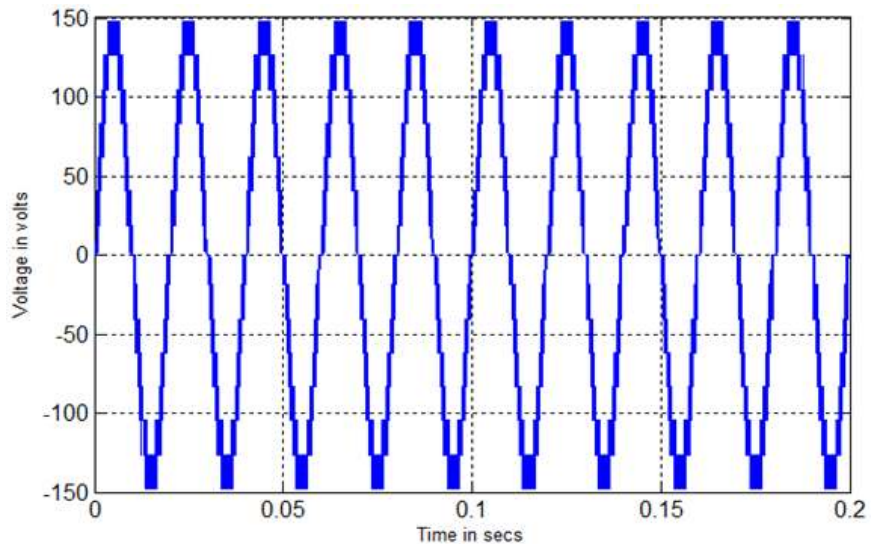


Fig. 16: Simulated fifteen level output voltage generated by unipolar sine reference with UCOPWM technique

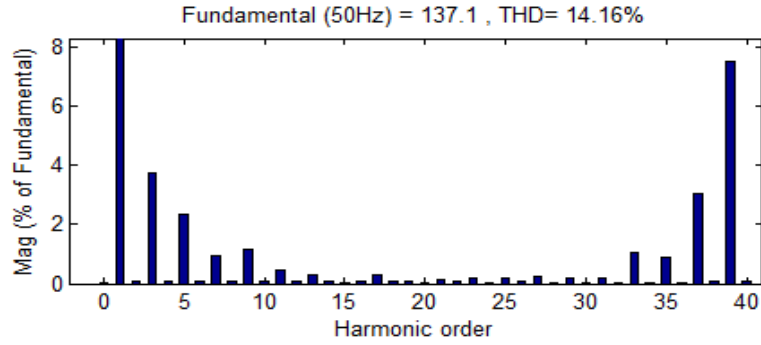


Fig. 17: FFT-harmonic spectrum of output of UCOPWM technique

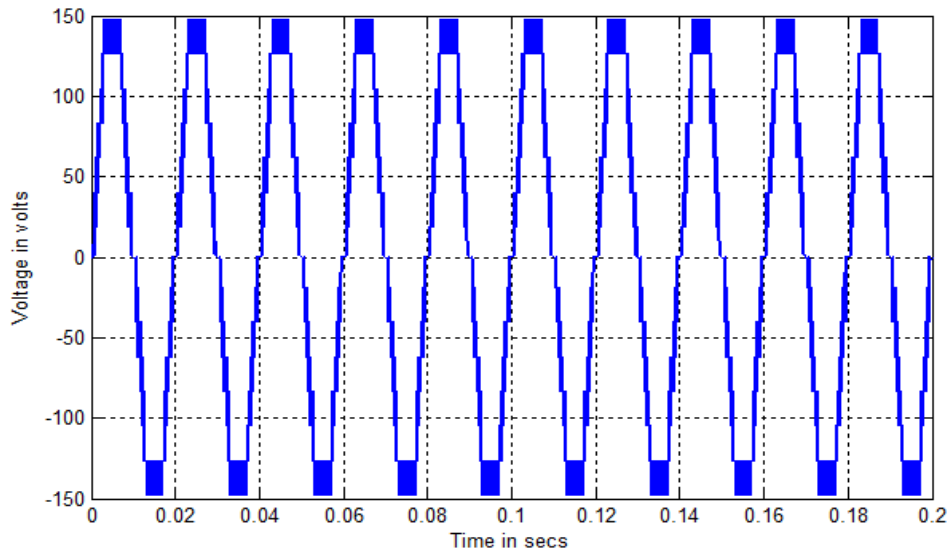


Fig. 18: Simulated fifteen level output voltage generated by unipolar trapezoidal reference with UCOPWM technique

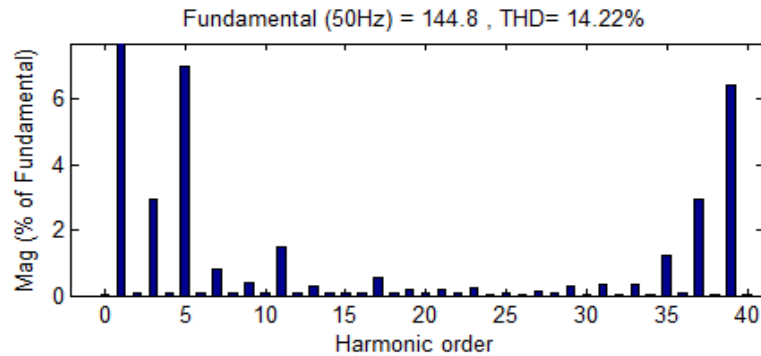


Fig. 19: FFT-harmonic spectrum of output of UCOPWM technique

performed for three different values of m_a (0.9, 0.95 and 1). Figure 8 to 19 shows the simulated output voltages and harmonic spectrum for only one sample value of m_a . Table 1 to 3 shows the various values of m_a ranging from 0.9-1 and corresponding THD% values and V_{RMS} of fundamental output voltage are measured using FFT block and the crest factor, form factor for the same modulation indices were calculated.

V_{RMS} output voltage of Trapezoidal reference with UCOPWM strategy is comparatively higher than the other PWM strategies. CF is relatively equal for all the strategies. From the FFT spectra it is observed that, no dominant harmonics were found in UPDPWM and UAPODPWM having Sine reference strategies and in UCOPWM the 3rd and 39th harmonic is comparatively more. The 5th and 39th harmonic is high in all the three

Table 1: THD % for different modulation indices

ma	UPDPWM		UAPODPWM		UCOPWM	
	Sine ref	Trap. ref	Sine ref	Trap. ref	Sine ref	Trap. ref
1.00	8.82	9.66	8.21	8.30	11.32	11.22
0.95	8.82	9.64	8.50	9.31	12.69	12.86
0.90	8.54	9.69	9.12	10.47	14.16	14.22

Table 2: VRMS (fundamental) for different modulation indices

ma	UPDPWM		UAPODPWM		UCOPWM	
	Sine ref	Trap. ref	Sine ref	Trap. ref	Sine ref	Trap. ref
1.00	103.50	109.10	103.90	109.50	106.50	110.4
0.95	98.16	102.40	98.60	103.90	102.10	106.6
0.90	92.99	98.32	93.32	98.24	96.96	102.4

Table 3: Crest factor for different modulation indices

ma	UPDPWM		UAPODPWM		UCOPWM	
	Sine ref	Trap. ref	Sine ref	Trap. ref	Sine Ref	Trap. ref
1.00	1.4138	1.4133	1.4144	1.4136	1.4140	1.4139
0.95	1.4137	1.4150	1.4140	1.4138	1.4142	1.4136
0.90	1.4144	1.4147	1.4141	1.4138	1.4139	1.4140

strategies having Trapezoidal reference. The following parameter values are used for simulation: $V_1 = 21.5$ V, $V_2 = 43$ V, $V_3 = 86$ V, $f_c = 2000$ Hz and R (load) = 100 ohms.

CONCLUSION

Single phase 15 level seven switch asymmetric inverter employing unipolar sinusoidal and trapezoidal reference modulation strategies have been investigated. It is found that unipolar sine reference with UPDPWM technique provides output with relatively low distortion. Fundamental RMS output voltage of unipolar trapezoidal reference with UCOPWM method is slightly higher than the other PWM methods. Appropriate PWM techniques may be employed depending on the performance index required in a chosen application of multilevel inverter. The proposed single phase 15 level asymmetric inverter enormously reduces the number of switches. Thus the switching losses, cost, low order harmonics and total harmonics distortion are effectively reduced.

REFERENCES

Babaei, E., 2008. A cascade multilevel converter topology with reduced number of switches. *IEEE T. Power Electron.*, 23(6): 2657-2664.

Babaei, E. and S.H. Hosseini, 2009. New cascaded multilevel inverter topology with minimum number of switches. *Elsevier J. Energy Conver. Manage.*, 55(11): 2761-2767.

Babaei, E., S.H. Hossein, G.B. Gharehpetian, M.T. Haque and M. Sabahi, 2007. Reduction of DC voltage sources and switches in asymmetrical multilevel converters using a novel topology. *Elsevier J. Electr. Power Syst. Res.*, 77(8): 1073-1085.

Banaei, M.R., E. Salary, R. Alizadeh and H. Khounjahan, 2012. Reduction of components in cascaded transformer multilevel inverter using two DC sources. *J. Elect. Eng. Technol.*, 7(4): 538-545.

Bensraj, R. and S.P. Natarajan, 2010. Multicarrier trapezoidal PWM strategies for a single phase five level cascaded inverter. *J. Eng. Sci. Technol.*, 5(4): 400-411.

Bensraj, R., S.P. Natrajan and B. Shanthi, 2010. Unipolar PWM using trapezoidal amalgamated rectangular function for improved performance of multilevel inverter. *Int. J. Comput. Appl.*, 7(13): 19-24.

Ceglia, G., V. Guzman, C. Sanchez, F. Ibanez, J. Walter and M.I. Gimanez, 2006. A new simplified multilevel inverter topology for DC-AC conversion. *IEEE T. Power Electron.*, 21(5): 1311-1319.

Malinowski, M., K. Gopakumar, J. Rodriguez and M.A. Perez, 2010. A survey on cascaded multilevel inverters. *IEEE T. Ind. Electron.*, 57(7): 2197-2206.

McGrath, B.P. and D.G. Holmes, 2002. Multicarrier PWM strategies for multilevel inverters. *IEEE T. Ind. Electron.*, 49(4): 858-867.

Murugesan, M., K. Ramani and S. Thangavel, 2011. A hybrid multilevel inverter with reduced number of switches for induction motor drive. *African J. Sci. Res.*, 4(1): 220-234.

Murugesan, M., R. Sakthivel, E. Muthukumaran and R. Sivakumar, 2012. Sinusoidal PWM based modified cascaded multilevel inverter. *Int. J. Computat. Eng. Res.*, 2(2): 529-539.

Urmila, B. and D. Subbarayudu, 2010. Multilevel inverters: A comparative study of pulse width modulation techniques. *J. Sci. Eng. Res.*, 1(13): 1-5.