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Research Article

Ultra Low Power, High Performance Negative Edge Triggered ECRL Energy Recovery Sequential Elements with Power Clock Gating

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Abstract: Flip flops form an indispensable building block in the design of digital systems. In this study, adiabatic switching technique is used in the design of low-power negative edge triggered energy recovery flip-flops. In particular, the negative edge triggered D, SR and JK flip-flop designs based on the Quasi-adiabatic ECRL (Efficient Charge Recovery Logic) architecture are proposed. The projected design is illustrated with an 8 bit Serial Input and Parallel Output shift register (SIPO). The setup time and hold time are minimal in negative edge triggering compared to the pulsed and positive edge triggering which contributes to the high performance and the signal integrity of the design. Additionally, glitching is avoided due to the edge triggering which in turn reduces the soft error rate in the flip-flops. The simulation results have shown improvements in power efficiency by 95 and 75%, respectively for the D flip-flop and 8 bit shift registers than their CMOS counter parts. Due to its several merits, this design can find many real time applications such as digital communication (cryptography), memories and shift registers in microcontrollers. The four phase power clocks are utilized in the pipelining of the stages of the shift register, which mitigates all the relevant timing problems addressed in the literature of flip flops. For simulation, SPICE EDA simulation environment using the 350 nm process technology library from Austria micro systems have been used.

Keywords: 8-bit SIPO register, D flip-flop, efficient charge recovery logic, JK flip-flop, negative edge triggered flip-flops, SR flip-flop

INTRODUCTION

With the rapid growth of CMOS technology, the density and complexity of the integrated circuit increases. This aggravates the power dissipation problem and temperature control becomes difficult thus enhancing the cooling costs. Moreover, the need for reliable, low cost, high performance portable devices adds power as one of the design metrics. The conventional approaches to achieve low power design are to reduce:

- The supply voltage
- The capacitance of the gate
- Loading capacitance of the gate
- The switching activity

One of the promising techniques in the design of low power digital circuits is to apply the concept of adiabatic switching or energy recovery. Energy recovery principle achieves low energy dissipation by recycling the energy through the use of an AC type (oscillating) power supply voltage (Hamid *et al*., 2009). In this method, the supply clock is a trapezoidal signal that pumps energy to the circuit during the first phase and retrieves the energy during the third phase.

This study identifies the following problems and the solutions:

- Major portion of total power in highly synchronous systems is dissipated in the clock network. Hence, energy recovery clocking is a much needed low power solution.
- In adiabatic or energy recovery logic, the clock generator circuit continuously provides clock signal. Generally, a clock system may be driving sequential elements like flip-flops and latches (Cooke *et al*., 2003). As the clock travels utmost distances, the design of power and performance efficient sequential elements with adequate concern on the clock skew and clock jitter is also necessary.
- Power gating can also be made at the clock nodes for reducing the clock switching power dissipation during the idle mode of the circuits.
- Both positive and negative edge triggered flip-flops are required in the sequential circuit. However, there are no negative edge triggered energy recovery flip-flops in the literature so far.

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Several adiabatic logic architectures have been reported in the literature. Most of these adiabatic logic families use either diodes for pre charge (Dickinson and Denker, 1995; Lau and Liu, 1997), or a Pair of Cross-Coupled PMOS transistors for both pre charge and evaluation (Moon and Jeong, 1996; Peiyi *et al*., 2011). These circuits overcome the CV^2f barrier posed by the conventional CMOS logic and achieve extremely low power consumption. This study presents the ECRL (Efficient Charge Recovery Logic), a promising architecture for low power design of the negative edge triggered energy recovery flip-flops. Further, four phase clocking used for pipelining in the stages of the ECRL architecture improves the performance also.

MATERIALS AND METHODS

Structure for the ECRL circuit: The ECRL circuits use a differential signaling scheme so that an inverter can also be used as a buffer. The supply clocks comprises of 4 operational phases. The 1st phase of ECRL circuit is the Evaluation, during which the input values are sampled and the output nodes are charged or discharged depending on the inputs. The sampled input values are held/stored during the Hold phase for the next stage and the stored charge is recovered during the Recovery phase.

The input signal can be changed during the Wait phase. The PMOS transistors are cross-coupled and are used for pre-charge and evaluation (Fig. 1a). The NMOS transistors, however, are used to tie one of the differential output nodes to ground, when the inputs are in the hold phase. Four power clocks are used for the cascading stages in sequence. Here, the power clocks are represented by trapezoidal waveforms (Fig. 1b). Although the ECRL is an adiabatic logic style, a small fraction of non-adiabatic energy dissipation still exists. Hence it is said to be belonging to 'quasi-adiabatic' logic family. When *in* = 1 during the evaluate phase of the clock cycle, *outb* is tied to ground (as the power clock Pclk ramps from 0 to *Vdd*). When *Pclk* reaches $|Vtp|$, (where *Vtp* is the threshold voltage of the PMOS transistor), P2 turns on and the load capacitance at the output node (out) will begin to charge up to logic '1'. This causes an initial, non-adiabatic dissipation of approximately 1/2 $C_L Vtp2$ where C_L is the load capacitance at the output nodes (Ng *et al*., 2000).

During the recovery phase, as the voltage of the power clock Pclk approaches $|V_{tp}|$, the PMOS transistor P_2 gets turned off and the recovery path to the power clock is disconnected. The charge left on the load capacitance at the end of the recovery phase will either leak away slowly through the turned-off devices, or discharge through N2, if *inb* changes value (from '0' to '1') for the next logic evaluation. Thus, the non-adiabatic dissipation during the recovery phase, (less than or equal to ½ $C_L V^2_{tp}$) is inevitable. However, it can be minimized as discussed below. As the PMOS

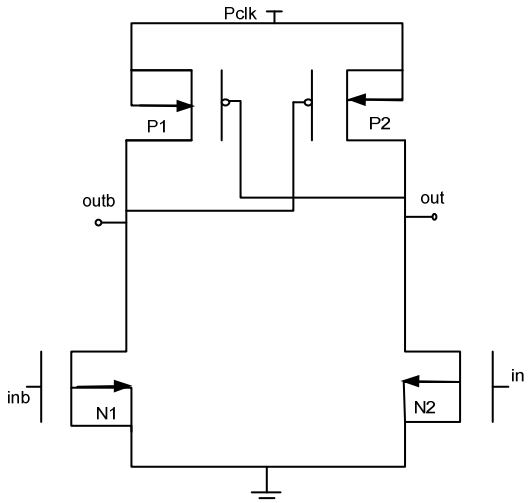


Fig. 1a: An ECRL inverter/buffer

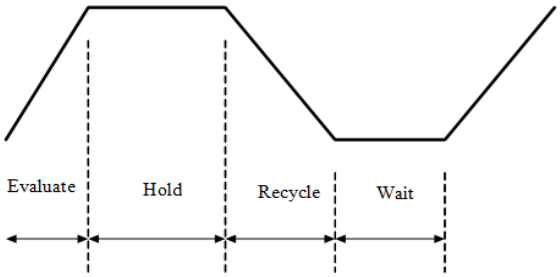


Fig. 1b: Power clock waveform

body is connected to the Pclk instead of a *DC* power line, better recovery is achieved through the parasitic diodes formed between the source/drain and the body of the PMOS transistors as shown in Fig. 1a. By doing so, the output voltage can be further recovered to *Vd* (0.5V), the forward voltage drop across the diode, even if the PMOS transistor is already switched off when *Pclk* decreases below V_{TP} during the recovery phase. This improves the energy recovery process and realizes a substantial improvement in terms of power dissipation.

However, this method only applies during the recovery phase, as the diodes are reverse biased during the pre-charge/evaluate phase. Subsequently, the proposed circuit designs of *D*, *SR*, *JK* flip flops and the 8 bit serial input parallel output shift register are designed using the modified ECRL structure The use of four clocks enables each of the cascaded stages to be simultaneously active during the same clock cycle. This pipelining greatly enhances the performance of the design. Furthermore, the several pulsed flip-flops in the literature are found to have less setup time but have many drawbacks like larger hold time and hence larger Clk-Q delay. On the other hand, the proposed edge triggered flip-flops have lesser setup time, lesser hold time and hence less Clk-Q delay overcoming all the

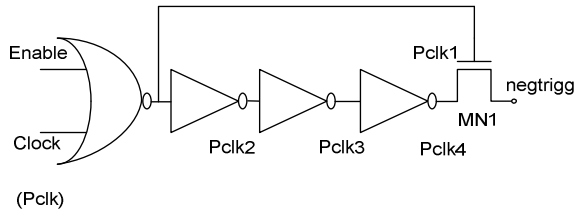


Fig. 2a: Negative trigger generator with clock gating

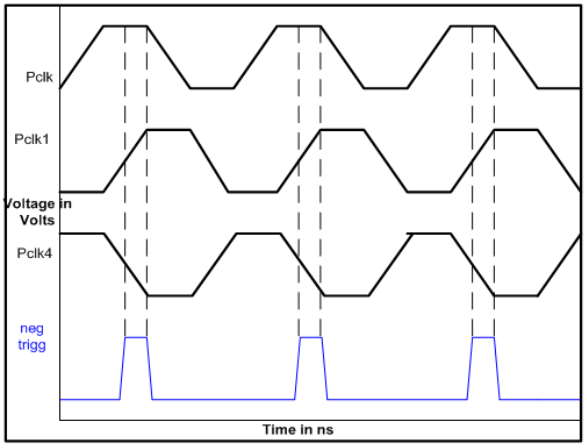


Fig. 2b: Waveforms of the trigger generator

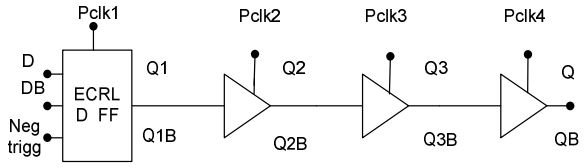


Fig. 2c: Cascaded blocks of ECRL negative edge triggered D flip-flop and buffers

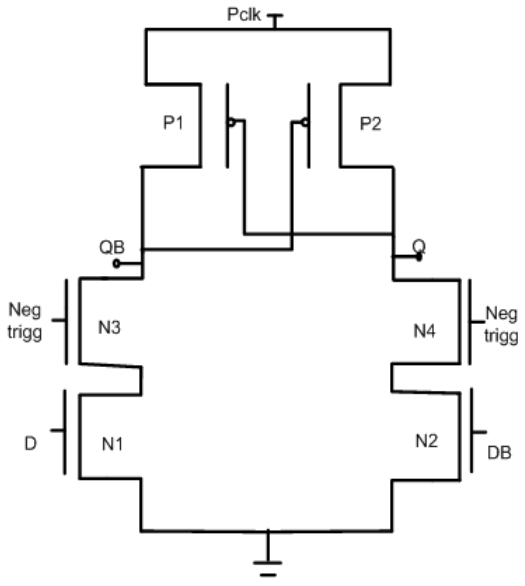


Fig. 2d: ECRL negative edge triggered D flip-flop

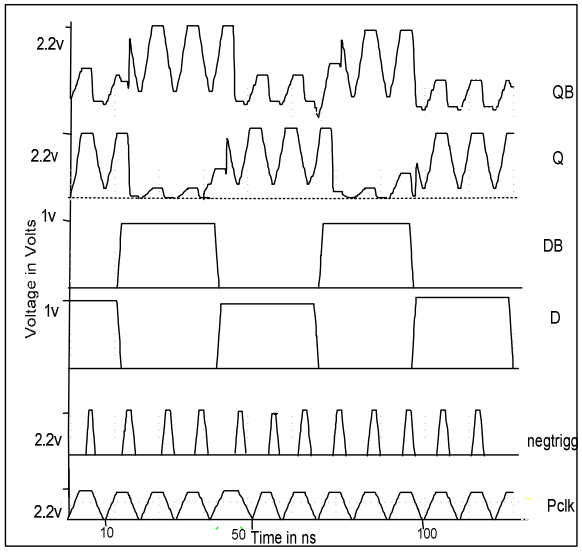
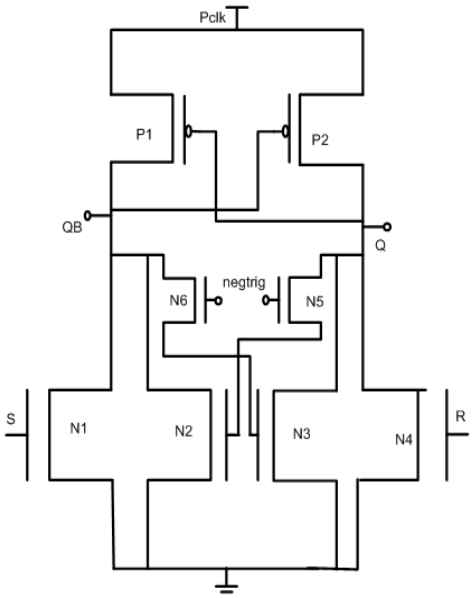


Fig. 2e: Simulated waveforms of Fig. 2d

demerits of pulsed flip-flops. And it is worth mentioning that glitches which may occur due to cosmic strikes are nullified in edge triggered devices which in turn also minimizes the soft error rate in registers and flip-flops.

Circuit designs:

Negative trigger generator with clock gating: In this study, negative edge triggering is supported. Thus as explained in the previous section, the data will generally be read in the evaluate phase of the PCLK in the adiabatic circuits. However in the proposed design, a negative edge trigger (negtrigg) signal is generated at the fall time of the PCLK only and hence input data will be read (at the rising edge of the trigger) and the recovery happens at the fall time of the trigger. The reason for choosing negative edge triggering is that the setup time and hold time is less than that of the positive edge triggering. Thus the overall Clk-Q delay is very less and hence improved performance. And also, to reduce the dissipation occurring in the clock network, a NOR clock gating is introduced. In Fig. 2a, there are a series of inverters with the first inverting done by a NOR gate. This NOR gate does the clock gating by separating the data and clock parts of the circuit. The inputs to the NOR gate are the enable *EN* and the clock signal Pclk. When the *EN* is high, the clock is prevented from reaching the output (i.e., the negtrigg signal is not present). When *EN* is low, the clock reaches the output. (i.e., there is a negative edge triggered signal, negtrigg). This enable signal EN is made low only when the data is arriving. This brings about great improvement in the clock power dissipation. The ANDing of *Pclk*1 and *Pclk*4 by the pass transistor MN1 generates the negative trigger signal (negtrigg). Further the need for multiple clock generators or the area overhead for multi phase



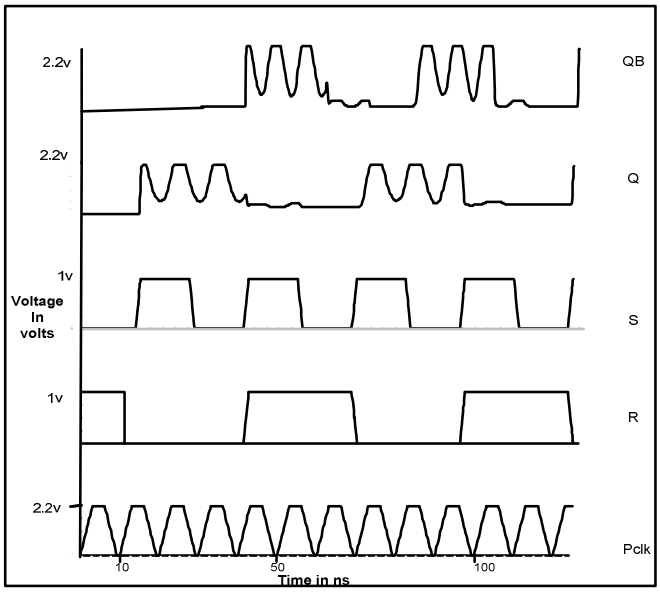


Fig. 3a: ECRL negative edge triggered SR flip-flop

Fig. 3b: Simulated waveforms of Fig. 3a

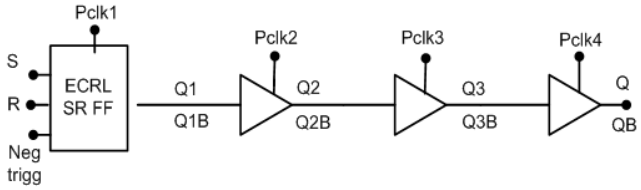


Fig. 3c: Cascaded blocks of ECRL negative edge triggered SR flip-flop and buffers

clock generation is overcome due to the use of the pulse generation circuitry shown in Fig. 2a and b, which by itself generates the four phase signal. The transient waveforms in Fig. 2b precisely explain the generation of the negative trigger signal (negtrigg). This negtrigg signal is used in the proposed flip-flops. Figure 2c shows the cascaded blocks of ECRL negative edge triggered D fip-flop and buffers

Proposed D flip-flop: The proposed *D* ECRL flip-flop and the simulated transient waveforms are as shown in Fig. 2d and e. Besides the PMOS loads (*P*1, *P*2) there are four NMOS pull down transistors (*N*1-*N*4). During the evaluate phase, when $D = 1$ and the negtrigg is high, node *QB* becomes low. This will turn P2 '*on'* and we have *Pclk* (high) in the *Q* output. The output is held during the hold phase. The energy delivered during the evaluate phase is recovered during the recovery phase by the discharging current through *P*1. When $D = 0$ and the negtrigg is high, node *Q* takes low value and this will turn *P*1 '*on'* and we have *Pclk* in the *QB* output and the energy is recovered during the recovery phase. Such a flip flop can be cascaded with four stages of buffers operating with the four phases of clock *Pclk*1, *Pclk*2, *Pclk*3 and *Pclk*4, respectively.

Proposed SR flip-flop: The proposed SR ECRL flip-flop and the simulated transient waveforms are as shown in Fig. 3a and b. Besides the PMOS loads (*P*1, *P*2) and the NMOS pull down transistors (*N*1-*N*4), there are two other NMOS transistors (*N*5, *N*6) along the feedback paths of the outputs Q and QB, respectively. The gates of *N*5 and *N*6 are connected to negtrigg. During the pre-charge/evaluate phase, if the output node *Q* swings 0 to *Pclk* (representing a logic '1'), the gate capacitance of *N*2 will be charged to turn *N*2 on. At the same time, *N*3 will be turned off since its gate is connected to *QB* (which is at logic '0') via *N*6. On the next clock cycle, if $S = 1$ and $R = 0$, or $S = R = 0$ (SET), *QB* will still be at 0 V by *N*1 or *N*2, while *Q* is at logic '1'. However, if $S = 0$ and $R = 1$ (RESET), *Q* will be held at 0 V and the gate capacitance of *N*2 will be discharged to 0V. With *N*1 and *N*2 turned off, QB will be charged up to Pclk by P2. The ECRL D, SR, JK negative edge triggered flip-flops can be cascaded as shown in Fig. 3c by three inverters driven by four different clocks *Pclk*1, *Pclk*2, *Pclk*3 and *Pclk*4, respectively. The outputs are *Q*1 (*Q*1*B*), *Q*2 (*Q*2*B*), *Q*3 (*Q*3*B*) and *Q*4 (*Q*4*B*). The inverters provide the delay needed by the consequent stages to be driven at the four phases of the clock.

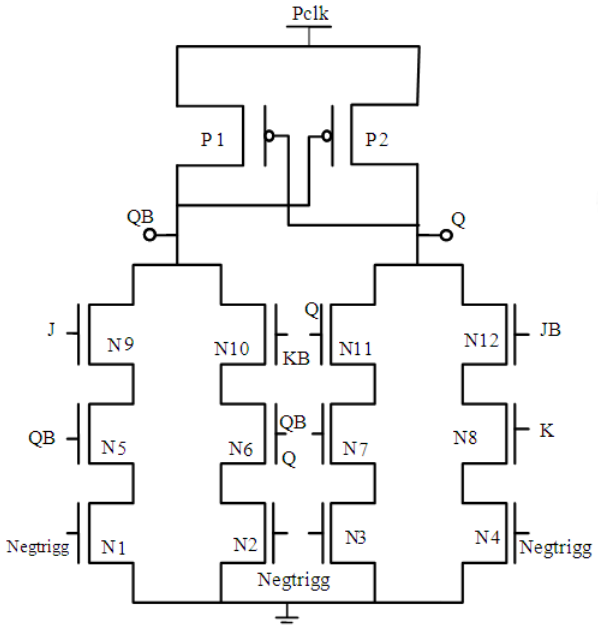


Fig. 4a: ECRL negative edge triggered JK flip-flop

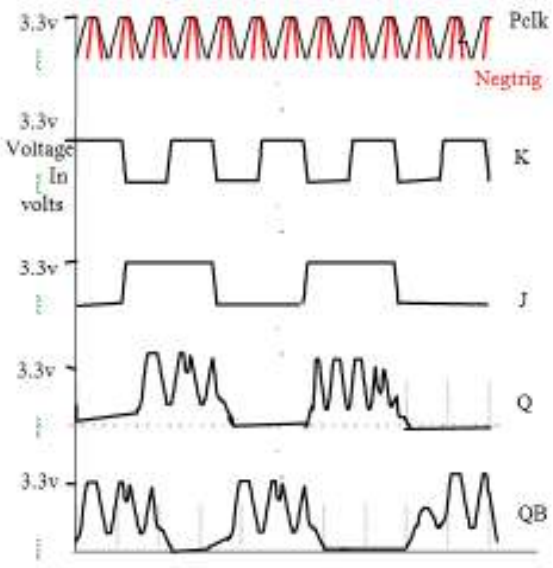


Fig. 4b: Simulated waveforms of Fig. 4a

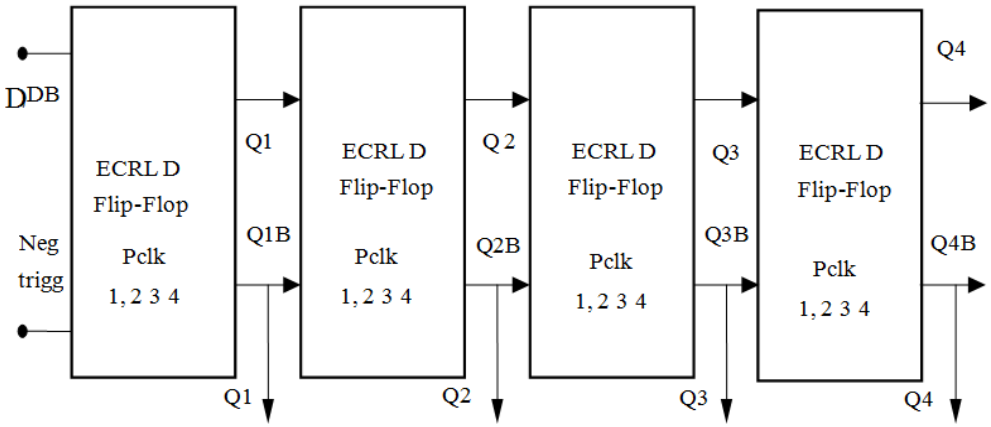


Fig. 4c: ECRL negative edge triggered 4 bit shift register

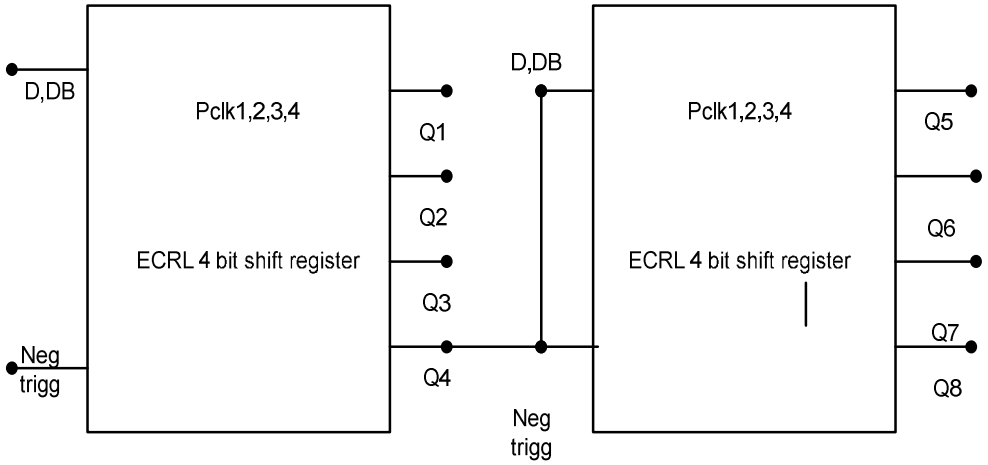


Fig. 4d: ECRL negative triggered 8 bit shift registers

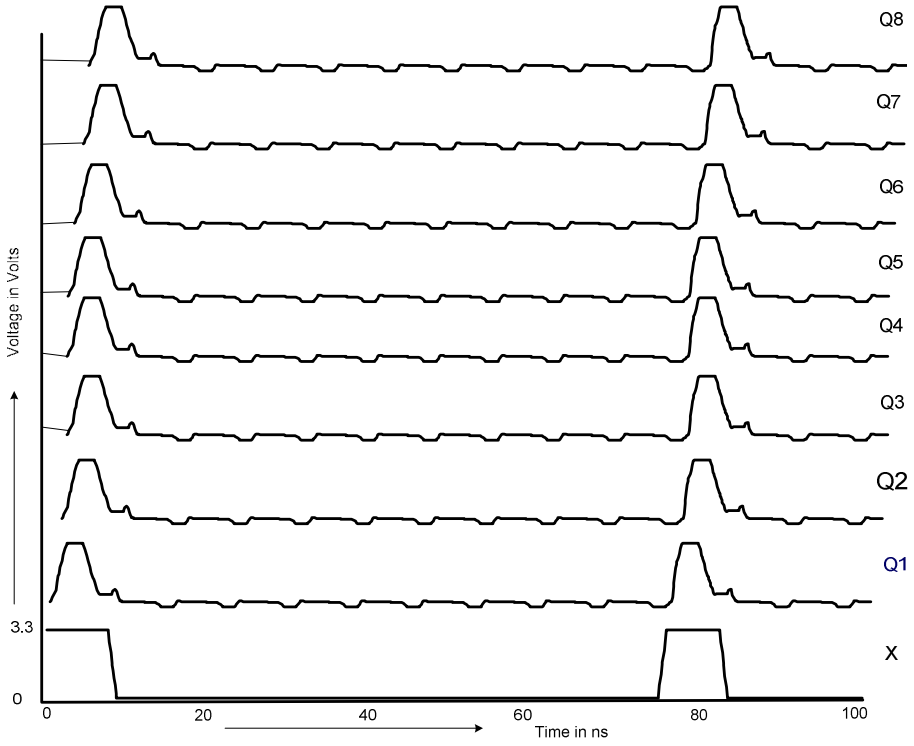


Fig. 4e: Simulation waveforms of 8 bit shift register

Proposed JK flip-flop: The proposed ECRL *JK* flip-flop is designed as shown in Fig. 4a. The simulated waveforms are as shown in Fig. 4b. It consists of a basic *JK* flip-flop cell. The NMOS evaluation trees (*N*1-*N*12) in the basic cell represent the true and complementary logics of the *JK* flip-flop. During the pre-charge/evaluate phase, if the output node *Q* swings from 0 to *Pclk* (representing a *logic*1), *QB* pulls to logic '*0*' through (*N*2-*N*6-*N*10). During the next clock cycle, when *J* = 1and *K* = 0 the outputs *Q* and *QB* is at *logic*1 and *logic* 0 respectively. When *J* = 0 and *K* = 1, the outputs *Q* and *QB* become *logic*0 and *logic*1, respectively.

Negative edge triggered Serial Input Parallel Output register (SIPO): The ECRL negative edge triggered *D* flip-flops are cascaded to form a 4 bit shift register as shown in Fig. 4c. The data is sampled during the negative trigger and the four outputs *Q*1, *Q*2, *Q*3 and *Q*4 are obtained. Such a 4 bit shift register is cascaded to form an 8 bit shift register as in Fig. 4d, whose simulation transients are as shown in Fig. 4e. The *Q4* output is fed to the negtrigg input of the second shift register. Hence it gets activated only after the arrival of the *Q4* output. So both the shift registers are given the same supply clocks for the consecutive stages. The active edge of the clock is very less in the negtrigg any glitching and the associated degraded performance and dissipation are avoided. Thus, this SIPO (Serial Input Parallel Output register) is found to have improvements in the power and performance than the CMOS counterparts.

RESULTS AND DISCUSSION

The circuits are designed based on the Austria micro systems 350 nm process CMOS technology and are simulated using SPICE tool. Four-phase sinusoidal power clocks with peak-to-peak voltage of 3.3 V are used to power up the ECRL circuits. A clock frequency of 125 *MHZ* is used. Simulated results of the *D* flip flop, *SR* flip-flop, the *JK* flip-flop at 125 *MHz* power clock frequency are shown in the tabulation. Furthermore, the designs are also simulated for the frequencies 20, 40, 50, 90, 100 *MHz*, respectively and the results were analyzed for optimum performance. The power reduction achieved by the ECRL-based negative edge triggered D flip-flop, ranges to 96% at 125 *MHz* compared to its CMOS counterpart as depicted in Fig. 5a. The power delay product has also been found to insist the tradeoff between the power and delay as depicted in Fig. 5b. The comparison of the flip-flops is shown in the Fig. 5c which illustrates the major three design metrics of the IC design. Besides, the other parameters determining the functionality, performance and area are also tabulated in Table 1 and compared for all the designed flip-flops. The energy dissipation of the designs at light and medium load are also evaluated. The power delay product calculated serves as the figure of merit to compare all the designs.

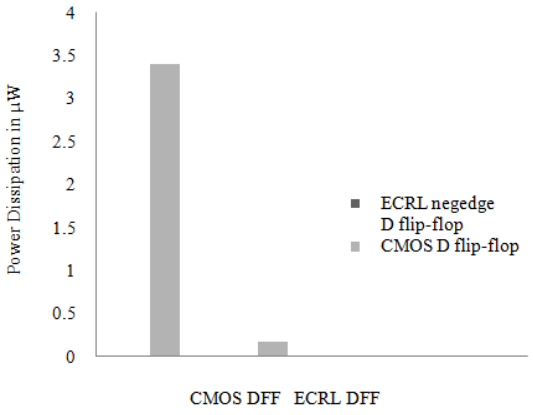


Fig. 5a: Power comparison of the ECRL negative edge triggered flip-flops with its CMOS counterparts

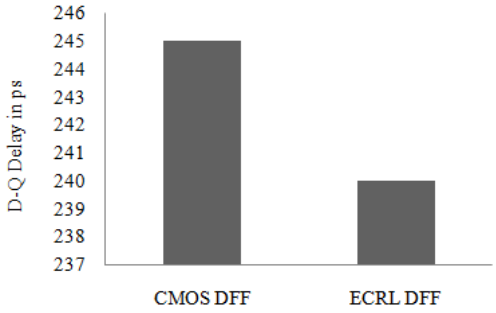


Fig. 5b: Comparison of the D-delay of the ECRL negative edge triggered flip-flops with its CMOS counterparts

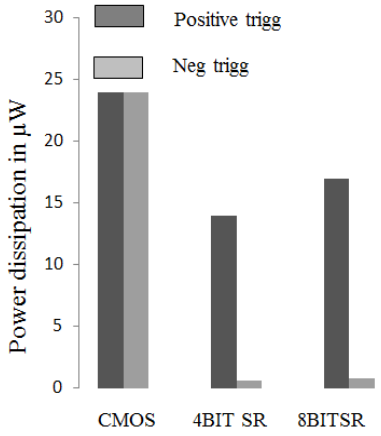


Fig. 5c: Comparison of ECRL 4 and 8 bit shift register

Table 1: Simulation results of the ECRL negative edge triggered flip-flops

Parameter	ECRL D-FF	ECRLSR-FF	ECRL JK-FF
Supply voltage	3.300	3.30	3.3
Frequency in MHz	125	125	125
No of transistors	6	8	10
Total width µm	4.900	6.30	9.2
Power dissipation µW	3.400	3.60	10
Delay in ps	240	240	340
Power delay product	0.816	0.82	3.4

To evaluate the performance of the proposed flip-flops, CMOS transmission gate based flip-flops powered at 3.3 V_{DC} supply are also designed and simulated. The pulsed flip-flops, namely, CDMFF, SDFF (Athas *et al*., 1994), use less number of clocked transistors for power improvement and incur lesser setup time. And, it has large hold time, thus increasing the total propagation delay. However, the proposed design of flip-flops, whose setup time is the rise time of the 'negtrigg' signal is extremely minimum (t setup = 490 ps) and the hold time is also less, of the order of t_h = 500 ps. The *CLK* to *Q* delay was found to be 240 ps (for f = 125 MHz) when simulated in the 350 nm technology. The above results clearly signify the performance enhancement of the proposed design, inn comparison against those published in the literature. Further, a 4-bit shift register implemented with the proposed *D* flip-flop shows a power dissipation of 84 µW showing 75% power efficiency (Fig. 5c).

CONCLUSION

This study presented the performance and power improvement of the quasi adiabatic sequential structures. Negative edge triggering realizes additional merits of reduced clock skew and jitter, when compared against the positive triggered and the pulsed flip-flops. This study presented a negative edge triggered ECRL energy recovery *D*, *SR*, *JK* flip-flops. From the simulations, these flip-flops have shown significant improvement in terms of power consumption and D-Q delay compared to the CMOS based flip-flops. The simulation results precisely shows that the proposed design of D flip flop is highly power efficient with an energy dissipation of 12.75 fJ for a load of C_L = 150 fF. Further, it is proved that the SR flip-flop is dissipating energy of 13.5 fJ for the same load. The design is validated through 4-bit and 8-bit shift register constructed with the proposed D flip-flop. Hence, the ECRL based negative edge triggered flip-flops can be used as building blocks in the design of adiabatic/energy recovery systems both in terms of power and delay.

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