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Research Article

Modified Embedded Switched Inductor Z Source Inverter

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Abstract: A novel modified embedded switched inductor Z-source inverter is proposed by inserting the photovoltaic panels at various locations to improve the output voltage boosting performance. The proposed inverter have the concepts of embedded and switched inductor Z source network to have better features in terms of increased voltage boost inversion ability, continuous input current, reduced voltage stress on the switches/capacitors. Simulations are carried out by employing (120°) pulse width modulation scheme. Hardware implementation of the proposed topology of rating 150 W, 60 V is made and the results are experimentally verified. Switch device power and reliability evaluation of the proposed inverter are also calculated.

Keywords: Embedded network, reliability evaluation, switched inductor network, Z-Source Inverter (ZSI)

INTRODUCTION

Ever increasing energy consumption, cost of fossil fuels, soaring costs and exhaustible nature and worsening global environment have created a booming interest in renewable energy generation systems, one of which is photovoltaic. Such a system generates electricity by converting Sun's energy directly into electricity. Photovoltaic generated energy can be delivered to power system networks through grid connected inverters. Z source inverters are recent find in inverter topologies mostly used for photovoltaic applications because they have many advantages like better voltage boost and improved reliability than the other traditional voltage and current type inverters (Peng, 2003; Saravanan *et al*., 2011). Voltage type Z source inverters are classified based on number and location of input dc sources, Z networks and switching devices as reported in (Loh *et al*., 2010; Li *et al*., 2013).

Various Z source inverter topologies and its variants are reported in the literature focusing on renewable energy and adjustable speed drive applications (Loh *et al*., 2005; Saravanan *et al*., 2012a, b). Various Pulse Width Modulation (PWM) strategies employed in these topologies are discussed in Loh *et al*. (2005) and Ellabban *et al*. (2009).

The work reported in this study have the combined features of embedded ZSI (Loh *et al*., 2010) and Switched inductor Z Source Inverter (SLZSI) (Zhu *et al*., 2010) to provide better voltage boosting ability with smoother output voltage waveforms at reduced voltage stress on the capacitors. In addition, the proposed inverter avoids the start up inrush current that could destroy the devices and thereby inverter's reliability is improved.

A two level embedded Z source inverter (Loh *et al*., 2010) shown in Fig. 1, has dc sources embedded within X shaped LC impedance network. Here, even if one of the sources fails to feed power to the inverter at times of interruptions or fault conditions, continuous operation is possible by feeding power from the other source.

Switched inductor Z Source Inverter (SLZSI) (Zhu *et al*., 2010) shown in Fig. 2 has high voltage conversion ratios with a very short shoot through state. It consists of four inductors (L_1, L_2, L_3 and L_4), two capacitors (C_1 and C_2) and seven diodes (D, D_1, D_2, D_3, D_4, D_5 and D_6). The combinations of L_1-L_3-D_1-D_3-D_5 and L_2-L_4-D_2-D_4-D_6 act as the switched inductor cells.

Despite this increase in boost inversion, SLZSI has significant drawback namely current drawn from the source is discontinuous in nature. A decoupling capacitor bank at the front end is used to avoid the current discontinuity and protect the source. In addition, SLZSI cannot suppress the startup inrush current resulting in voltage and current spikes which can destroy the devices connected to it.

To overcome these problems, modified embedded switched inductor Z-source inverter topology is proposed in this study which has the concepts of embedded and switched inductor topologies to have better features, like:

- Input current is continuous
- It provides inrush current suppression at start up
- Capacitor stress voltage is reduced

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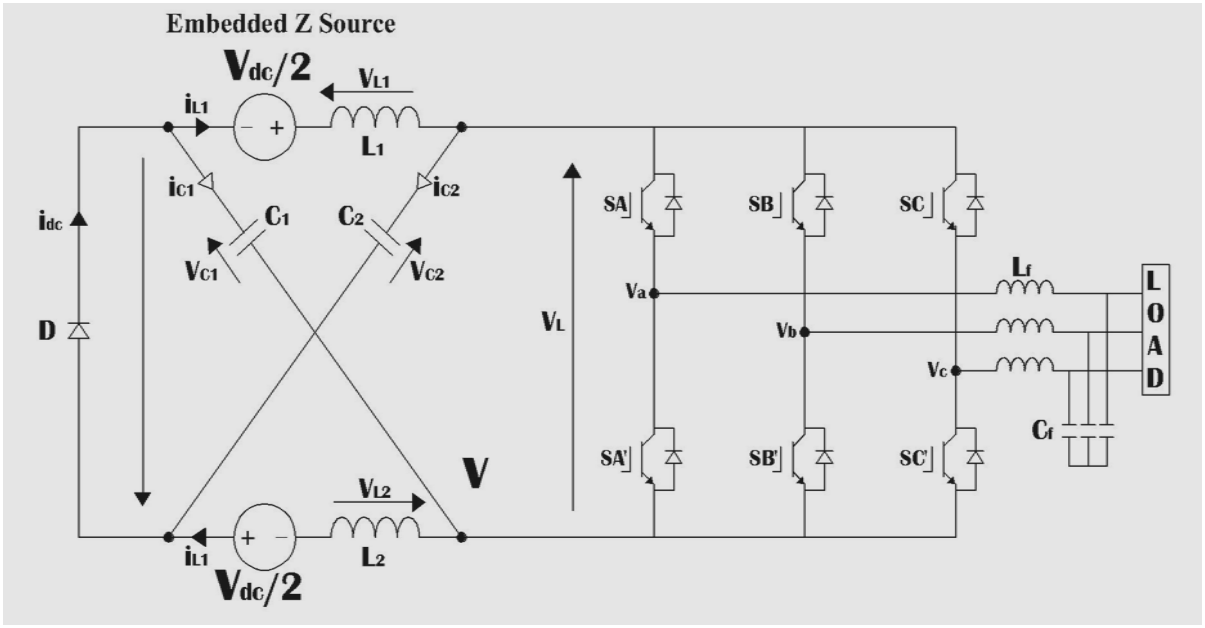

Fig. 1: Two level embedded Z source inverter

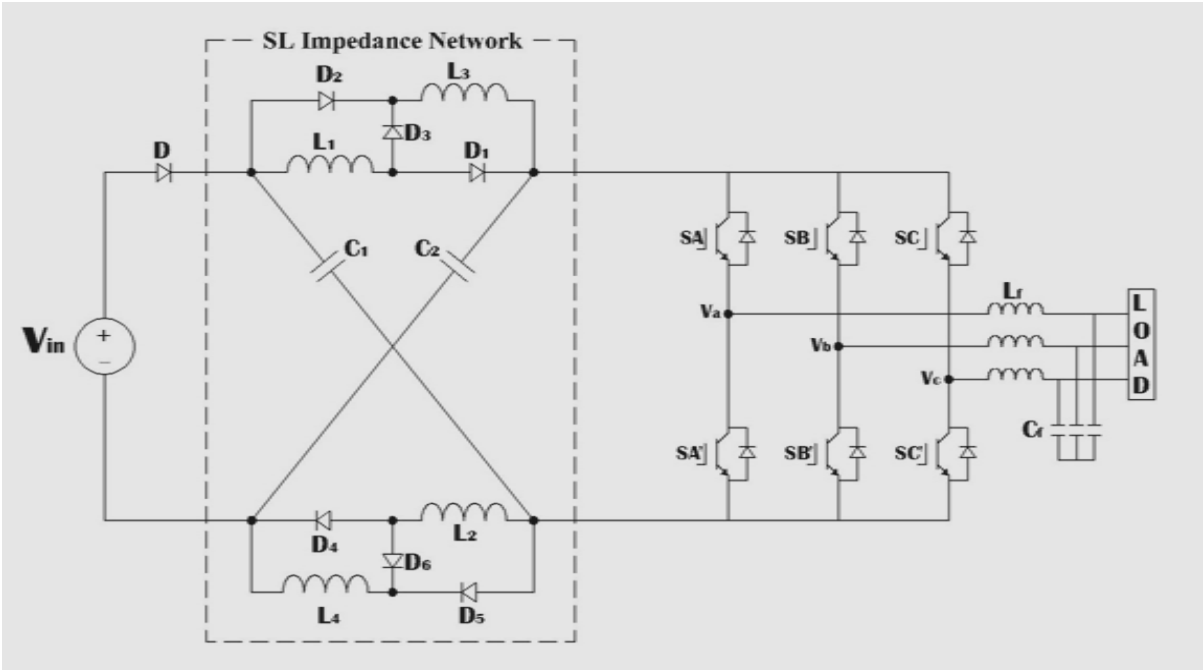

Fig. 2: Switched inductor Z source inverter

Modified embedded switched inductor Z-source inverter is obtained by inserting split dc sources into the switched-inductor cells. Multiple PV panels now need not be series-connected at one location, but can be divided into isolated strings, hence minimizing series output reduction caused by shading.

The aim of this study is to propose a modified embedded switched inductor Z-source inverter to provide high voltage boost inversion ability, lower voltage stress across the active switching devices, continuous input current and reduced voltage stress on the capacitors. Simulation and experiments are carried out to validate the proposed topology.

PROPOSED INVERTER TOPOLOGY AND ITS CONTROL SCHEME

Topology description: Figure 3 shows the circuit of proposed modified embedded switched inductor Z-source inverter topology (MESL Z-source inverter). A

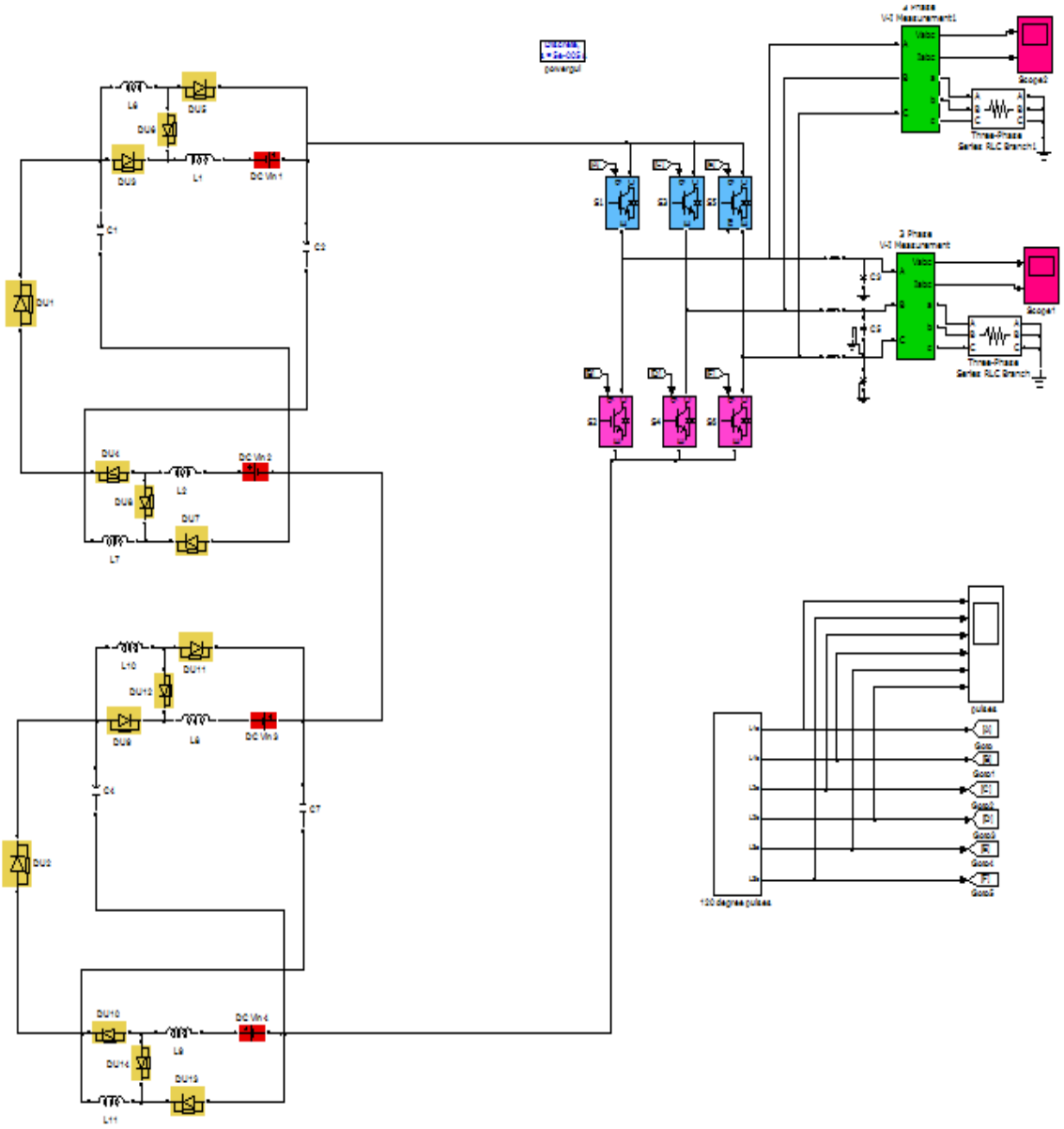

Fig. 3: Proposed modified embedded switched inductor Z-source inverter

successful combination of embedded Z-source inverter, switched-inductor structure and cascaded connection makes the modified embedded switched-inductor Z-source inverter to provide a high step-up inversion that increases its boost capability.

The proposed inverter topology is built by inserting dc sources into the X-shaped impedance network. Since the dc sources are connected directly to the impedance network's inductors, boosted dc current flows through the inverter smoothly. The modified inverter provides a continuous input current without adding an input passive filter and also exhibits a lower voltage stress on the capacitors with improved reliability.

The MESLZSI topology consist of four inductors and two capacitors for each cell, (L_1, L_2, L_3 and L_4) and (C_1, C_2) for first cell and (L_5, L_6, L_7, L_8) and (C_1, C_4) for second cell and seven diodes (D_{in}, D_1, D_2, D_3, D_4, D_5, D_6, D_7, D_8, D_9, D_{10}, D_{11}, D_{12}, D_{13} and D_{14}). The combinations of L_1-L_3-D_1-D_3-D_5 and L_2-L_4-D_2-D_4-D_6 act as the switched-inductor cells in a single cell.

For the purpose of analysis, operating states of MESLZSI are simplified into shoot through and non shoot through states. In non shoot through states, the proposed inverter has six active states and two zero states in the inverter main circuit. During non shoot through state, in first cell D_1, D_4 and D_7 are ON, whereas D_2, D_3, D_5 and D_6 are OFF. Inductors (L_1 - L_4) and (L_5 - L_8) are connected in series in this state. Capacitors C_1 and C_2 are charged, whereas the inductors L_1, L_2, L_3 and L_4 transfer energy from dc

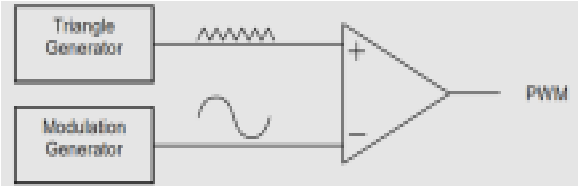

Fig. 4: PWM signal generating unit

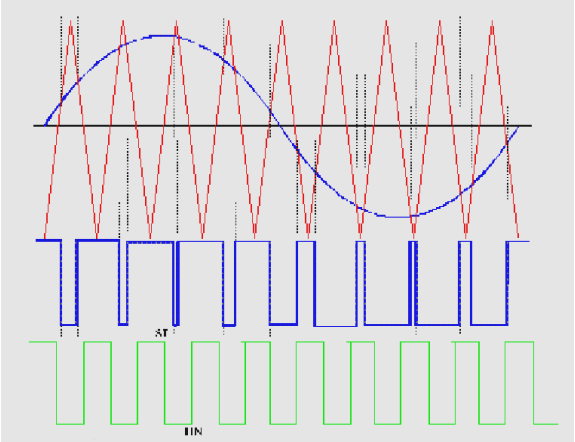

Fig. 5: Obtained PWM switching signals

voltage sources to the main circuit. The corresponding voltages across L_1, L_2, L_3 and L_4 in this state are V_{L1_non}, V_{L2_non}, V_{L3_non} and V_{L4_non}, respectively. In second cell D_8, D_{11} and D_{14} are ON, whereas D_9, D_{10}, D_{12} and D_{13} are OFF. (L_5, L_7) and (L_6, L_8) are connected in series. Capacitors C_1 and C_2 are charged, whereas the inductors L_5, L_6, L_7 and L_8 transfer energy from the dc voltage sources to the main circuit. The corresponding In shoot through state:

$$v_{L1} = V_{C1} + V_{dc} \quad (7)$$

$$v_{L2} = V_{C2} + V_{dc2} \quad (8)$$

$$v_{L3} = V_{C1} \quad (9)$$

$$v_{L4} = V_{C2} \quad (10)$$

$$i_{C1} = -2I_{L3},\ i_{C2} = -2I_{L2}$$

$$i_{in1} = I_{L3}\ i_{in2} = I_{L2}$$

$$v_{L5} = V_{C3} + V_{dc3} \quad (11)$$

$$v_{L6} = V_{C4} + V_{dc4} \quad (12)$$

$$v_{L7} = V_{C3} \quad (13)$$

$$v_{L8} = V_{C4} \quad (14)$$

$$i_{C3} = -2I_{L7},\ i_{C4} = -2I_{L6}$$

voltages across L_5, L_6, L_7 and L_8 in this state are V_{L5_non}, V_{L6_non}, V_{L7_non} and V_{L8_non}, respectively.

In the shoot through states, the inverter side is shorted by both the upper and lower switching devices in the phase legs. During the shoot through state, in first cell D_1, D_4 and D_7 are off, whereas D_2, D_3, D_5 and D_6 are ON. (L_1, L_3) and (L_2, L_4) are connected in parallel. Capacitors C_1, C_2, C_3 and C_4 are discharged, whereas inductors L_1, L_2, L_3, L_4, L_5, L_6, L_7 and L_8 store energy. In second cell D_8, D_{11} and D_{14} are off, whereas D_9, D_{10}, D_{12} and D_{13} are on. (L_5, L_7) and (L_6, L_8) are connected in parallel; Capacitors C_1, C_2, C_3 and C_4 are discharged, whereas inductors L_1, L_2, L_3, L_4, L_5, L_6, L_7 and L_8 store energy. The circuit analysis for the proposed inverter based on the shoot through and non shoot through states are described below:

In non shoot through state:

$$v_{L1} + v_{L3} = V_{dc1} - V_{C2} \quad (1)$$

$$v_{L2} + v_{L4} = V_{dc2} - V_{C1} \quad (2)$$

$$V_{PN} = V_{C1} + V_{C2} \quad (3)$$

$$i_{C1} = I_{L2} - i_{i1};\ i_{C2} = I_{L1} - i_{i1} \quad i_{in1} = I_{L1};\ i_{in2} = I_{L2}$$

$$v_{L5} + v_{L7} = V_{dc3} - V_{C4} \quad (4)$$

$$v_{L6} + v_{L8} = V_{dc4} - V_{C3} \quad (5)$$

$$V_{PN} = V_{C3} + V_{C4} \quad (6)$$

$$i_{C3} = I_{L4} - i_{i2}\ i_{C4} = I_{L3} - i_{i2} \quad i_{in3} = I_{L3}\ i_{in4} = I_{L4}$$

Control scheme employed: As discussed earlier, any modulation method (Loh *et al*., 2005; Ellabban *et al*., 2009) can be adopted to control the proposed MESLZSI. Figure 4 depicts the pictorial representation of 120° mode of conduction of PWM generator. Here the triangular signal is carrier or switching signal of the inverter, whose switching frequency employed ranges from 10-20 kHz. The modulation generator produces a sine wave signal that determines the pulse width and therefore the RMS voltage output of the inverter. For PWM signal generation, it requires both reference and carrier signals that feed into a comparator which creates output signals based on the difference between the signals. Obtained PWM switching signals are shown in Fig. 5. The proposed inverter consist of six switches named as S_1, S_2, S_3, S_4, S_5, S_6 each device conduct for 120° phase shift. Sequence of firing is in the order 61, 12, 23, 34, 45, 56, 61 and the gating signals are shifted from each other by 60°.

Switching device power calculation: The Switching Device Power (SDP) is expressed as the product of

voltage stress and current stress. The total SDP of an inverter system is defined as the aggregate of SDP of all switching devices used in the circuit (Miaosen and Alan, 2007b; Miaosen *et al*., 2007a). Total SDP is a measure of the total semiconductor device requirement, thus an important cost indicator of an inverter system:

$$\text{Total average SDP} = (\text{SDP})\,av = \sum_{M=1}^{N} Vm\ \text{Im\_avg} \quad (15)$$

$$\text{Total peak SDP} = (\text{SDP})\,pk = \sum_{M=1}^{N} Vm\ \text{Im\_peak} \quad (16)$$

where,

Im_avg, Im_peak = The average and peak currents through the device respectively

Vm = The peak voltage induced on the devices

The average and peak SDPs of proposed inverter can be calculated for the given typical values {P_o = 150 W, M = 1, Cos ø = 1} as:

$$(\text{SDP})\,av = (2Po\,(2 - \sqrt{3}M) / (\sqrt{3}M - 1)) + (4\sqrt{3}Po/\cos ø\,\pi)) \quad (17)$$

$$(\text{SDP})\,av = 0.109\ \text{KVA}$$

$$(\text{SDP})\,pk = \max (4Po/ (\sqrt{3}M - 1)) + (4Po/\cos øM), (8Po/\cos ø\ M)) \quad (18)$$

$$(\text{SDP})\,pk = 1.2\ \text{KVA}$$

Reliability evaluation: Reliability analysis of the proposed inverter can be found out in terms of mean time to failure.

IGBT Reliability (ƛp) is expressed (Xue *et al*., 2012) as:

$$ƛp,_{IGBT} = ƛ_b\,\pi_T\,\pi_A\,\pi_R\,\pi_S\,\pi_Q\,\pi_E\ \text{failure}/10^6\ \text{h} \quad (19)$$

The typical values for the proposed inverter are listed as: base failure rate, ƛb = 0.00074; junction temperature factor, π_T = 5.9; application factor, π_A = 0.7; power rating factor, $\pi_{R,} = P^{0.37}$; voltage stress factor, π_S = 1, quality factor, π_Q = 2.4, environment factor, π_E = 6.0:

$$ƛp,_{IGBT} = 0.00074*5.9*0.7*35.08*1*0.7*6.0 = 0.45028\ \text{failure}/10^6\ \text{h}$$

Using 6 IGBT's in the proposed inverter, the reliability can be calculated as:

$$ƛp,_{inv} = 6*0.4502\ \text{failure}/10^6\ \text{h} = 2.70172\ \text{failure}/10^6\ \text{h}$$

Mean Time to Failure (MTTF) for the system use in full life period is expressed as inverse of failure rate and, calculated as:

$$\text{MTTF} = 1/\lambda = 1/2.7017\ \text{failure}/10\text{^}6\ \text{h} = 10^6/\ 2.7017\ \text{h} = 37, 01, 373\ \text{h} = 60.36\ \text{years}$$

Thus the reliability (estimated life) of the proposed inverter is theoretically calculated to be 60.36 years.

SIMULATION RESULTS

To verify the operation of proposed inverter, simulations are performed in MATLAB/SIMULINK environment, where the solver is chosen as variable step discrete with step of 1.0 µs with following PV system input voltages of values: V_1, V_2, V_3 = 12 V and V_4 = 24 V, collectively, V_{dc} = 60 V; L_1 to L_8 = 2 mH C_1, - C_4 = 10 µF and switching frequency, f_s = 20 kHz employing 120° switching scheme with a modulation index of value one. The output ac voltage waveforms (peak value) obtained through simulation for the proposed inverter are around 100 V in all the phases A, B and C, respectively which are observed with LC filter as shown in Fig. 6 and 7 shows the switching sequence of the switches S_1 to S_6. Table 1 provides a list of simulation parameters for the proposed inverter.

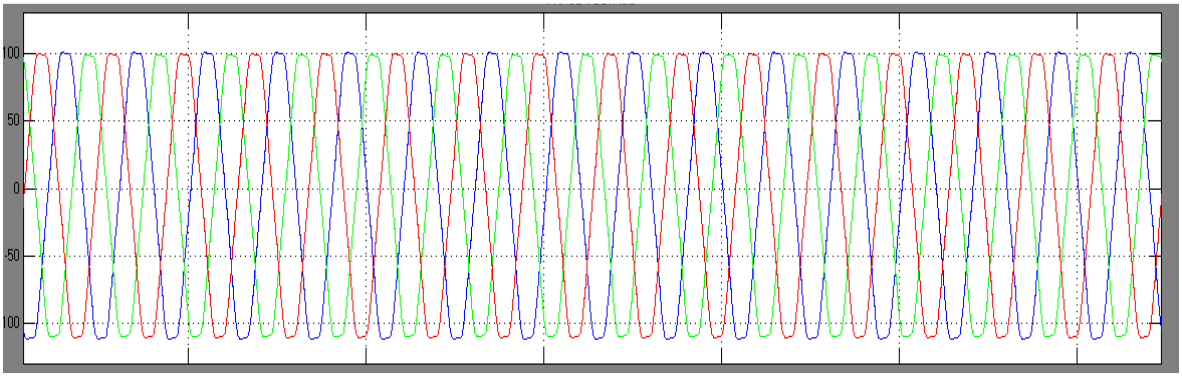

Fig. 6: Simulated output voltage waveforms of proposed inverter observed with LC filter (Scale: Y axis: 50 V/div)

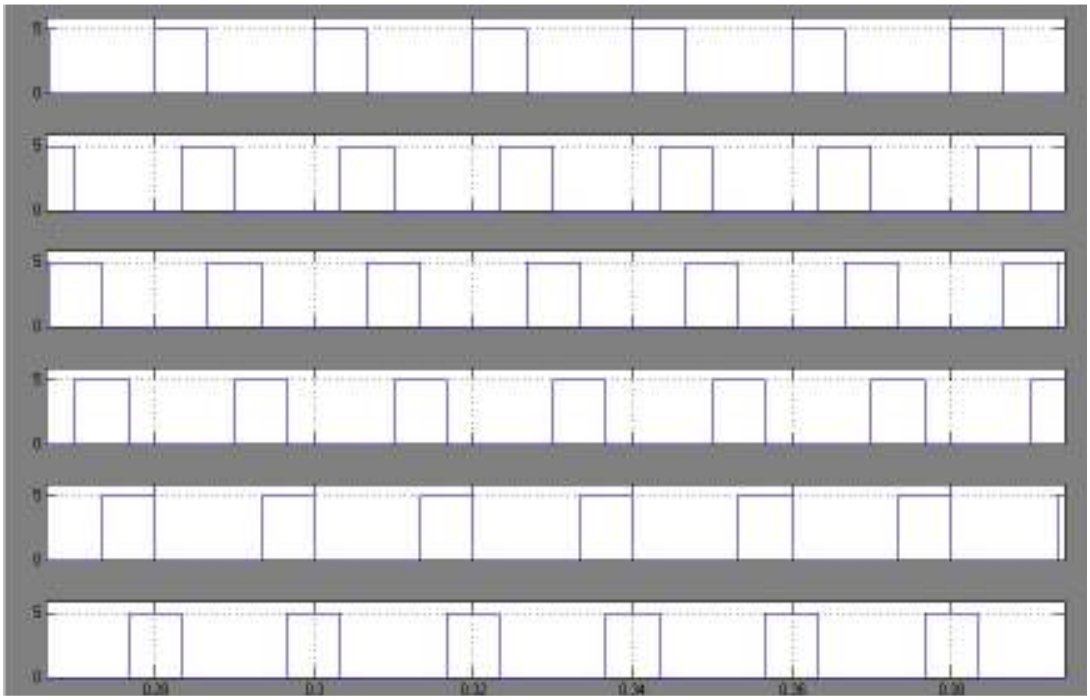

Fig. 7: Switching sequence of the proposed inverter (S_1 to S_6)

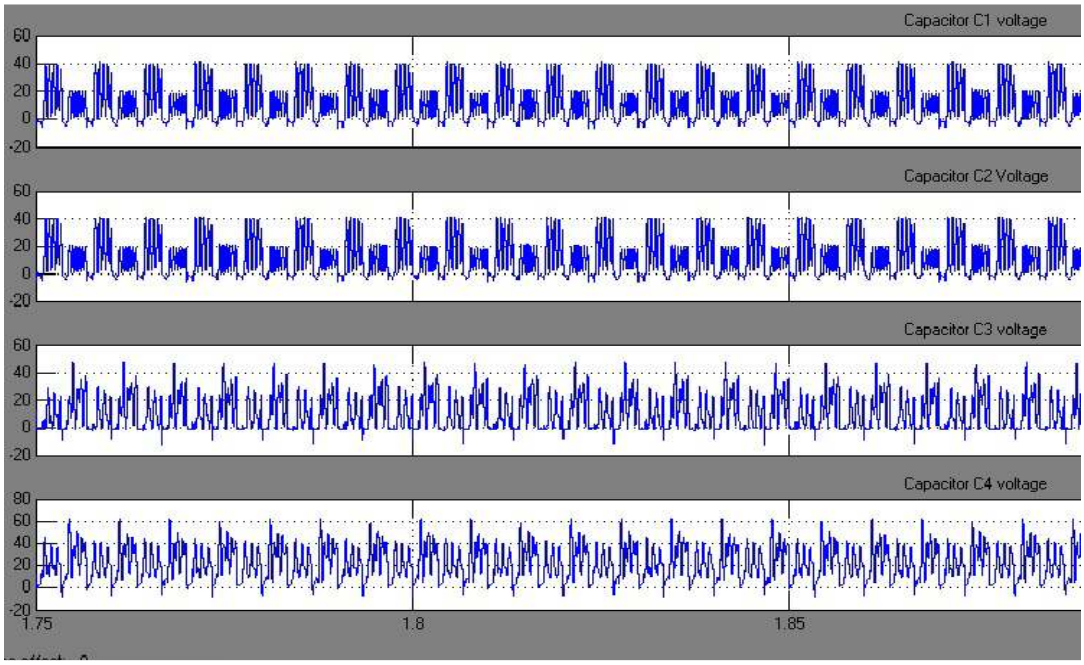

Fig. 8: Simulated capacitor waveforms (C_1 to C_4) (capacitor voltage values are given in the text)

Table 1: Simulation parameters of the proposed modified embedded switched inductor ZSI

Input DC voltage		60 V
Z-source network	L_1-L_8	2 mH
	C_1-C_4	10 µF
Switching frequency, f_s		20 kHz
Three phase output filter	L_f	10 mH
	C_f	2000 µF
Three phase resistive load, R_L	10 Ω/phase	10 Ω/phase

Figure 8 shows the capacitor voltage waveforms connected to the inverter having the values as 32.66V in the capacitors V_{C1} and V_{C2}, where V_{C3} and V_{C4} have 21.93 V and 18.43 V respectively. The obtained value shows that the internal capacitors C_3 and C_4 are under reduced stress condition, which is the notable feature of this proposed topology. Figure 9 shows the inductor current waveforms of values I_{L1} = 3.245 A, I_{L2} = 3.252

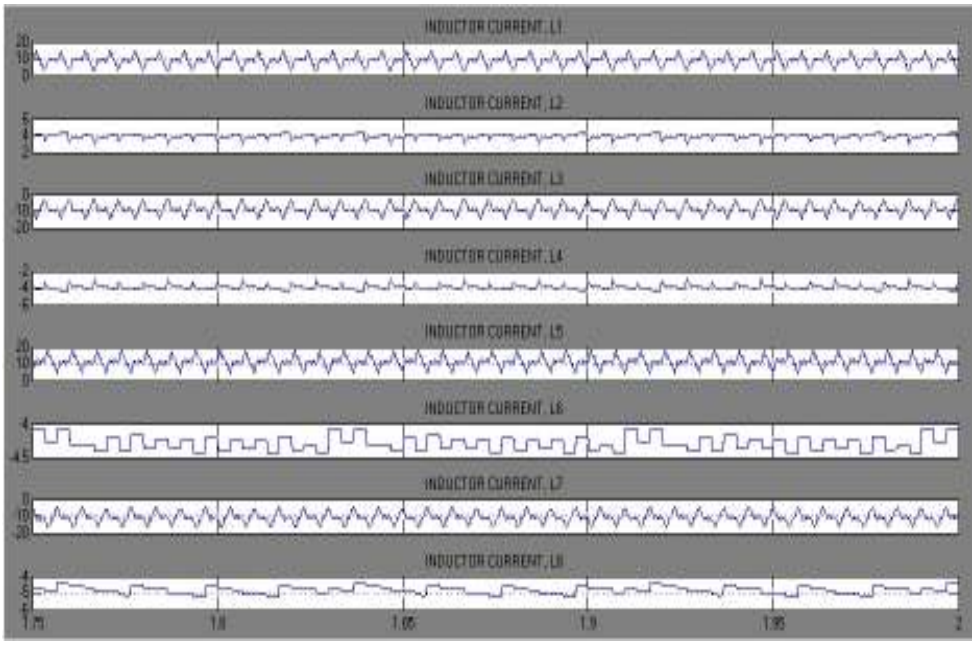

Fig. 9: Simulated inductor current waveforms (I_{L1} to I_{L8}) (inductor current values are given in the text)

Fig. 10: Experimental setup of the system

A, I_{L3} = -3.245 A, I_{L4} = -3.252 A, I_{L5} = 10.4 A, I_{L6} = -4.056 A, I_{L7} = 10.84 A, I_{L8} = -4.438 A.

Experimental results: Simulation results are verified through the experimental setup as shown in Fig. 10. In this model, four PV panels each rated for 37 W are connected at four different locations to produce a voltage of 60V. The dc sources are embedded within the switched inductor network, connected to the main inverter circuit to feed the load. The switching pulses of

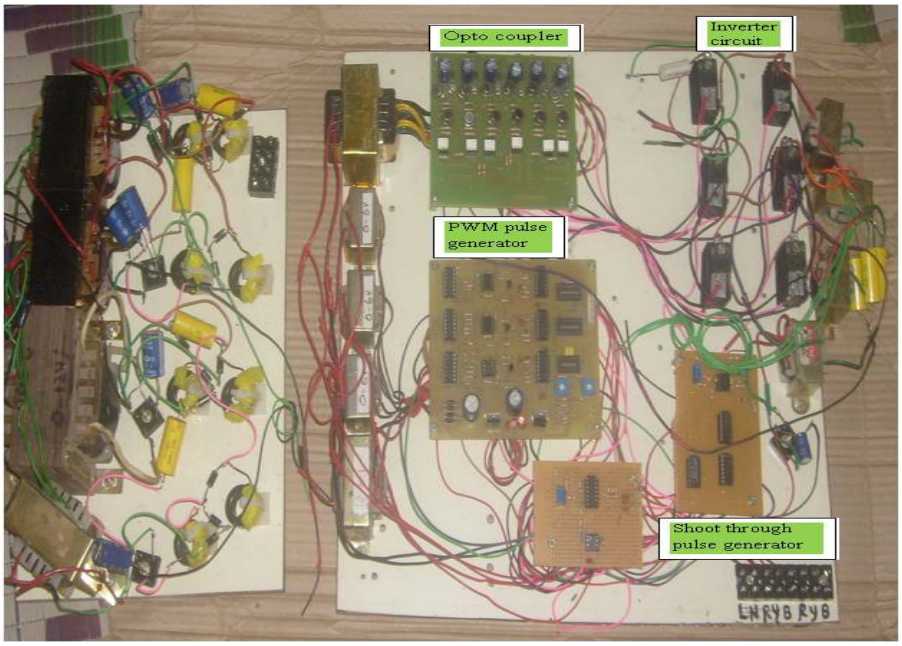

Fig. 11: Interior view of the proposed inverter

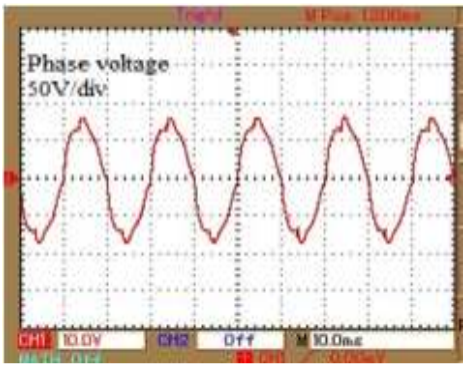

Fig. 12: Experimental phase voltage waveform, observed without filter

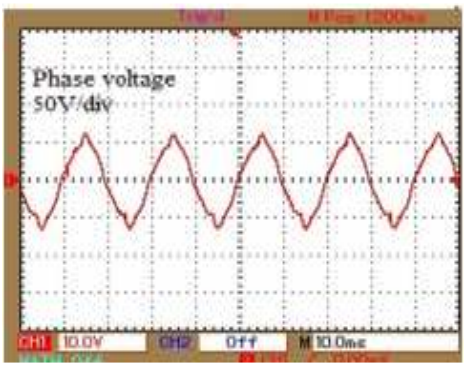

Fig. 13: Experimental phase voltage waveform, observed with filter

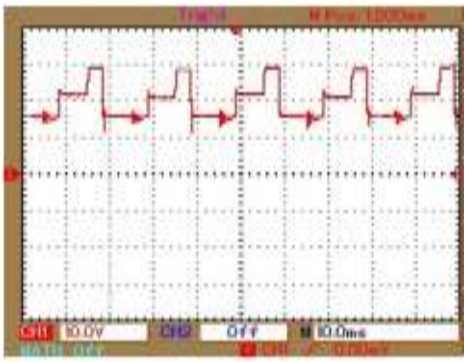

Fig. 14: Voltage waveform observed across the capacitor, C_1

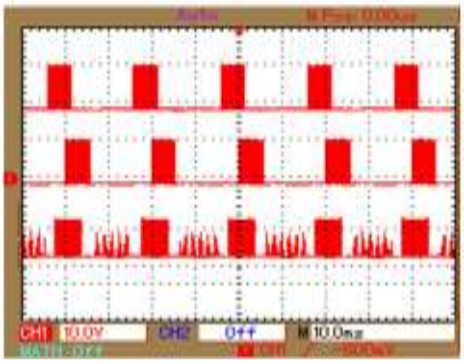

Fig. 15: Gate switching pulses observed across the inverter terminals

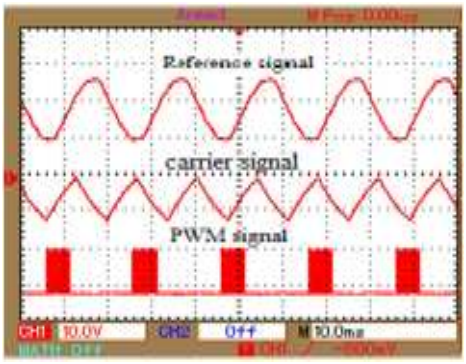

Fig. 16: Gate switching pulse observed for a single switch

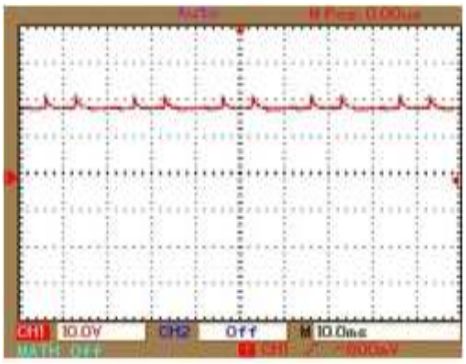

Fig. 17: Shoot through pulses observed for a single switch

the main inverter circuit are given from PWM pulse generating circuit employing 120° PWM control strategy. Shoot through pulses to turn ON the switches of the same phase leg are obtained through a separate circuit which is connected to the main PWM pulse generator circuit.

Figure 11 shows the various operating units like PWM pulse generator, shoot through pulse generator, isolation opto coupler and impedance network are assembled to form the hardware of the proposed inverter. Various IC's and passive elements are used to build the proposed inverter. It has IC MCT2E for isolation purposes. LM358P, HEF40106BP, CD4071BCN, HEF40718P are used to produce the pulses for the shoot through operations. Control signals for inverter switching operation with 120^0 phase shift are obtained through IC's TL084CN, LM358N and HCF408LBE to produce reference, triangle carrier and PWM pulses, respectively. Output phase voltage reaches 88 and 70 V, respectively, when observed without and with filter through the digital signal oscilloscope as shown in Fig. 12 and 13. It is also observed that the voltage stress across the capacitors is reduced as shown in Fig. 14. Switching pulses given to the inverter terminals are shown in Fig. 15. Waveforms

of reference, carrier and PWM signals captured for a single switch are shown in Fig. 16 and the shoot through pulse for a single switch is shown in Fig. 17.

CONCLUSION

A novel modified embedded switched inductor ZSI is proposed for solar photo voltaic applications. Simulations are carried out by employing 120° pulse width modulation scheme. Hardware, for the proposed inverter is implemented. The simulation and hardware results agree to a great extent. The proposed inverter exhibits better performance and is most suitable for solar PV applications.

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