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Research Article

A High Voltage-lift Efficient Isolated Full Bridge DC-DC Converter

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Abstract: The aim of this study is to propose a high voltage lift isolated full bridge dc-dc converter. The proposed converter consists of an isolation transformer a low turn ratio to obtain high step up voltage gain. The secondary of the transformer connected with two boosting capacitors which connects parallel when power switches switch on period and discharged in series during the switch off period. In addition full bridge converter on primary side consists of clamping diode and capacitor, leakage energy is recycled there by improving conversion efficiency. The proposed circuits simulated using PSIM software form input voltage of 48V, an output of 410 V obtained. These results and operations experimented and validated by implementing in hardware model at 20/40 Vdc, 20 Watts.

Keywords: Full bridge converter, PSIM software, voltage gain, voltage lift

INTRODUCTION

The conventional isolated converters like fly back, forward, push-pull and single ended primacy inductor converter can achieve high voltage gain by adjusting the turn ratio of the transformer. Further the leakage inductance energy in the transformer causes high voltage stress on the switches switch reduces the system efficiency which explained by Tsorng-Juu *et al*. (2013), Changchien *et al*. (2010) and Wang *et al*. (2004). Several non-isolated topologies developed to obtain high stet-up voltage fain in the past decade recently the topologies are described by Wu *et al*. (2008), Li *et al*. (2010) and Yang *et al*. (2011). The non-isolated converters can be used with the coupled inductor technique, cascade technique are can refer the authors Araujo *et al*. (2010) and Chen *et al*. (2011) and switched-inductor and switched capacitor techniques given by Axelrod *et al*. (2008) and Kuo *et al*. (2010) with appropriate duty ratio to obtain high voltage gain. But these converters not met the safety standards needed for galvanic isolation. To meet the safety standards some isolated converters are proposed for high step-up applications. These converters voltage lift techniques also boost type converters integrates with a transformer to obtain high voltage gain explanation given by Kuo *et al*. (2010) and Lin *et al*. (2009).

The dc-dc converters with coupled inductors can provide high voltage gain, but their efficiency is degraded by the losses associated with leakage inductors mention by Gopi and Saravanakumar (2013). These degradations improved in the proposed circuit provided with isolation transformer. The conventional topologies to get high output voltage use fly back converters, they have the leakage components that cause stress and loss of energy that results in low efficiency. These disadvantages overcome by using active clamp and the transformer turns ratio provides the high boost and isolation.

This proposed full bridge converter isolated dc-dc converter used phase shift technique. Also the proposed converter consists of an isolation transformer a low turn ratio to obtain high step up voltage gain. The secondary of the transformer connected with two boosting capacitors which connects parallel when power switches switch on period and discharged in series during the switch off period. In addition full bridge converter on primary side consists of clamping diode and capacitor, leakage energy is recycled there by improving conversion efficiency. The proposed circuits simulated using PSIM software form input voltage of 48 V, an output of 410 V obtained. These results and operations experimented and validated by implementing in hardware model at 20/40 Vdc, 20 Watts. The gate control signal of the switches S1 and S4 and S2 and S3 get simultaneously ON during this period freewheel state recycle leakage energy of the transformer to the input side. On the other side the concept of charge in parallel and discharge in series, output capacitors C1 and C2 and diodes D1 and D2 are utilized to form the voltage double circuits and to get high voltage gain. The circuit configuration of proposed isolated dc-dc full bridge converter is shown in Fig. 1. The proposed circuit consists of dc input voltage V_i, S1 to S4 power switches, C_a to C_d clamp diodes and capacitors. Transformer (T), two boosting capacitor C1 and C2 and diodes D1 and D2 and output diode D_o. Output capacitor C_o and the output load R. the transformer induces magnetizing inductance L_m and leakage inductance L_{kp} and L_{ks}.

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METHODOLOGY

Proposed DC-DC converter: The operating wave forms of the proposed converter are shown in Fig. 2. The proposed converter operating modes can be divided into four operating modes.

Mode-1 (t-t1): Switches S1 and S4 active switches are ON. Diodes D1 and D2 are reverse biased. Do is forward biased. The operating circuit in this mode is shown in Fig. 3. L_m stores energy from the input voltage V_i. L_m and leakage inductance L_k in series with V_i. Leakage i_{lk} continuous and circulates. When primary voltage zero hence input currents also be equal to zero. Secondary current is decreases; the secondary leakage L_{ks} limits the flow, to the output. The secondary winding voltage V_s and boosting voltages V_{C1} and V_{C2} are linked series to release energy to the

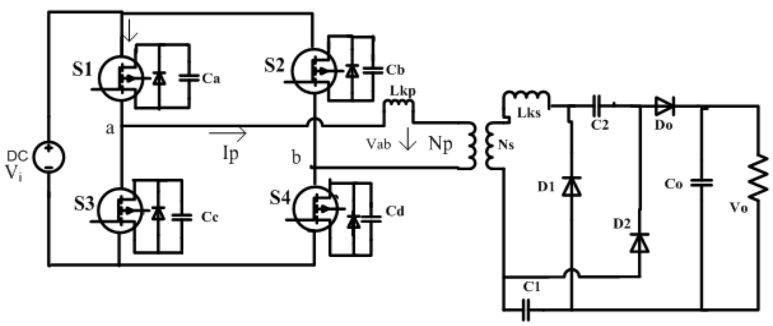

Fig. 1: Proposed isolated DC-DC full bridge converter

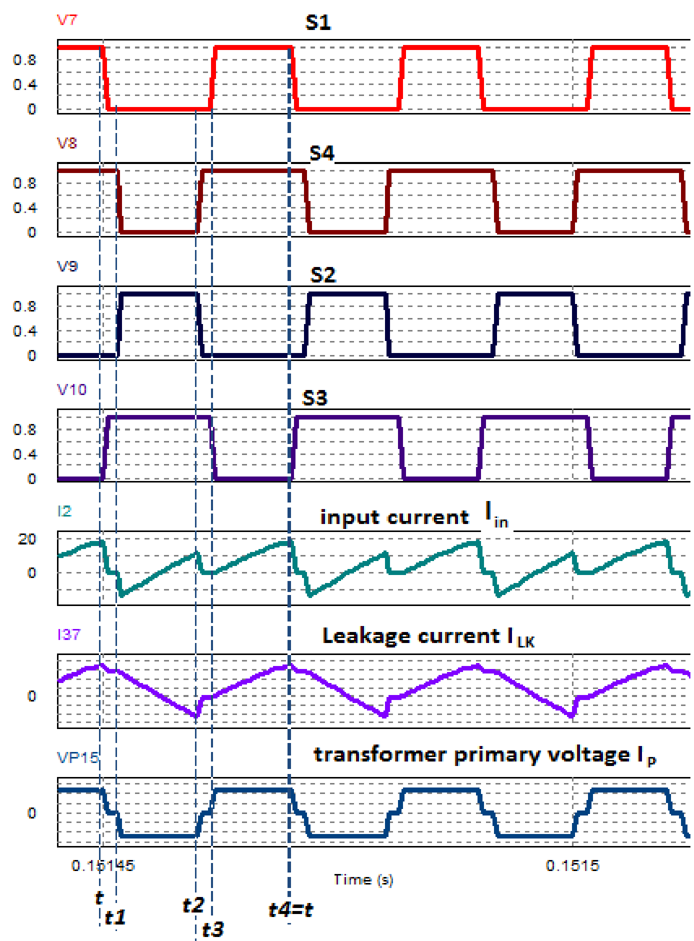

Fig. 2: Operating waveforms of proposed converter

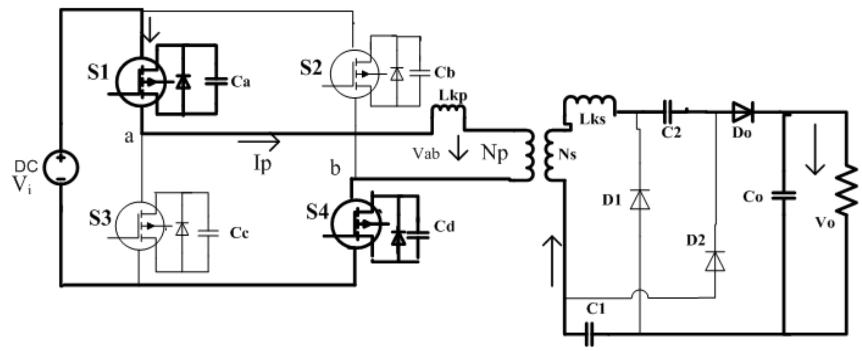

Fig. 3: Mode-1 operating circuit

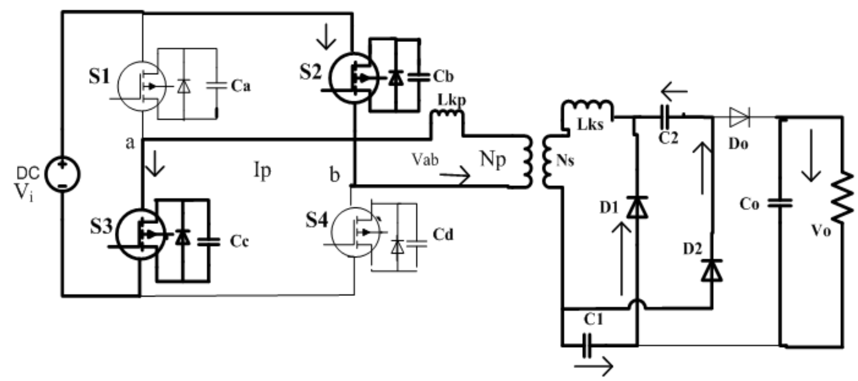

Fig. 4: Mode-2 operating circuit

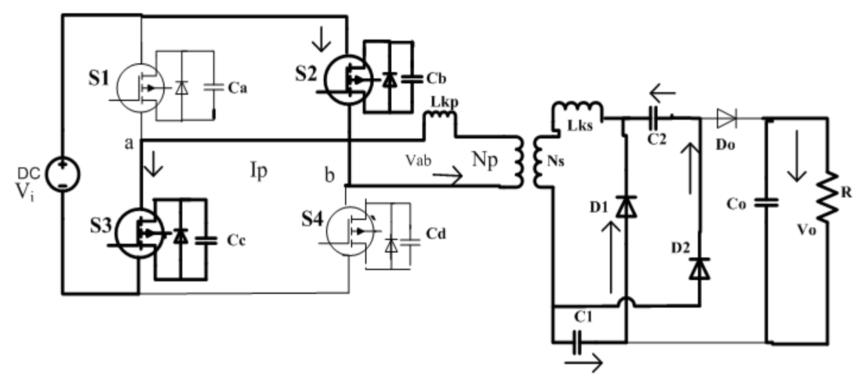

Fig. 5: Mode-3 operating circuit

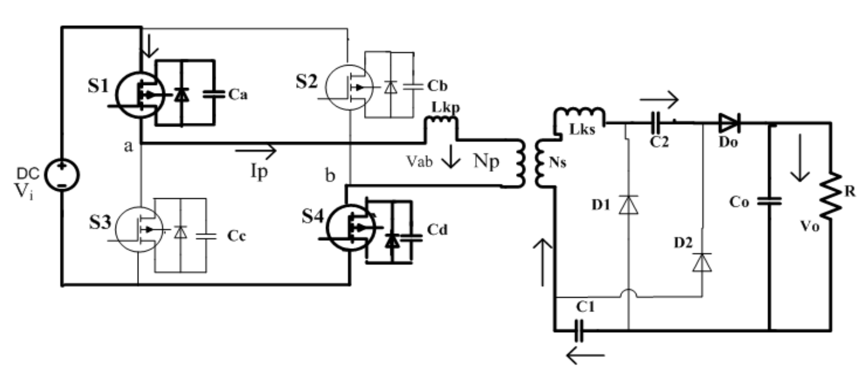

Fig. 6: Mode-4 operating circuit

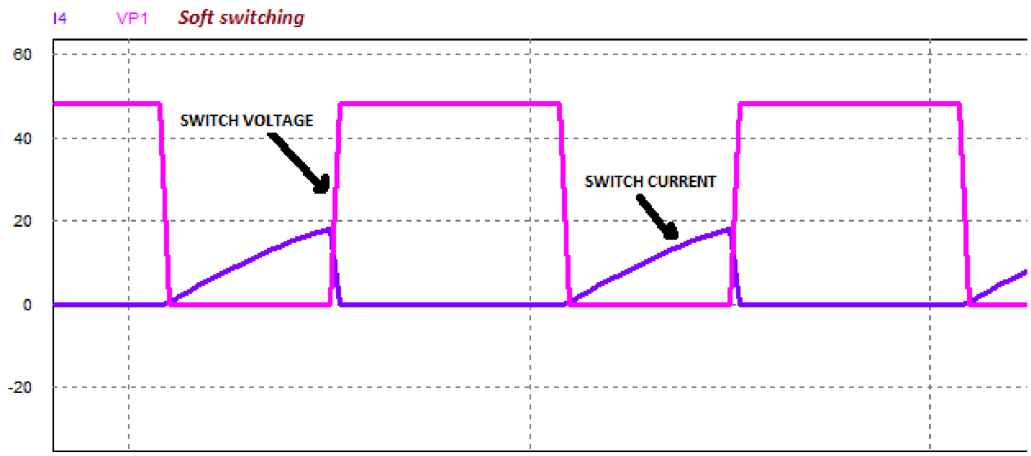

Fig. 7: ZVS soft switching

output capacitor C_o and the load R. When it drops to zero boosting capacitors C1 and C2 begin to charge. This mode ends at t = t1.

Mode-2 (t1-t2): S2 and S3 switches are ON. D1 and D2 forward bias. D_o reverse bias. L_m continuous to store energy from dc input voltage Vi. Vi delivered to secondary winding through D1 and D2 to charge the balancing equations C1 and C2 respectively. Voltage across C1 and C2 are nearly equal to nV_i. Id3 = id4, Co relives energy to output R. The operating circuit in this mode is shown in Fig. 4.

Mode-3 (t2-t3): S3 turned ON, S2 comes to OFF, S4-comes to ON, S1 is OFF at end. D_o reverse biased, D1 and D2 forward biased. I_{lk} charges the clamping capacitances. Boosting capacitors C1 and C2 continue to charge the input voltage Vi. Input current stats increasing and leakage current stats decreases. D1 and D2 and Co continues to release energy to load R. operations ends at t = t3. The operating circuit in this mode is shown in Fig. 5.

Mode-4 (t3-t4): S1 is ON, S3 is OFF, S4 is ON and S2 already OFF. D1 and D2 forward biased. D_o is reverse biased. I_{lk} delivers quickly. C1 and C2 continue to produce energy in forward mode. This modes end id1 = id2 = 0 at t = t4. The operating circuit in this mode is shown in Fig. 6.

Zero voltage switching: The proposed converter is in the switching technique of DC-DC phase-shift converters to reduce the switching losses. Returning to the turn-on loss if V_{DS} is set to zero there will be no losses at all. This principle is known as Zero-Voltage Switching (ZVS).

ZVS is achieved by forcing the current flowing through the switch to reverse. When the switch current reverses the body diode clamps the voltage to low value. When the voltage waveform reaches its zero crossing point the current is still negative allowing zero-voltage switching. With the techniques proposed the performance at normal operation could be improved. Even with ZVS technique the Turn on loss could be minimized and turn off loss limits the capability of the converter to operate at higher switching frequency. ZVS of proposed converter simulated waveform shown in Fig. 7.

RESULT ANALYSIS

While the S1 and S4 ON, D1 and D2 forward biased. V_{Lp} the primary magnetizing inductance voltage. And boosting capacitor voltages V_{C1} and V_{C2} are given by:

$$V_{Lp=} V_i \tag{1}$$

$$v_{C1} = v_{C2} = nV_i \tag{2}$$

While active switches are off. The primary magnetizing inductance voltage VLP for this interval is:

$$v_{LP} = 2V_{in} - \frac{V_o}{n} \tag{3}$$

$$V_o = 2 \times V_s \tag{4}$$

Application of the principle of volt-second balance, The primary-side magnetizing inductance Lm yields:

$$\int_0^{DTs} V_i \, dt + \int_{DTs}^{Ts} (2V_i - \frac{V_0}{n}) dt = 0 \tag{5}$$

using Eq. (5). The voltage gain is given by:

$$V_{Gain} = \frac{V_o}{V_i} = \frac{n(2-D)}{1-D} \tag{6}$$

Performance analysis: The voltage gain can be obtained from inductor volt-second balance principle from Eq. (6) the output voltage is given by:

$$V_o = \left(\frac{n(2-D)}{1-D}\right)V_{in} \tag{7}$$

Voltage gain rises when turns ratio (N) increases. To optimize the load regulation performance to the proposed isolated high boost DC-DC converter extreme duty cycle can be designed. N = 0 it is the conventional converter. The voltage gain of the proposed converter is increases greatly by using a proper turn's ratio design. The voltage stress of the switch and clamp diode can be written as:

$$V_{stress} = \frac{V_{in}}{1-D} \tag{8}$$

Turns ratio design play an important role in the circuit design, by using this find out the voltage stress of the switch and duty ratio also obtained, it is given by:

$$N = \frac{(1-D)\times V_o}{V_{in}} \tag{9}$$

These both capacitors are used as DC voltage source; the aim is to reduce the ripples in the capacitors. The relationship between the output power and voltage ripple is given by:

$$C = \frac{P_o}{V_o \times \Delta V_c \times f_s} \tag{10}$$

$$P_o = V_o \times \Delta V_C \times C \times f_s \tag{11}$$

In above equation ΔV_c is voltage ripple on the capacitor C_1 or C_2. The proposed dc-dc converter defined as low loss converter. The efficiency of the converter is the ratio of the output power to the input power.

Simulation results: The proposed circuit is simulated in PSIM software. The circuit simulation of phase shift converter with voltage lift and the output waveforms are shown in Fig. 8. In Fig. 8 shows diode D1 current, diode D2 current, output diode current and output capacitor current respectively with switching pulses S1 to S4.

The output voltage waveform is shown in Fig. 9. The observations from the simulation output waveform are tabulated in Table 1.

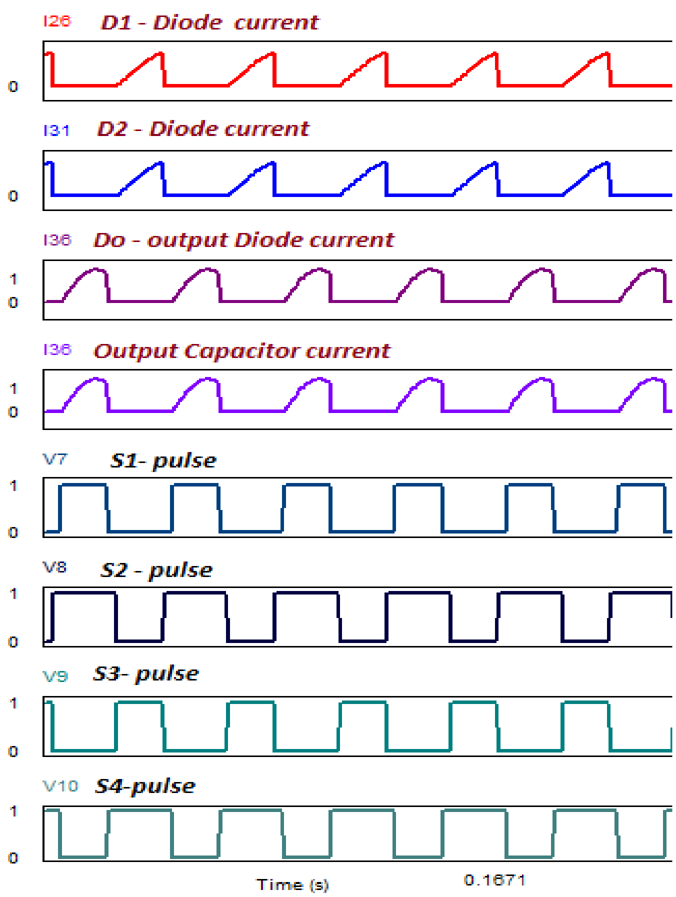

Fig. 8: Diode D1 and D2, Do and Co currents and switching pulses

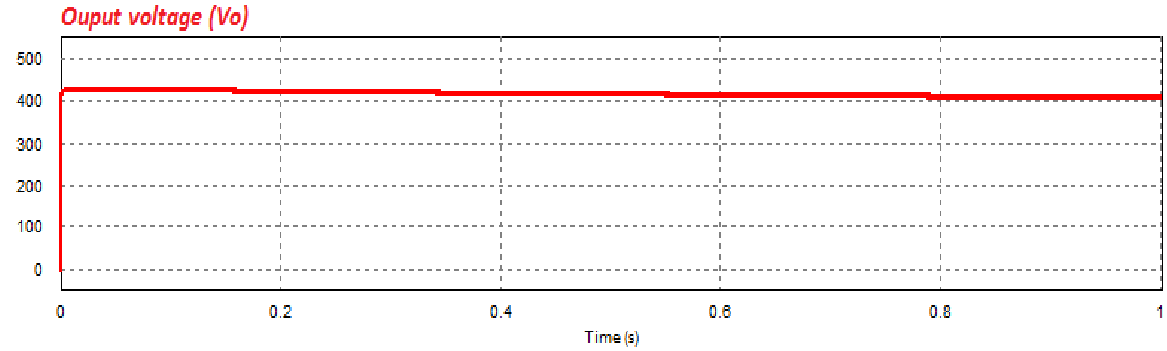

Fig. 9: Output voltage

Table 1: Simulation specifications

Parameters	Specifications
Input	48 V
Turns ratio n	1:3
Output	410 V
Output power	160 W
Output current	0.390 A
Output resistance	1100 ohm

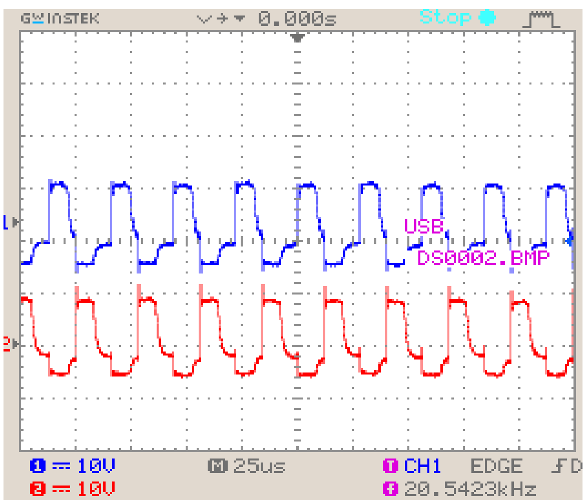

Fig. 10: Drain to source voltage of switches S1 and S4

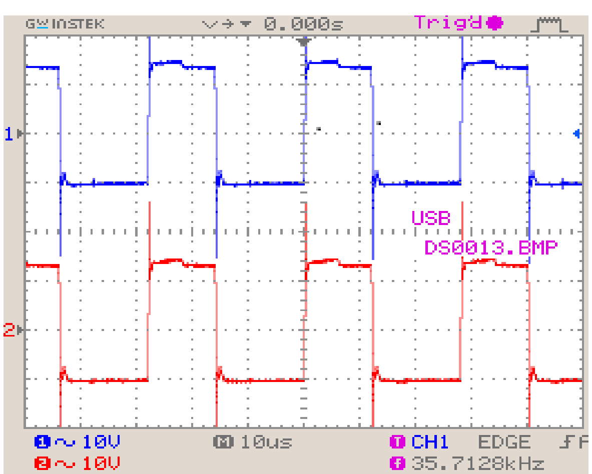

Fig. 11: Isolated transformer primary and secondary voltage

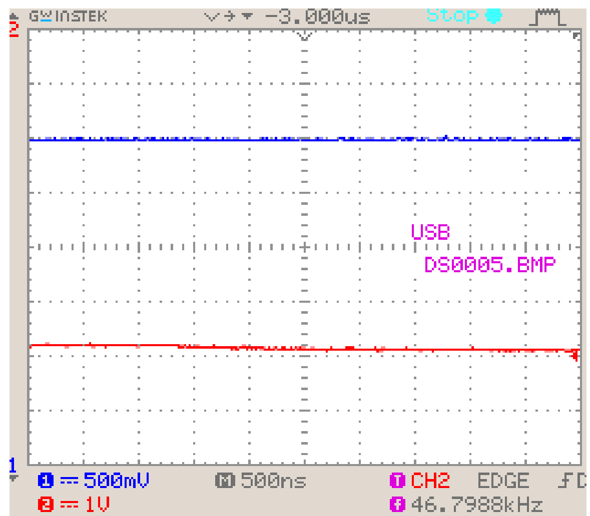

Fig. 12: Input voltage and output voltage

Experimental results: The hardware model of the proposed circuit can be implemented. The hardware is implemented 20/40 Vdc 20 Watts prototype model. The results of the hardware model are compared with theoretical and with the simulation results.

The output waveform is observed by using Digital Signal Oscilloscope and measured. The output results obtained from the prototype. Figure 10 shows the MOSFET switches S_1 to S_4 drain to source voltage drops during switching period with loading operation. The isolated transformer primary and secondary change in voltage observed waveform shown in Fig. 11. The output voltage lifted up to 40 V (Table 2). The input voltage, output voltage of the proposed converter is shown in Fig. 12. Hence it is realized with the simulation output voltage $V_o = 400$ V. The experimental results show that the output voltage can be boost upto the voltage gain 8.5 and the output voltage matches the theoretical value of the given Eq. (6). Thus, the proposed boost converter can be interface to the inverter grid at the user end. The experimental results are tabulated in Table 2. The calculated efficiency of the proposed model at full load is 97.8%. Due to the

Table 2: Hardware specifications

Parameters	Specifications
Input voltage	20 V
Output voltage	40 V
Primary turns	100
Secondary turns	200
Output voltage	40 V
Output power	20 W
Output current	0.07 A

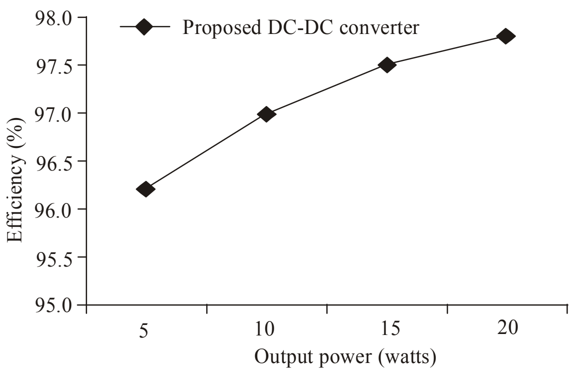

Fig. 13: Efficiency (%) vs. output power (watts)

limitations in the power hardware setup, the prototype was intended only to verify the operational concept (Fig. 13).

CONCLUSION

In this study phase shift full bridge converter have been successfully implemented using voltage lift technique to achieve high voltage gain. Energy stored in the primary leakage inductance during ON time returned to input side Vi via clamping diodes D1 and D2. This improves the efficiency and reduces voltage stress on the power switches. So low voltage rating and low-on-resistance R_{on} switches can be selected. Here steady state voltage gain has been analyzed in detail. Simulation done using PSIM software from the simulation results 48 V input dc voltage can lift upto 410 Vdc output at 160 watts output power. Also the results validated with the experiment. Further an improvement of this topology can be useful to demonstrate the new features.

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