Research Journal of Applied Sciences, Engineering and Technology 7(23): 4986-4998, 2014
DOI:10.19026/rjaset.7.890
ISSN: 2040-7459; e-ISSN: 2040-7467

Submitted: January 31, 2014 Accepted: March 24, 2014 Published: June 20, 2014

Research Article

Improved Parallel Boost Power Converter for Power Factor Correction

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Abstract: The main objective of the study is to analysis and design parallel boost power converter for power factor correction using an active filtering approach by implementing single-phase soft-switching technique with an active snubber circuit. Zero voltage transition to turn ON and zero current transition to turn OFF is implemented by the active snubber circuit for the main switches with no any further current or voltage strains. By zero-current switching without the need of added voltage stress, auxiliary switch is turned ON and OFF. The proposed converter has simple structure, low cost and ease of control. The efficiency, which is about 96% in hard switching, will increases to about 98% in the proposed soft-switching parallel boost converter.

Keywords: Boost converter, Power Factor Correction (PFC), rectifier, Soft-Switching (SS), Zero-Current Switching (ZCS), Zero-Current Transition (ZCT), Zero-Voltage Switching (ZVS), Zero-Voltage Transition (ZVT)

INTRODUCTION

The boost converter topology is continuously used in various ac-dc and dc-ac applications (Silva Ortigoza *et al*., 2012). Isolated ac/dc converters are frequently employed in service interfaced systems such as power supplies in telecommunication and data centers, plug-in hybrid electrical vehicles and battery operated electric vehicles (Jordi *et al*., 2012). A low-cost and stout ac to dc converter consisting of a line frequency diode bridge rectifier with a large output filter capacitor requires a harmonic affluent ac line current. As a consequence, the input power factor is derived (Ortiz *et al*., 2012).

Nowadays, designers provide all the electronic devices to meet the harmonic content requirements. ac-dc converters have drawbacks of poor power quality in terms of injected current harmonics, which cause voltage distortion and poor power factor at input ac mains and slow varying ripples at dc output load, low efficiency and large size of ac and dc filters (Singh *et al*., 2003) These converters are required to operate with high switching frequencies due to demands for small converter size and high power density. High switching frequency operation, however, results in higher switching losses, increased Electromagnetic Interference (EMI) and reduced converter efficiency (Wannian and Moschopoulos, 2006).

Soft switching technique is more suitable for IGBT applications, when compared with power MOSFET's, which presents much higher conduction losses than IGBT's. On the other hand, IGBT's are relatively slow in switching speed, so the switching losses and the high frequency of operation are two well-known problems (Yungtaek and Milan, 2002; Rangan *et al*., 1989; Wang *et al*., 1994). There has been an increasing interest in the soft-switching power conversion technologies in order to overcome the limitations of the hard-switching technologies Soft-switching techniques have been proposed for power converters since 1970s (Lai *et al*., 1996; McMurray, 1993; Rogayeh *et al*., 2011; Deepakraj, 1989).

Switching frequency should be increased by decreasing switching losses to achieve higher power density and faster transient response in well known Pulse Width Modulated (PWM) dc-dc converters (Ned Mohan *et al*., 2003). This aim can be realized by using soft switching techniques instead of hard switching techniques. Soft switching techniques are implemented by snubber cells and basically provide Zero Voltage Switching (ZVS) or Zero Current Switching (ZCS) for semiconductor devices in these converters (Bodur and Faruk, 2002, 2004; Yu *et al*., 2002; Bodur *et al*., 2003).

Soft-switching technique improves performance of the high-power-factor boost rectifier by reducing switching losses. The losses are reduced by an active snubber circuit, which consist of an inductor, a capacitor, a rectifier and an auxiliary switch. Since the auxiliary switch is turn's OFF and ON with zero current, this technique is well suited for the implementation of switch insulated-gate bipolar transistors. The reverse-recovery-related losses of the rectifier are also reduced by the snubber inductor which is connected in series with the boost switch and the boost rectifier (Yungtaek and Milan, 2002). Active

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Power-Factor-Correction (PFC) technique, using a boost converter, has been successfully implemented to improve the power factor and reduce input current distortion in single-phase line current rectification. A near unity power factor and very low harmonic distortion along with good output voltage regulation can be achieved (Salmon, 1993). In parallel operation of converters, uniform current distribution among modules is of primary concern. Unbalanced current sharing is always encountered even with a careful design (Siri *et al*., 1992).

In this study, a new active snubber circuit is proposed to contrive a new family of PWM converters. This proposed circuit provides perfectly ZVT turn ON and ZCT turn OFF together for the main switch of a converter by using only one quasi resonant circuit without an important increase in the cost and complexity of the converter. This study is organized as follows. Classical Boost Converter is presented first, Need for Power Factor Correction is presented next then proposed Parallel Boost Converter with Active Snubber Circuit is presented after that describes the MATLAB Simulation for Proposed Boost Converter with Active Snubber. Finally Simulation Results and Discussions, Conclusion is presented.

MATERIALS AND METHODS

Classical boost converter: The basic circuit diagram of the classical Boost converter is represented in Fig. 1. It consists of inductor L_f, Capacitor C_1, V_g and V_{out} represents rectified input voltage and output voltage respectively, switch S is an active switch, diode D is a freewheeling diode and R_{load} is the load resistance. Switch S operates at a switching frequency f_s with duty ratio D to obtain the mathematical model of the controller, the state model of Boost converter is derived by considering S = 1 during IGBT switch condition subinterval and S = 0 during the diode conduction subinterval (Mahdavi *et al*., 1997; Umamaheswari and Uma, 2013).

Mathematical model for classical boost converter: The converter dynamics is described by state-space averaging method and by using the same method, the state equations during switch-on and switch-off conditions are combined as follows:
When the switch is ON (S = 1):

$$\frac{d_{i_L}}{dt} = \frac{1}{L_f}(V_g) \tag{1}$$

$$\frac{dV_{0ut}}{dt} = \frac{1}{C_1}(-\frac{V_{out}}{R_{load}}) \tag{2}$$

At 0<t<TON; S = ON.
And when the switch is OFF (S = 0):

$$\frac{d_{i_L}}{dt} = \frac{1}{L_f}(V_g - V_{out}) \tag{3}$$

$$\frac{dV_{out}}{dt} = \frac{1}{C_1}(i_L - \frac{V_{out}}{R_{load}}) \tag{4}$$

At TON<t<T; S = OFF.

Similar to the previous case, the state space averaging model results the following equations:

$$\frac{dx_1}{dt} = \frac{1}{L}V_g - \frac{(1-D)}{L}x_2 \tag{5}$$

$$\frac{dx_2}{dt} = \frac{1-D}{C_1}x_1 - \frac{1}{R_{load}C_1}x_2 \tag{6}$$

$$\frac{dx_1}{dt} = \dot{x}_1 \text{ and } \frac{dx_2}{dt} = \dot{x}_2 \tag{7}$$

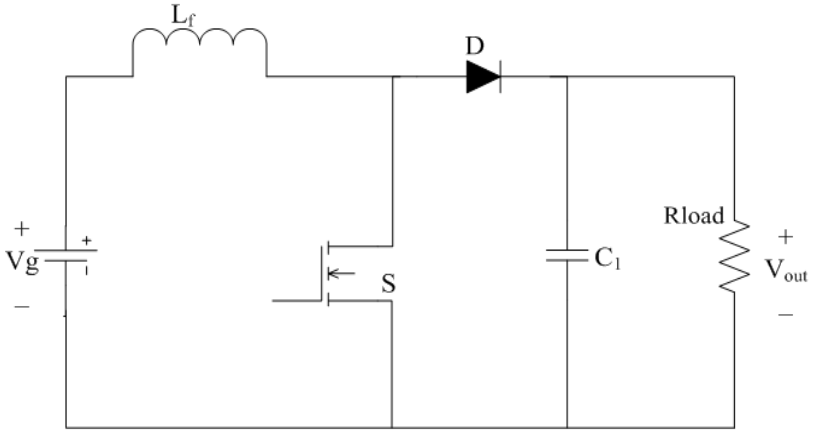

Fig. 1: Circuit diagram for classical boost converter

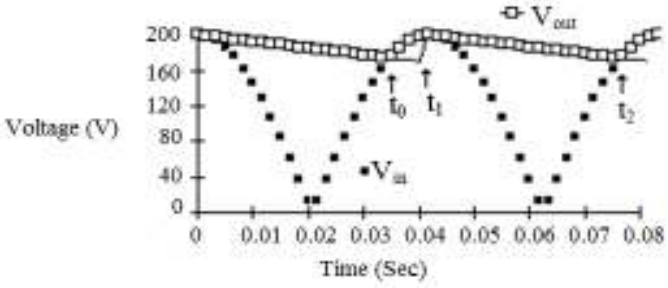

Fig. 2: Output voltage of a full wave rectifier for Vin = 200 V

Sub (7) in (5) and (6):

$$\dot{x}_1 = \frac{1}{L_f} V_g - \frac{1-D}{L_f} x_2 \tag{8}$$

$$\dot{x}_2 = \frac{1-D}{C_1} x_1 - \frac{1}{R_{load}\, C_1} x_2 \tag{9}$$

where, x_1 and x_2 are the current through the inductor (i_L), Voltage across the output capacitor (V_C) respectively and D represents the duty cycle. From Eq. (8) and (9), the averaged system matrices were derived as given below:

$$A = \begin{bmatrix} 0 & \frac{-(1-D)}{L_f} \\ \frac{1-D}{C_1} & \frac{-1}{R_{load}\, C_1} \end{bmatrix}, \quad B = \begin{bmatrix} \frac{1}{L_f} \\ 0 \end{bmatrix} \tag{10}$$

Mathematical model of single phase classical boost converter with rectifier unit: The circuit scheme of the proposed power factor correction converter mainly consists of a full wave bridge rectifier and a modified boost converter. The filtered full wave rectifier is obtained from the FWR by adding a suitable capacitor at the output. The FWR output is the outcome of the addition of a capacitor. The output is presently a pulsating dc, during a peak to peak variation is recognized as ripple. The input voltage magnitude and frequency be obtained during the magnitude relies of the ripple, through the filter capacitance, as well as the load resistance. The rectifier input is a sine wave of frequency f. For the rectifier let V_{in} be the filter stage input which is a full wave rectified signal and the output is denoted as V_{out}. Input voltage can be anticipated as the complete value of the rectifier input, with the frequency of 2f.

For the duration of the time period t_0 to t_1, the diode D_1 (or D_3, based on the segment of the signal) is forward biased then $V_{in}>V_{C1}$ (inexact the forward biased diode as a short circuit), when the capacitor C_1 get charged due to the voltage across the load R increases. Starting from t_1 to t_2, the D_1 and D_2 diodes are biased reversely (open circuit) as $V_{cap}>V_{in}$ and then the capacitor get discharge over the load R_{load} during a time constant of $R_{load}C_1$ seconds as in Fig. 2. Along a capacitor discharge arc the voltages among times t_1 and t_2 set. Through which the output voltage is:

$$V_{out}(t) = V_{mx} e^{\frac{-t+t_1}{R_{load}\, C_1}} \tag{11}$$

The peak to peak ripple is indicating as the voltage difference between V_{max} and V_{min}:

$$V_{Ripp}(PP) = V_{out}(t_1) - V_{out}(t_2)$$
$$V_{Ripp}(PP) = V_{mx} - V_{mn} \tag{12}$$

$$V_{Ripp}(PP) = V_{mx}\left[1 - e^{\frac{-t_2+t_1}{R_{load}\, C_1}}\right] \tag{13}$$

If C is huge, such that $RC>>t_2 - t_1$, we can estimate the exponential:

$$1 - e^{\frac{-t_2+t_1}{R_{load}C_1}} \text{ as } 1 + \frac{-t_2+t_1}{R_{load}\, C_1}$$

Then,

$$V_{Ripp}(PP) = V_{mx} \frac{(t_2 - t_1)}{R_{load} C_1} \tag{14}$$

Then t_2-t_1~t/2, somewhere t is the period of the sine wave, Now:

$$V_{Ripp}(PP) = V_{mx} \frac{t}{2 R_{load}\, C_1} = \frac{V_{mx}}{2\text{fR}_{\text{load}}\, \text{C}_1} \tag{15}$$

The voltage through the inductor rises to a value that is greater than the combined voltage across the

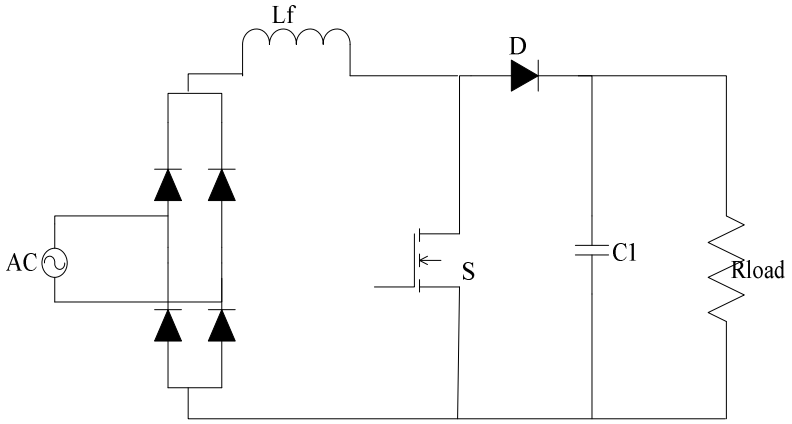

Fig. 3: Circuit diagram for single phase classical boost converter

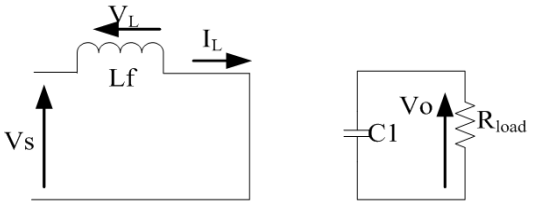

Fig. 4: On state of classical boost converter

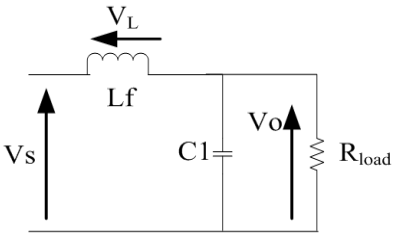

Fig. 5: OFF state of classical boost converter

diode and the output capacitor. After this value is obtained, the diode starts conducting and the voltage that seems across the output capacitor, is higher than the input voltage. This causes current to flow through it and store energy magnetically. On switching off this voltage causes the stored energy to be transmitted to the voltage output in a restricted way. The output voltage is synchronized by modifying the ratio of on/off time.

In Fig. 3 indicates the circuit diagram for single phase Classical Boost Converter. The circuit is constructed by inductor L_f, Capacitor C_1, Load resistor R_{load}, Switch S, Diode D and input AC source with bridge rectifier. From Fig. 4 while the switch is on, the voltage through the inductor is:

$$V_{L_{on}} = L_f \frac{di}{dt} = L_f \frac{I_{L_{peak}}}{t_{on}} \tag{16}$$

Then the current is given by:

$$I_{Lon} = \left[\frac{V_{in} - V_{sat}}{L_f}\right] t_{on} \tag{17}$$

From the Fig. 5, after the switch is off, the voltage across the inductor is set by:

$$V_{L_{off}} = L_f \frac{di}{dt} = L_f \left[\frac{I_{Lmn} - I_{L_{peak}}}{t_{off}}\right] \tag{18}$$

As well as the current is given by:

$$I_{Loff} = I_{L_{peak}} - \left[\frac{V_{out} + V_{Frwd} - V_{in}}{L_f}\right] t_{off} \tag{19}$$

where, V_{Frwd} is the forward voltage drop of the output rectifier and V_{sat} is the saturation voltage of the output switch. As $I_{Lon} = I_{Loff}$, Eq. (12) and (14) can be fixed equal to each other. This process gives a ratio for the on time over the off time. This is given by:

$$\frac{t_{on}}{t_{off}} = \frac{V_{out} + V_{Frwd} - V_{in(mn)}}{V_{in(mn)} - V_{sat}} \tag{20}$$

The drawbacks of classical boost converter is poor power quality in terms of injected current harmonics, voltage distortion and power factor at input ac mains and slow-varying ripples at dc output load, low efficiency and large size of ac and dc filters. So it is proposed to develop a parallel boost converter.

Need for power factor correction: Power Factor is usually specified as a number between 0 and 1 and is equal to the ratio of reactive power to active power, or Cosine. The increase in power factor number makes the system more efficient. Thus, a system with a Power

Factor of 0.9 is much more efficient than the power factor with 0.6.

The benefit of power factor correction is the elimination of charges related to reactive power-consumption. Improvement in power factor eliminates utility power factor penalties, which may be applied to users with poor power factors. Such penalties can result in electricity bills for users being increased by anything up to 20%, depending on individual electricity companies. High power factor reduces the I^2R losses. This result reduces heat in cables, switchgear, transformers and alternators which also prolong the life of such equipment. Using same cable to supply a larger motor and improving the starting of motors at the end of long cable runs by the reduction of voltage drop in cables. An investment for power factor correction is typically between 12 to 24 months. So it was felt that there is a need for power factor correction techniques.

Passive power factor correction and Active power factor correction are the two methods. Harmonic current can be controlled in the simplest way by using a filter that passes current only at line frequency. Harmonic currents are suppressed and the non-linear device looks like a linear load. Power factor can be improved by using passive devices. Such capacitor and inductor filters with passive devices are called passive filters. The passive power factor correction large value high current inductors are commanded, which are expensive and bulky. An active approach is the most effective way to correct power factor of electronic supplies. Here, boost converters are designed between the bridge rectifier and the main input capacitors. The converter tries to maintain a constant DC output bus voltage and draws a current that is in phase with and at the same frequency as the line voltage. The overall advantages of proposed active power factor correction is dynamic wave shaping of the input current, high frequency switching filtering, feedback sensing of the source current for waveform control and regulate output voltage with feedback control.

Proposed parallel boost converter with active snubber circuit: Usually, boost converters are used as active Power factor correctors. However, a recent novel approach for PFC is to use dual boost converter i.e., two boost converters connected in parallel. By using a parallel scheme, where inductor L_{f1} and switch S_1 are for main PFC while L_{f2} and S_2 are for active filtering. The filtering circuit serves two purposes i.e., improves the quality of line current and reduces the PFC total switching loss. The reduction in switching losses occurs due to different values of switching frequency and current amplitude for the two switches. The parallel connection of switch mode converter is a well known strategy. It involves phase shifting of two or more boost converters connected in parallel and operating at the same switching frequency (Parillo, 2012). The overall advantages of using this approach is to improve the efficiency, reduce the development cost, high reliability, reduced current ripples, reduced conduction losses and reduced the size of active and passive components as boost inductor.

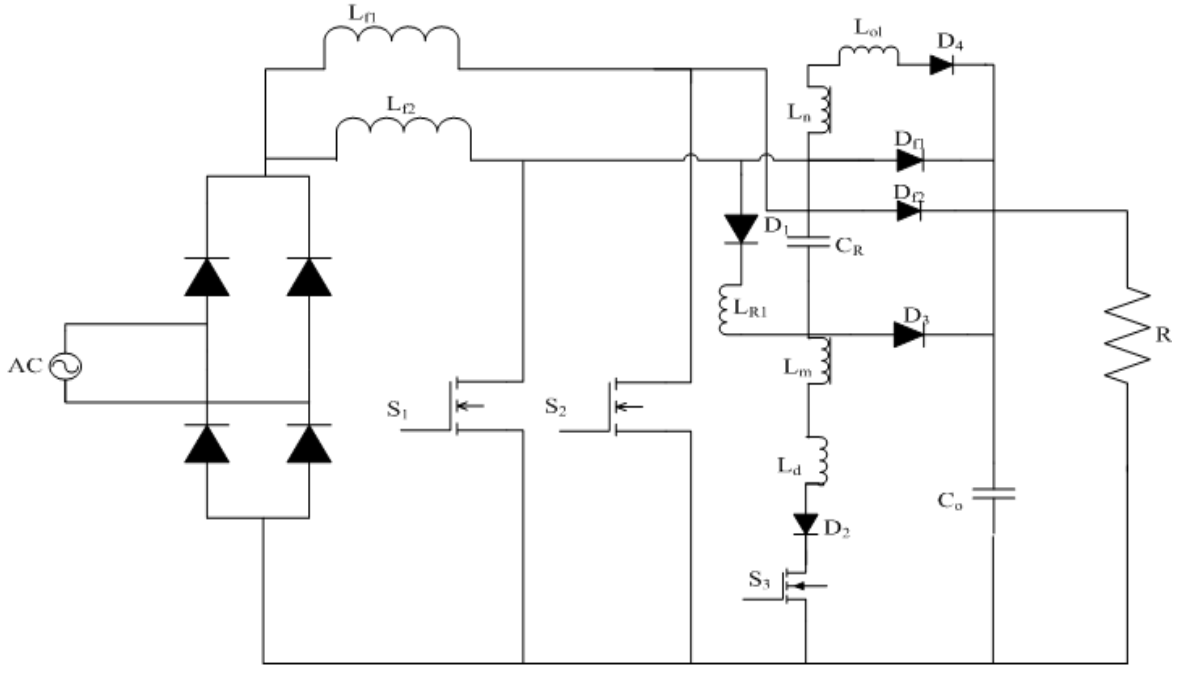

Fig. 6: Circuit diagram for single phase boost converter with active snubber

The purpose of Parallel Boost Converter is to avoid twice power process in two-stage scheme. Two converters can be connected in parallel to form the parallel PFC scheme. Here, power from the ac main to the load flows through two parallel paths. The main path is a rectifier, in which power is not processed twice for PFC, whereas the other path processes the input power twice for PFC purpose. To achieve both unity power factor and tight output voltage regulation, only the difference between the input power and output power needs to be processed twice. Therefore, high efficiency can be obtained by this method. Normally, boost converters are used as active Power factor correctors. However, a recent novel approach for PFC is to use parallel boost converter i.e., two boost converters connected in parallel. Circuit diagram of parallel boost converter for PFC is shown in Fig. 6. By using the snubber circuit, it reduces or eliminates voltage or current spikes, limitation of dI/dt or dV/dt, shape the load line to keep it within the Safe Operating Area (SOA), transfer power dissipation from the switch to a resistor or a useful load, due to switching reduce total losses, ringing damping voltage and current to reduce EMI. The advantages of parallel boost converter with active snubber circuit is to improve overall efficiency, high reliability, reduced development cost due to the modular design, low harmonics and conduction loss.

Features of proposed parallel boost converter: Assume both the Main Switches (S_1 and S_2) are operates in the same frequency:

- All the Semiconductors are work with soft switching in the proposed converter.
- The main switches S_1 and S_2 are turn on with ZVT and turn off with ZCT.
- The secondary switch is turn on with ZCS and turn off with ZCS.
- All other components of the parallel boost converter functioned based on this soft switching.
- There is no additional current or voltage force on the main switches S_1 and S_2.
- There is no additional current or voltage force on the secondary switch S_3.
- Also there is no additional current or voltage force on the main Diodes D_{f1} and D_{f2}.
- According to the ratio of the transformer, a part of the resonant current is transferred to the output load with the coupling inductance. So there is less current stress on the secondary switch with satisfied points.
- At resistive load condition, in the ZVT process, the main switches voltage falls to zero earlier due to decreased interval time and that does not make a problem in the ZVT process for the main switch.
- At resistive load condition, in the ZCT process, the main switches body diode ON-state time is increased when the input current is decreased. However, there is no effect on the main switch turn-OFF process with ZCT.
- This parallel boost converter is operates in high-switching frequency.
- This converter is easily control because the main and the auxiliary switches are connected with common ground.
- The most attraction of this proposed converter is using ZVT and ZCT technique.
- The proposed new active snubber circuit is easily adopted with other basic PWM converters and also switching converters.
- Additional passive snubber circuits are not necessary for this proposed converter.
- SIC (Silicon Carbide) is used in the main and auxiliary diodes, so reverse recovery problem is not arise.
- The proposed active snubber circuit also suitable for other dc-dc converters.

Figure 7 shows the components of proposed boost converter. It is the combination of new active snubber circuit with parallel boost converter. Three switches are used switch S_1 and S_2 are act as main switch and S_3 act as an auxiliary switch. S_1 and S_2 are controlled by ZVT and ZCT respectively also S_3 is controlled by ZCS. This circuit operates at 200V/50Hz AC supply. The proposed converter block diagram is in Fig. 7.

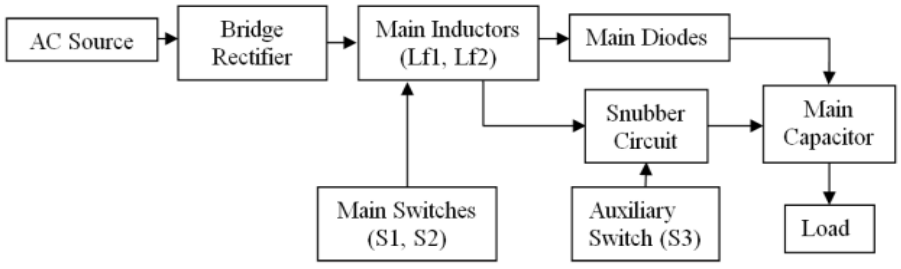

Fig. 7: Components of single phase parallel boost converter with active snubber

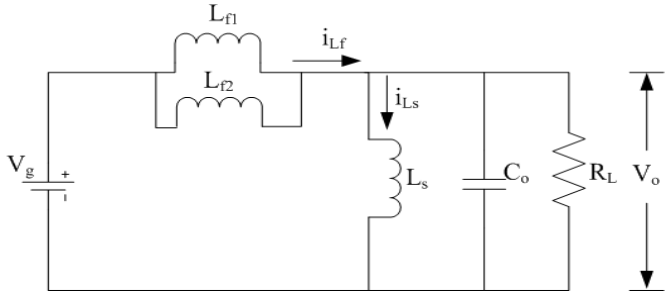

Fig. 8: When $S_1 = S_2 = 0$ and $S_3 = 1$

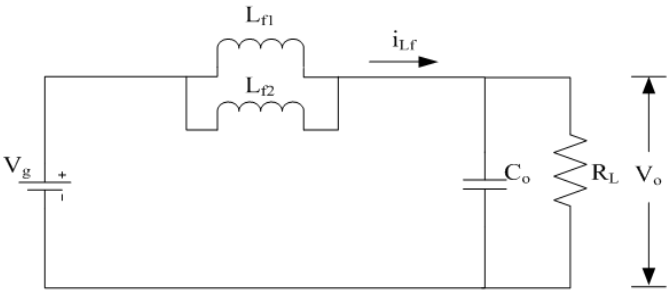

Fig. 9: When $S_1 = S_2 = S_3 = 1$

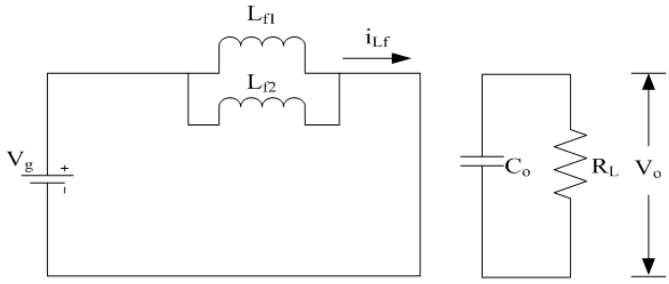

Fig. 10: When $S_1 = S_2 = 1$ and $S_3 = 1$ or 0

Mathematical model for parallel boost converter with active snubber circuit: Figure 6 represents the circuit diagram of the parallel boost converter with active snubber. It consists of five inductors L_{fi}, L_{f2}, L_{R1}, L_{R2}, L_n and three capacitors C_s, C_r, C_o, V_g and V_o represent supply and output voltage respectively, S (S_1, S_2) is an active primary switch, D (D_{f1}, D_{f2}) is a freewheeling diode, D_s (D_1, D_2, D_3) is a Snubber diode and R_L is the load resistance. S (S_1, S_2, S_3) operates at a switching frequency f_s with duty ratio d.

Choose the switching frequency of switches $S_1 = S_2$ = 100 KHz and S_3 = 200 KHz.

When $S_1 = S_2 = 0$ and $S_3 = 1$ as in Fig. 8:

$$\frac{diL_F}{dt} = \frac{1}{L_F}\left[V_g = V_o\right] \tag{21}$$

$$\frac{dV_o}{dt} = \frac{1}{C_o}\left[iL_F - \frac{V_o}{R_L} - iL_S\right] \tag{22}$$

Also the switches $S_1 = S_2 = S_3 = 1$ as in Fig. 9:

$$\frac{diL_F}{dt} = \frac{1}{L_F}\left[V_g - V_o\right] \tag{23}$$

$$\frac{dV_o}{dt} = \frac{1}{C_o}\left[iL_F - \frac{V_o}{R_L}\right] \tag{24}$$

Similarly, the switches $S_1 = S_2 = 1$ and $S_3 = 1$ or 0 as in Fig. 10:

$$\frac{diL_F}{dt} = \frac{V_g}{L_F} \tag{25}$$

$$\frac{dV_o}{dt} = \frac{1}{C_o}\left[-\frac{V_o}{R_L}\right] \tag{26}$$

By using state-space averaging method the state equations during switch-on and switch-off conditions are:

$$\dot{x}_1 = \frac{-(1-d_1)}{L_F} x_2 - \frac{(1-d_2)}{L_F} x_2 + \frac{V_g}{L_F} \quad (27)$$

$$\dot{x}_2 = \frac{-1}{R_L C_o} x_2 + \frac{(1-d_1)d_2}{C_o} x_1 + \frac{(1-d_1)(1-d_2)}{C_o} x_1 \quad (28)$$

where, x_1 and x_2 are the moving averages of i_{LF} and V_o respectively.

Procedure for constructing a proposed converter: Steps to obtain a system level modeling and simulation of proposed power electronic converter are listed below:

- Determine the state variables of the proposed power circuit in order to write its switched state-space model, e.g., inductance current and capacitance voltage.
- Assign integer variables (ON-1 and OFF-0 state) to the proposed power semiconductor to each switching circuit.
- Determine the conditions controlling the states of the proposed power semiconductors or the switching circuit.
- Assume the main operating modes, apply Kirchhoff's Current law and Kirchhoff's Voltage law and combine all the required stages into a switched state-space model, which is the desired system-level of the proposed model.
- Implement the derived equations with MATLAB SIMULINK.
- Use the obtained switched space-state model to design linear or nonlinear controllers for the proposed power converter.
- Perform closed-loop simulations and evaluate converter performance of proposed converter. The algorithm for solving the differential equations and the step size should be chosen before running any simulation. This step is only suitable in closed-loop simulations (Umamaheswari and Uma, 2013).

OPERATION OF PROPOSED BOOST CONVERTER WITH SNUBBER CIRCUIT

The proposed PFC is shown in Fig. 6 and it is based on a dual boost circuit where the first one (switch S_1 and choke L_{f1}) is used as main PFC circuit and where the second one (switch S_2 and choke L_{f2}) is used to perform an active filtering. The proposed PFC converter is obtained by adding ZVT-ZCT PWM active snubber circuit to the parallel boost converter. The proposed converter applies active snubber circuit for soft switching. This snubber circuit is mostly built on the ZVT turn-ON and ZCT turn-OFF processes of the main switches. Specification of parallel boost converter with active snubber is in Table 1.

Table 1: Specification of parallel boost converter with active snubber

Main inductor L_{f1}	750 µH
Main inductor L_{f2}	750 µH
Upper snubber inductor L_{R1}	5 µH
Lower snubber inductor L_{R2} (L_m+L_d)	2 µH
Magnetization inductor L_M (L_n+L_{0l})	3 µH
Parasitic capacitor C_s	1 µF
Snubber capacitor C_R	4.7 nF
Output capacitor C_o	330 µF/450V
Output load resistance R = R_L	530 Ω

The power from the ac main to the load flows through the two parallel paths. The main path is a rectifier, where power is not processed twice for PFC, but the other path processes the input power twice for PFC purpose. To attain both unity power factor and tight output voltage regulation, only the difference among the input power and output power needs to be processed twice. Thus, high efficiency can be found by this method. So as to reach Soft Switching (SS) for the main and the auxiliary switches, main switches turn on with ZVT and turn off with ZCT. The proposed converter utilizes active snubber circuit for SS. This snubber circuit is mostly based on the ZVT turn-ON and ZCT turn-OFF processes of the main switch. C_S capacitor is the addition of the parasitic capacitors of the main switch S_1 and the main diode D_f. L_{R2} value is limited with $(V_{out}/L_{R2})\ t_{riseS2} \leq I_{imax}$ to conduct maximum input current at the end of the auxiliary switch rise time ($t_{rise}S_2$) and $L_{R1} \geq 2L_{R2}$. To turn OFF S_1 with ZCT, the duration of t_{ZCT} is at least longer than fall time of S_1 ($t_{fall}S1$) $t_{ZCT} \geq t_{fall\_S1}$. Though the main switches are in OFF state, the control signal is functional to the auxiliary switch. The parasitic capacitor of the main switch should be discharged absolutely and the main switches anti parallel diode should be turned ON. The ON-state time of the anti parallel diode is named t_{ZVT} and in this time period, the gate signal of the main switch would be applied. So, the main switch is turned ON below ZVS and ZCS with ZVT.

Whereas the main switches are in ON state and ways input current, the control signal of the auxiliary switch is applied. After the resonant starts, the resonant current should be higher than the input current to turn ON the anti-parallel diode of the main switch. The ON-state time of the anti-parallel diode (t_{ZCT}), has to be longer than the main switches fall time (t_{fS1}). After all these terms are completed, while anti-parallel diode is in ON state, the gate signal of the main switch should be cutoff to provide ZCT for the main switch. Auxiliary switch turn ON with ZCS and turn OFF with ZCS. The auxiliary switch is turned ON with ZCS for the coupling inductance limits the current rise speed.

The current pass through the coupling inductance, must be partial to conduct maximum input current at the end of the auxiliary switch rise time (t_{rS3}). So, the turn-ON process of the auxiliary switch with ZCS is offered. To turn OFF the auxiliary switch with ZCS, though the auxiliary switch is in ON state, the current pass complete the switch should fall to zero with a new resonant. Then, the control signal can be cutoff. If C_S is ignored, L_{R1} value should be two times added than L_{R2}

to fall the auxiliary switch current to zero. As the current cannot stay at zero as long as the auxiliary switch fall time (t_{fS3}), the auxiliary switch is turned OFF nearly with ZCS.

MATLAB simulation for proposed converter with active snubber: The proposed SIMULINK topology is shown in Fig. 11. The inductors L_{f1} and L_{f2} have the similar values, the diodes D_{f1}-D_{f2} are the same type and the same guess was for the switches (S_1 and S_2). All inductor has its individual switch and thus it's like with the paralleling of both single/classic converters.

RESULTS AND DISCUSSION

A modular single phase ac-dc converter using parallel boost converter of the proposed system is simulated using MATLAB SIMULINK program. The waveforms of V_{in} and I_{in} of the converter is shown in Fig. 12 and 13. The output dc voltage (V_o) is shown in

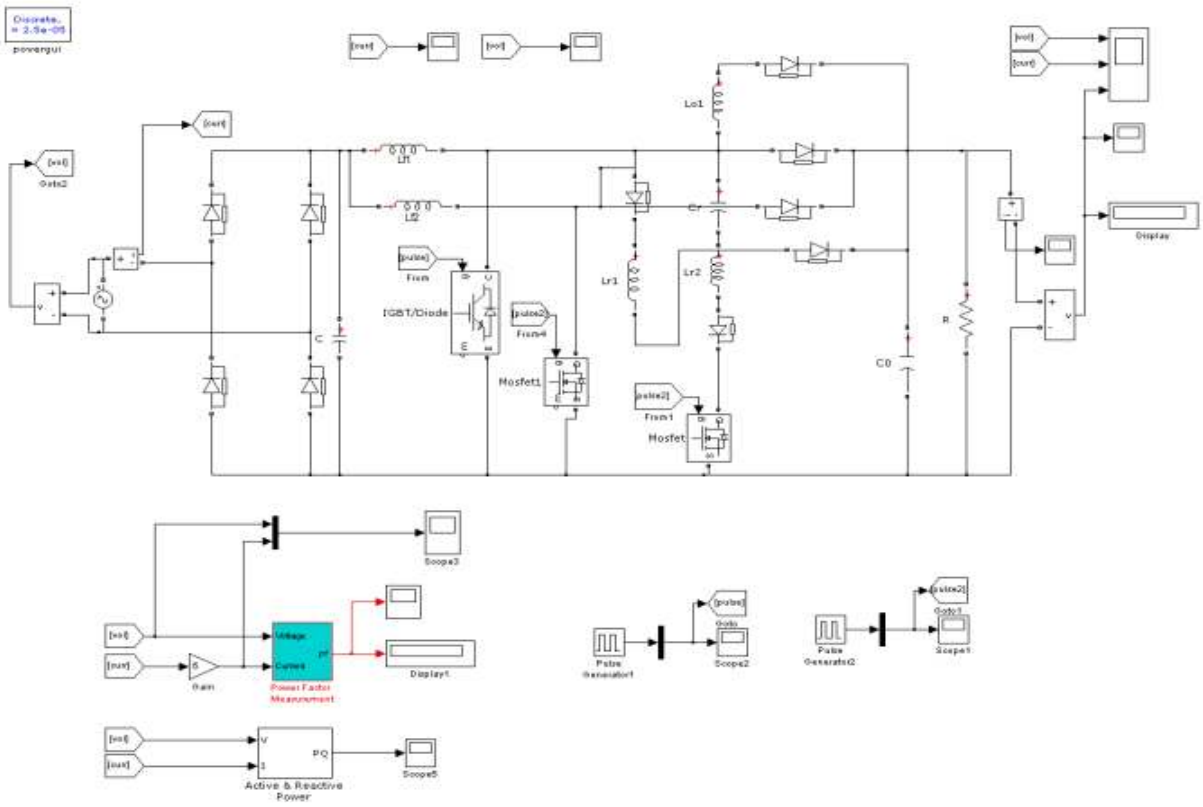

Fig. 11: SIMULINK model of proposed PFC boost converter with snubber circuit

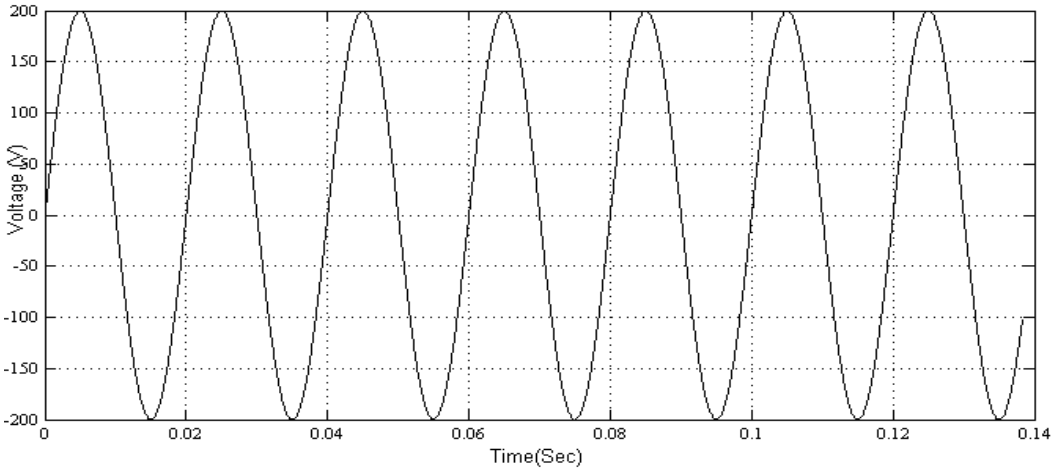

Fig. 12: Input voltage of proposed boost converter with active snubber circuit

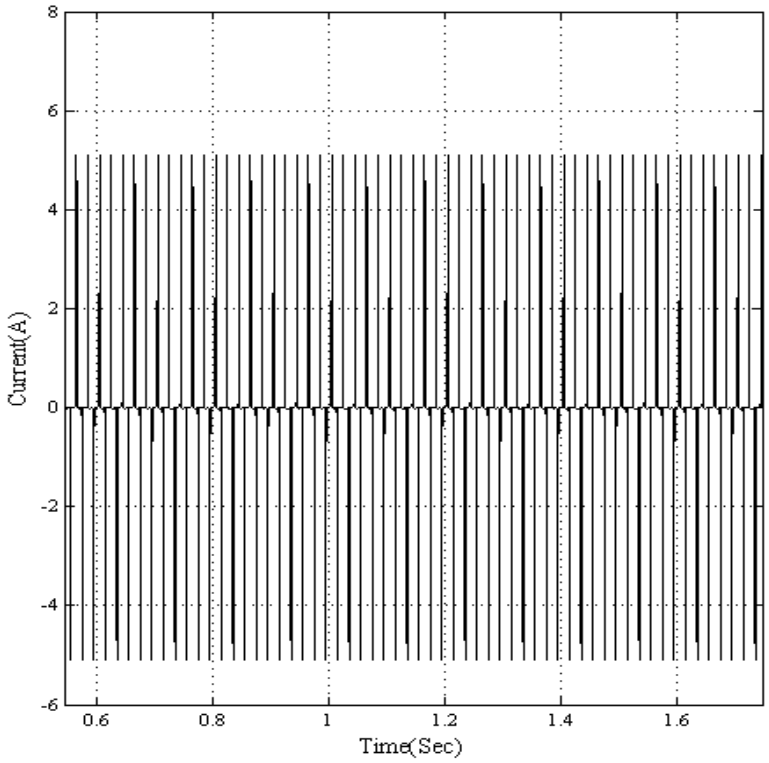

Fig. 13: Input current of proposed boost converter with active snubber circuit

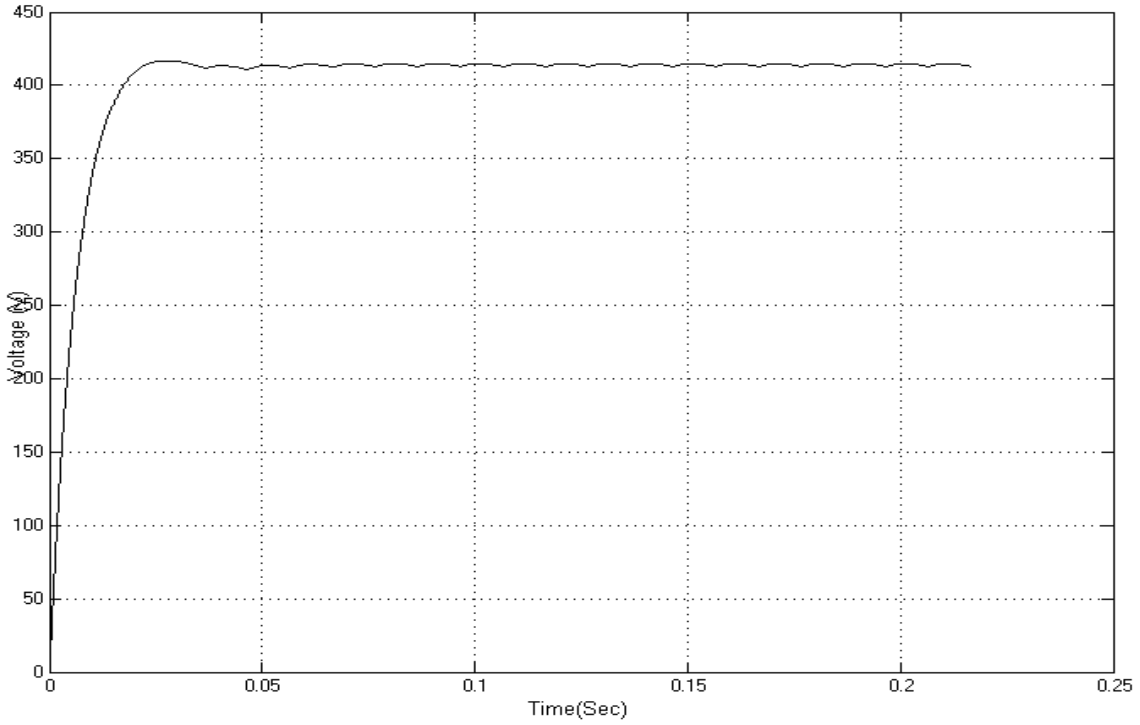

Fig. 14: Output voltage (Vo = 420V)

Fig. 14. The waveform of power factor is shown in Fig. 15. The combined input and output voltage is shown in Fig. 16 and the control signals of the switches are shown in Fig. 17 and 18, respectively. The simulation results show the proposed soft switched parallel boost ac-dc converter has the proper response.

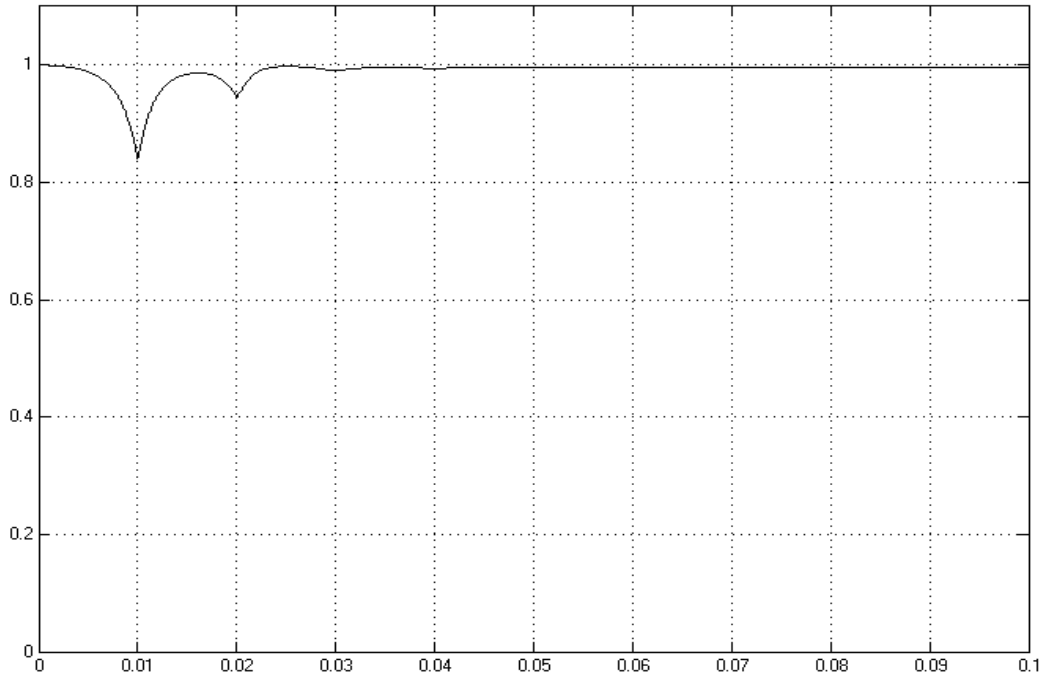

Fig. 15: Power factor (PF = 0.997)

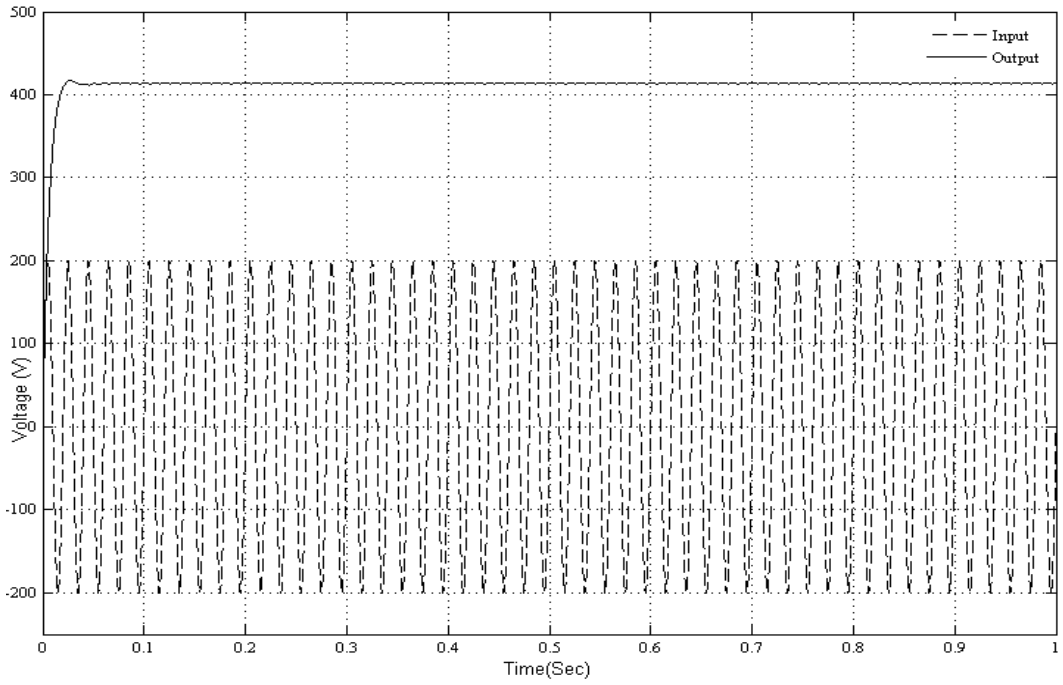

Fig. 16: Input voltage and output voltage (Vin = 200v and Vo = 420V)

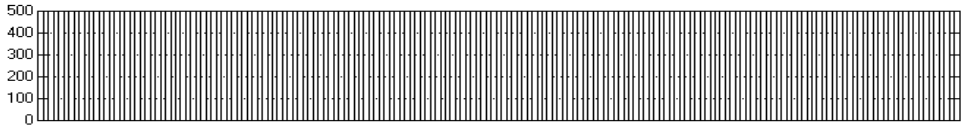

Fig. 17: Control signals of switch S3

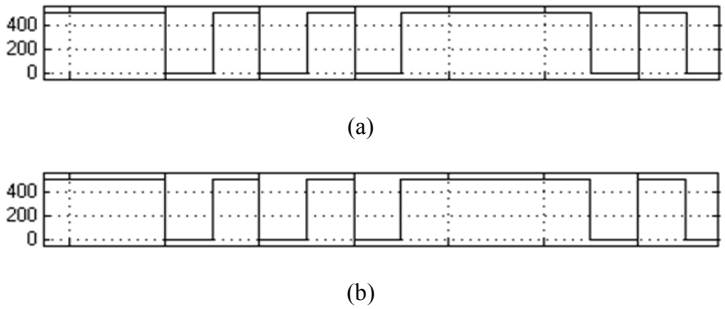

Fig. 18: Control signals of switches S1, S2

Table 2: A summary of system performance parameters for parallel boost converter

Type of output dc voltage (constant, variable, etc.)	Constant
Power flow (unidirectional and bidirectional)	Unidirectional
Input voltage	200 V
Line frequency	50 Hz
Number of switches	3
Nature of dc output (isolated, non-isolated)	Isolated
DC output (buck, boost and buck-boost)	Boost (420 V)
Type of dc loads (linear, non-linear, etc.)	Non-linear
Power factor	99.7%
Efficiency	98%
Rating (W, kW, MW, etc.)	340 W
Load resistance	530 Ω

Finally the overall system performance of proposed parallel boost converter is shown in Table 2.

CONCLUSION

The main objective of this study was to improve the power factor with active snubber circuit for the parallel boost converter. Simulations were initially done for conventional boost converter with snubber circuit. The changes in the input current waveform were obtained. A PFC circuit having a parallel boost converter was designed with soft switching which is provided by the active snubber circuit. For this idea, only one auxiliary switch and one resonant circuit was operated. The main switches and all the other semiconductors were switched by ZVT and ZCT techniques. The active snubber circuit was applied to the parallel boost converter, which is fed by rectified universal input ac line. This latest PFC converter was achieved with 200 V ac input mains. The diode was added in order to the auxiliary switch path to avoid the incoming current stresses as of the resonant circuit to the main switch. It was noticed that the Power Factor and the efficiency is better for Dual Boost Converter Circuit. Finally, 98% efficiency at full load was achieved and the power factor was reached to 99.7% for the proposed converter. Due to the main and the auxiliary switches have a common ground, the converter was controlled easily. The proposed new active snubber circuit can be simply functional to the further basic PWM converters and to all switching converters.

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