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Research Article

Design of A Novel 8-point Modified R2MDC with Pipelined Technique for High Speed OFDM Applications

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Abstract: This study presents, design of modified R2MDC with pipelined Technique. Radix-2 Multipath Delay commutators is the one type of Radix-2 FFT. Wireless networks have found a significant place in the growing technologies. Orthogonal Frequency Division Multiplexing (OFDM) is a key technique used in wireless networks for high speed operation, high data capacity and spectral efficiency. The Fast Fourier Transform (FFT) are essential in the field of Digital Signal Processing (DSP), widely used in communication systems, especially in Orthogonal Frequency Division Multiplexing (OFDM) systems. Not a lot of research has been done on modified R2MDC FFT in OFDM. In this study, we propose a modified R2MDC 8-Point FFT in which pipelining technique is used in each Butterfly unit architecture. Using this technique through VLSI simulations it is found to reduce the delay and increase the throughput and hence is suitable for OFDM. This method can be extended to OFDM implementation that is apt for Wireless Networks.

Keywords: FFT, MIMO OFDM, R2MDC, VLSI, wireless networks

INTRODUCTION

The Fast Fourier Transform (FFT) are essential in the field of Digital Signal Processing (DSP), widely used in communication systems, especially in Orthogonal Frequency Division Multiplexing (OFDM) systems, wireless-LAN, WiMAX, ADSL and VDSL systems (Lin *et al*., 2005). Apart from the applications, the system demands high speed of operation, low power consumption, reduced truncation error and reduced chip size of Fast Fourier Transform (FFT) is one of the mathematical concept that can be implemented in real time applications, it can be capable of converting the data from one form to the other form i.e.; frequency domain to time domain and vice versa. OFDM can be utilized in most of the practical day to day life applications that makes the OFDM as one of the most converging technique (Pradeepa and Gowtham, 2012). There are two types of FFT structures:

- Decimation in time
- Decimation in frequency

And there are different types of FFT architectures and they are (Sang-In *et al*., 2008):

- Radix-2
- Radix-4
- Mixed radix
- Split radix

These four types of architectures can be used and each having its unique operations and functions.

In our paper we describe the Fast Fourier transform with two different architectures that can be operated with OFDM; we proposed modified R2MDC architecture with pipelined technique in Fast Fourier transform that shows less delay and high frequency.

Radix-2 algorithm: The radix-2 algorithm is a special case of the common factor algorithm for N-point DFTs, where N is power-of-2. To derive the radix-2 algorithm, the indices n and k in Eq. (1) are represented by Cooley and Tukey (1965) (Fig. 1):

$$n = 2^{\alpha-1}.\mathrm{n}_{\alpha-1} + 2^{\alpha-2}.\mathrm{n}_{\alpha-2} + \ldots + n_0 - \sum_{\beta=0}^{\alpha-1} 2^{\beta}.\mathrm{n}_{\beta}$$

$$k = 2^{\alpha-1}.\mathrm{k}_{\alpha-1} + 2^{\alpha-2}.\mathrm{k}_{\alpha-2} + \ldots + k_0 - \sum_{\beta=0}^{\alpha-1} 2^{\beta}.\mathrm{k}_{\beta} \quad n_i, k_i \in \{0,1\}, \mathrm{i} = 0 \ldots \alpha - 1 \tag{1}$$

where,

$$N = 2^{\alpha} \quad \alpha \in N$$

Types of Radix2 FFT:

- Radix-2 Single Path Delay Feed back
- Radix-2 Single Path Delay Commutator
- Radix-2 Multipath Delay Commutator (R2MDC)

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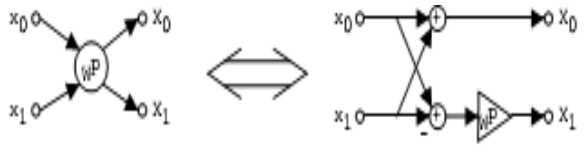

Fig. 1: Structure of a radix-2 DIF butterfly

Radix-2 Multipath Delay Commutator (R2MDC): Features of Radix-2 Multipath Delay Commutator (R2MDC) are:

- The most classical approach for pipeline implementation of radix-2 FFT
- Input sequence broken into two parallel data streams flowing forward with correct "distance "between data elements entering the butterfly scheduled by proper delays
- Both butterflies and multipliers are in less utilization

The Block Diagram of Radix-2 Multipath Delay Commutator (R2MDC) is consists of Butterfly (BF2) architecture, Delay unit and commutator block. One of the most straightforward approaches for pipeline implementation of radix-2 FFT algorithm is Radix-2 Multipath Delay Commutator (R2MDC) architecture it's the simplest way to rearrange data for the FFT/IFFT algorithm. The input data sequence are broken into two parallel data stream flowing forward, with correct distance between data elements entering the butterfly scheduled by proper delays (Gin-Der and Ying, 2006).

The 8-point FFT in R2MDC architecture is shown in Fig. 2. In R2MDC architecture, at each stage, half of the dataflow is delayed via the memory element and processed with the second half of data flow. The delay for each stage is 4, 2 and 1, respectively. The total number of delay elements is 4+2+2+1+1 = 10. In this Radix 2 Multipath Delay Commutator (R2MDC) architecture, both Butterflies (BF) and multipliers are idle half the time waiting for the new inputs. The 8-point FFT/IFFT processor has one multiplier, 3 of radix-2 butterflies, 10 Registers (R) (delay elements) and 2 Switches (S).

PROPOSED METHODOLOGY

Fast Fourier Transform is a high efficient algorithm to compute the DFT. The basic idea of this approach is to decompose the N-point DFT into successively smaller DFT. This approach leads to highly efficient computation of FFT algorithm (Nirmal Kumar and Santhosh, 2013). The reconfigurable FFT facilitates the efficient Transformation between the time domain and the frequency domain for a sampled signal. Various FFT processors can be used for hardware implementation. These implementations can be mainly classified into memory-based and pipeline architecture styles (Mounir *et al*., 2010).

In order to overcome the disadvantages of the memory based architecture style, we go for pipeline based architecture style. For a pipelined FFT processor, each and every stage has its own set of processing elements.

This entire methodology quickens the processes to a great extent and hence found a significant part in most OFDM systems. In the proposed reconfigurable scheme, pipeline technique is applied to modified R2MDC architectures in order to reduce the delay and also to increase the frequency (Deepa and Sarada, 2013).

In the physical layer of the IEEE 802.11n standard, the Fast Fourier Transform (FFT) /Inverse Fast Fourier Transform (IFFT) processor are highest computationally complex modules. However to increase the signal processing capability, to reduce the power consumption and to reduce the hardware cost, FFT processor have challenging targets (Sneha and Meghana, 2011). This paper present a pipelined Fast Fourier Transform (FFT) /Inverse Fast Fourier Transform (IFFT) processor for MIMO OFDM based IEEE 802.11n WLAN baseband processor is presented. High throughput and delay reduction are achieved by using novel R2MDC-FFT in MIMO-OFDM (Kosher *et al*., 2004). In the proposed modified FFT/IFFT with pipelined architecture reduces the delay and increase the throughput.

In the proposed scheme shown in the Fig. 3, pipeline technique is applied to modified R2MDC architectures in order to reduce the delay and also to

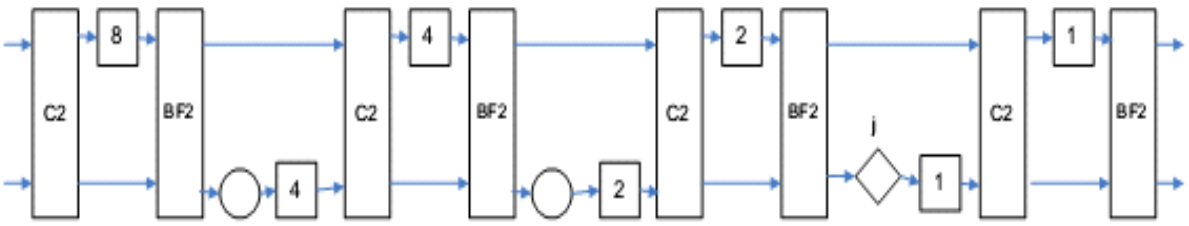

Fig. 2: Block diagram of Radix-2 Multipath Delay Commutator (R2MDC)

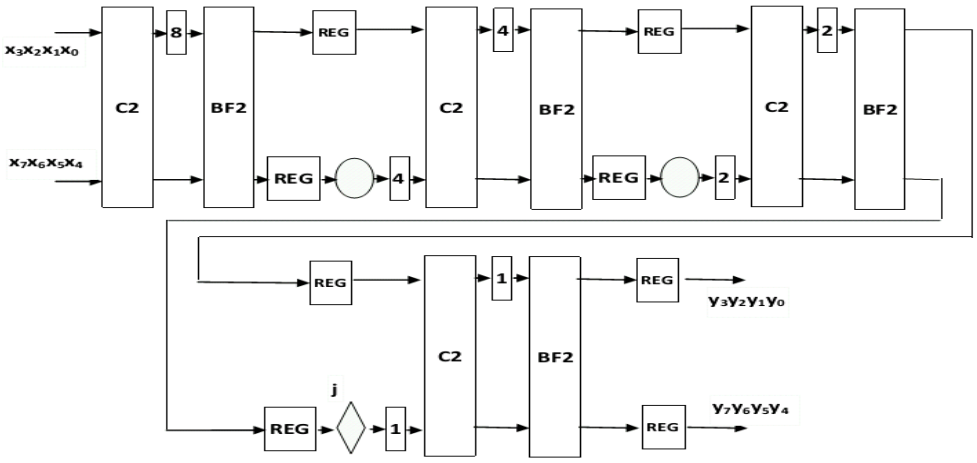

Fig. 3: Block diagram of modified Radix-2 Multipath Delay Commutator (R2MDC) with pipelined technique

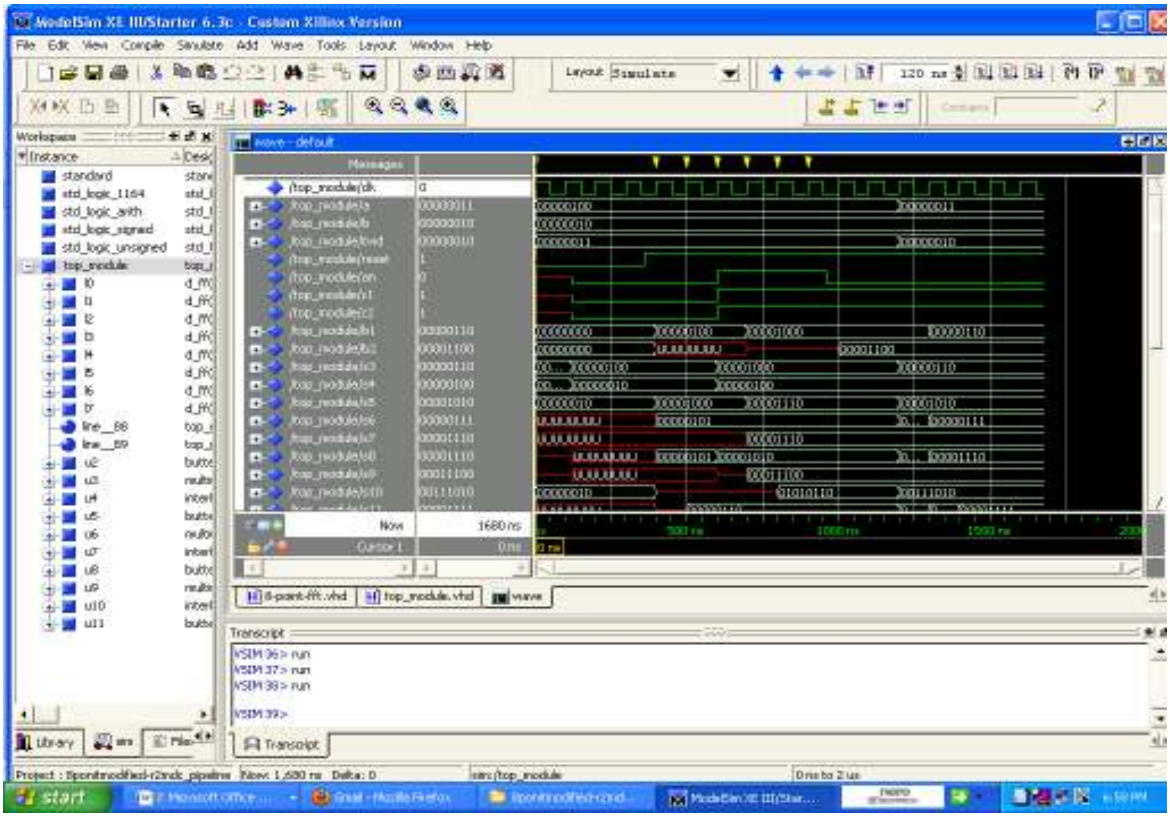

Fig. 4: Simulation results of modified R2MDC with pipelined technique

increase the frequency. In the modified R2MDC block a Register unit is included after the every butterfly unit; hence it is called modified R2MDC with pipelined technique. The modified R2MDC blocks can be used in the OFDM or MIMO OFDM technique. It is vital to notice that pipelining is a part of all the FFT blocks. This will reduce the delay; Simulation is performed to get the analysis.

The proposed Modified R2MDC with pipelined technique based architecture consist of Commutate, Butterfly unit, register unit, multiplier unit and inter block unit are presented. Two point R2MDC butterfly unit is processed based on twiddle factors c1 and c2 values. Different combinations of inputs were given to get the various outputs as listed below:

- x1 = 4, x2 = 2; c1 = 0 and c2 = 0 or c1 = 0 and c2 = 1; gave the output y1 = x1 and y2 = x2
- x1 = 4, x2 = 2; c1 = 1 and c2 = 0 or c1 = 1 and c2 = 1; gave the output y1 = 2* (x1) and y2 = 2*x2

Here 4 butterfly stages are used. Every stage follows the same condition. Inter block consist of mux, adder and sub-tractor. If the input x and twiddle factor $a_n = 0$, the output y = x+1. But $a_n = 1$, the output y = x. register unit is used to store the values. Based on the functionality of every block, the output is performed at every stage. Simulation result of 8 point R2MDC with pipelined techniques is shown in Fig. 4.

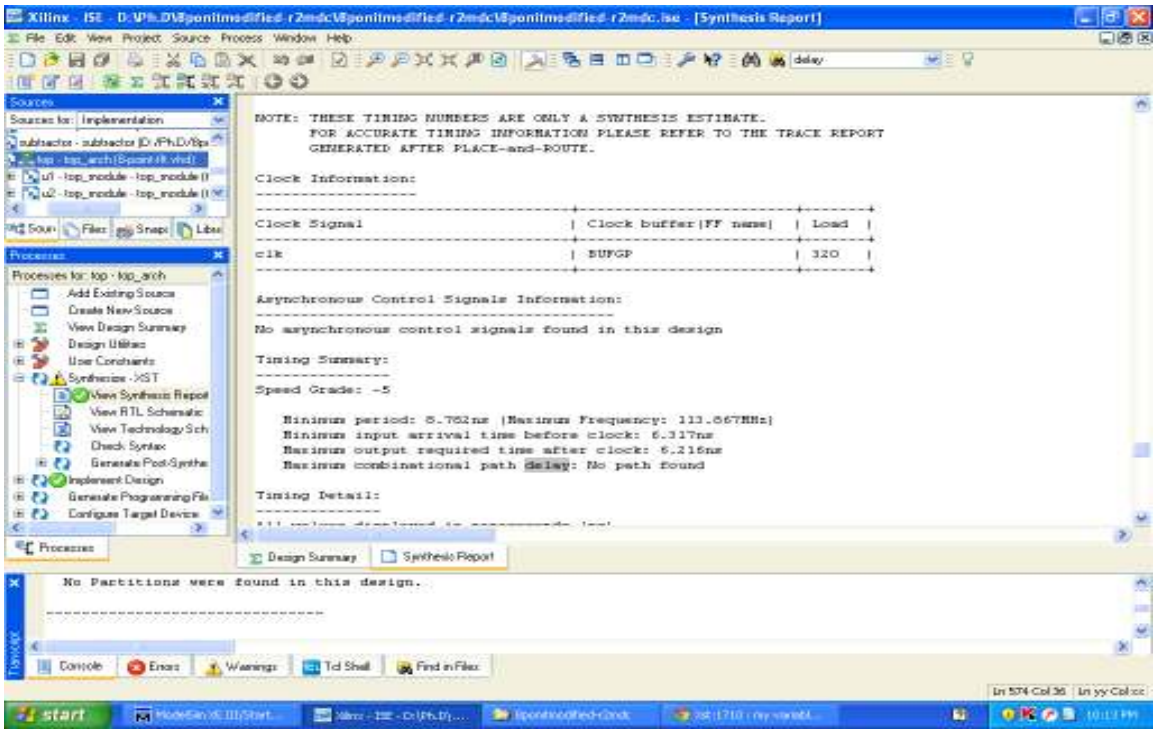

Fig. 5: Synthesis results of modified R2MDC with pipelined technique for delay utilization

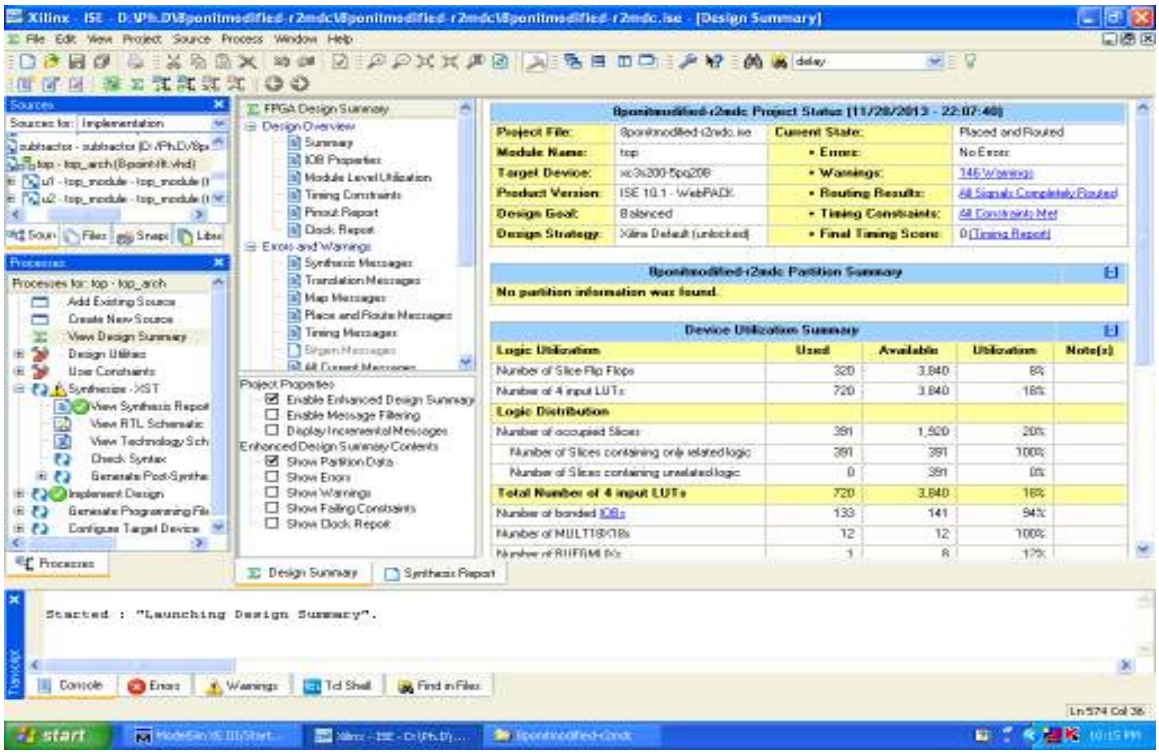

Fig. 6: Synthesis results of modified R2MDC with pipelined technique for area utilization

Table 1: Comparison between R2MDC with pipelined and without pipelined technique

FFT	Delay (NS)	Slices
Modified R2MDC without pipelined	32.230	369
Modified R2MDC with pipelined	7.451	391

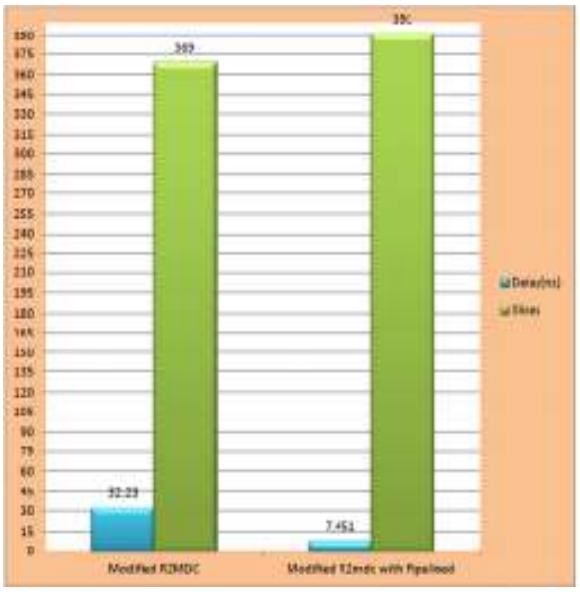

Fig. 7: Performance analysis of modified R2MDC with pipelined and without pipelined techniques

RESULTS AND DISCUSSION

The simulation is carried out by Modelsim 6.3c and Synthesis is carried out by Xilinx10.1. The proposed scheme provides less delay and high throughput utilization. This modified FFT architecture is applied in MIMO OFDM for WiMax in order to increase the throughput and Frequency of the wireless Networks.

The modified R2MDC without pipelined and proposed modified R2MDC with pipelined 8 point FFT are designed using VHDL. From the synthesized result shown in Fig. 5 and 6, the modified R2MDC without pipelined technique consumes 32.230 ns of delay and the proposed modified R2MDC with pipelined technique consumes 7.451 ns of delay. The proposed modified R2MDC with pipelined, delay are reduced by 70% compared to the conventional modified R2MDC without pipelined. So the throughput of proposed R2MDC FFT is increased than the conventional R2MDC FFT Table 1 shows comparison between R2MDC with pipelined and without pipelined Technique. The area of proposed R2MDC FFT is increased due to include the register in various stages for pipelined techniques. Figure 7 shows Performance analysis of Modified R2MDC with Pipelined and without pipelined techniques.

CONCLUSION

This paper presents a novel R2MDC 8Point FFT in which pipelining technique was used after the each butterfly unit architecture. Using this technique through VLSI simulations it was found to reduce the delay and increase the frequency and hence it is suitable for MIMO OFDM. This method can be extended to OFDM implementation that is apt for Wireless Networks. Finally, this new MIMO OFDM can be used in 4G and 5G wireless networks for high speed data transmissions.

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