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Research Article

Proportional-integral Control for SEPIC Converter

[1]S. Venkatanarayanan and [2]M. Saravanan
[1]Department of EEE, K.L.N. College of Engineering, Pottapalayam, Sivagangai District, India
[2]Department of EEE, Thiagarajar College of Engineering, Madurai, India

Abstract: The object of this study is to design and analyze a Proportional-Integral (PI) control for SEPIC, which is the start-of-the-art DC-DC converter. The single Ended Primary Inductor converter performs the voltage conversion from positive source voltage to positive load voltage. This study proposes a development of PI control capable of providing the good static and dynamic performance compared to Proportional-Integral Derivative (PID) controller. Using state space average method derives the dynamic equations describing the SEPIC converter and PI control is designed. The simulation model of the SEPIC converter with its control circuit is implemented in MATLAB/SIMULINK. The PI control for SEPIC is tested for transient region, line changes, load changes, steady state region and also for components variations.

Keywords: DC-DC converter, Proportional-Integral (PI) control, Single Ended Primary Inductor Converter (SEPIC)

INTRODUCTION

DC-DC conversion technology has been developing very rapidly and DC-DC converters have been widely used in industrial applications such as dc motor drives, computer systems and communication equipments. The output voltage of Pulse Width Modulation (PWM) based DC-DC converters can be changed by changing the duty cycle. The Single Ended Primary Inductor (SEPIC) is a series of DC-DC converters possessing high-voltage transfer gain, high power density; high efficiency, reduced ripple voltage and current (Middlebrook and Cuk, 1977). These converters are widely used in computer peripheral equipment, industrial applications and switch mode power supply (Comines and Munro, 2002). Control for them needs to be studied for the future application of these good topologies. The SEPIC increases the voltage transfer gain stage by stage in geometric progression (Fang and Hong, 2004; Katsuhiko, 2005). However, their circuits are complex. An approach, SEPIC converters, that implements the output voltage increasing in geometric progression with a simple structured have been introduced. These converters also effectively enhance the voltage transfer gain in power-law (Kanaan *et al*., 2009). Due to the time variations and switching nature of the power converters, their static and dynamic behavior becomes highly non-linear. The design of high performance control for them is a challenge for both the control engineers and power electronics engineers. In general, a good control for DC-DC converters always ensures stability in arbitrary operating condition. Moreover, good response in terms of rejection of load variations, input voltage variations and even parameter uncertainties is also required for a typical control scheme. The static and dynamic characteristics of these converters have been well discussed in the literature (Namnabat *et al*., 2007). With different state-space averaging techniques, a small-signal state-space equation of the converter system could be derived. The Proportional Integral Derivative (PID) controller's recent tuning methods and design to specification has been well reported in the literature (Aggarwal *et al*., 2006). The PI control technique offers several advantages compared to PID control methods: stability, even for large line and load variations, reduce the steady error, robustness, good dynamic response and simple implementation. Intensive research in the area of DC-DC converter has resulted in novel circuit topologies (Rodriguez *et al*., 2005). These converters in general have complex non-linear models with parameter variation. The averaging approach has been one of the most widely adopted modeling strategies for switching converters that yields a simple model (Kumar and Jeevananthan, 2011). Analysis and control design of paralleled DC-DC converters with master-slave current sharing control has been well reported (Alonso *et al*., 2008).

In this study, state-space model for Single Ended Primary Inductor Converter (SEPIC) are derived at first. A PI control with zero steady state error and fast response is brought forward. The static and dynamic performance of PI control for SEPIC converter is studied in MATLAB/SIMULINK. Details on operation,

Corresponding Author: S. Venkatanarayanan, Department of EEE, K.L.N. College of Engineering, Pottapalayam, Sivagangai District, India

analysis, control strategy and simulation results for SEPIC are presented in the subsequent sections.

CONVERTER OPERATION AND MODELING SEPIC

For the purpose of optimize the stability of SEPIC converter dynamics, while ensuring correct operation in any working condition, a PI control is a more feasible approach. The PI control has been presented as a good alternative to the control of switching power converters. The main advantage PI control schemes is its insusceptibility to plant/system parameter variations that leads to invariant dynamics and static response in the ideal case.

Circuit description and operation: Single-Ended Primary-Inductor Converter (SEPIC) is a type of DC-DC converter allowing the voltage at its output to be greater than, less than, or equal to that at its input. The output of the SEPIC is controlled by the duty cycle of the control transistor. A SEPIC has a advantages of having non-inverted output, using a series capacitor to couple energy from the input to the output and thus can respond more gracefully to a short-circuit output and being capable of true shutdown: when the switch is turned off, its output drops to 0 V, following a fairly hefty transient dump of charge.

SEPICs are useful in applications in which a voltage can be above and below that of the regulator's intended output. As with other switched mode power supplies, the SEPIC exchanges energy between the capacitors and inductors in order to convert from one voltage to another. The amount of energy exchanged is controlled by switch S, which is typically a transistor like MOSFET, IGBT etc. MOSFETs offer much higher input impedance and lower voltage, do not require biasing resistors. MOSFET switch is controlled by differences in voltage rather than a current.

A power circuit diagram of the SEPIC shown in Fig. 1. It includes DC input supply voltage V_{in}, the capacitors C_1, C_2 the inductors L_1 L_2, the switch S (MOSFET), the diode D and the load resistance R. It is assumed that the components are ideal and also SEPIC operates in CCM. Figure 2 and 3 shows the modes of operation of the SEPIC.

In Fig. 2, when the switch s is closed, the diode open, the Inductor L_1 occupied by the source voltage V_{in}, the L_2 charges to the capacitor C_1, the polarity of the inductor current and, capacitor shown in Fig. 2. The equation can be obtained from this condition:

$$V_{in} = V_{L1ON} \tag{1}$$

V_{L1ON} is the voltage of the inductor L_1 when the switch is ON condition.

In the Fig. 3 when the switch is open, diode D is closed, Inductor L_1 charges the capacitor C_1 and the Inductor L_2 provide the load current, at this time the equation can be obtained is:

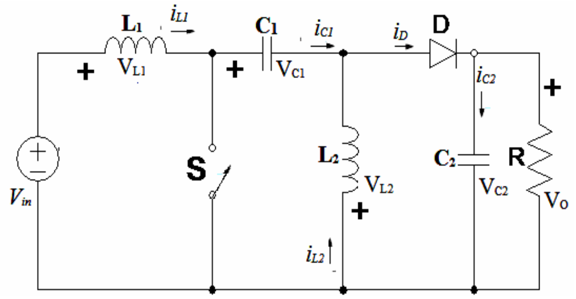

Fig. 1: Basic SEPIC converter

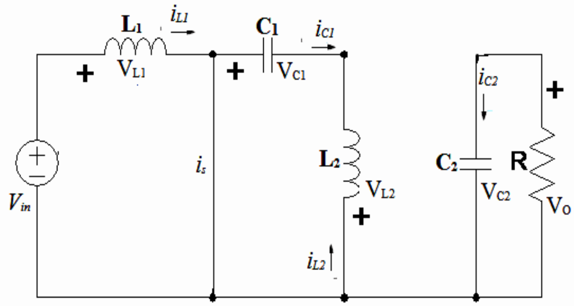

Fig. 2: SEPIC converter during switch on

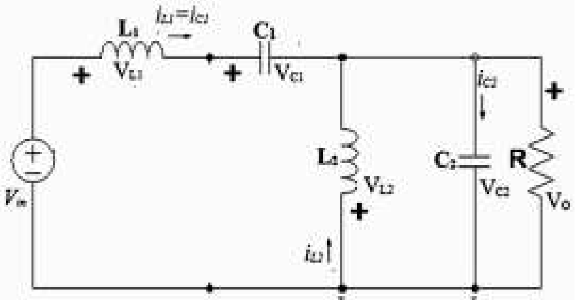

Fig. 3: SEPIC converter during switch off

$$V_{L1SOFF} = Vo \tag{2}$$

V_{L1SOFF} is voltage of Inductor L1 when the switch is open. Using the voltage-time analysis the equation can be obtained as:

$$V_{L1SON}\,(dT) + V_{LSOFF}\,(1 - dT) = 0 \tag{3}$$

State space modeling:

The state variables: The state space variables of a SEPIC are take as currents $i_{L_1}$and i_{L_2}, the voltages V_{C_1} and V_{C2} respectively when the switch is closed, the state space equation can be obtained as:

$$\begin{cases} i_{L1} = \frac{-1}{L_1} + \frac{V_{in}}{L_1} \\ i_{L2} = \frac{-1}{L_2} - \frac{1}{L_2} \\ V_{C1} = \frac{V_{C1}}{C_1} \\ V_{C2} = \frac{1}{C_2} - \frac{1}{C_2} - \frac{V_{C2}}{RC_2} \end{cases} \tag{4}$$

$$\frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \\ v_{c1} \\ v_{c2} \end{bmatrix} = \begin{vmatrix} \frac{-1}{L_1} & 0 & 0 & 0 \\ 0 & \frac{-1}{L_2} & \frac{-1}{L_2} & 0 \\ 0 & \frac{1}{C_1} & 0 & 0 \\ \frac{1}{C_1} & -\frac{1}{C_2} & 0 & \frac{-1}{RC_2} \end{vmatrix} \begin{bmatrix} i_1 \\ i_2 \\ v_{c1} \\ v_{c2} \end{bmatrix} + \begin{bmatrix} i_1 \\ 0 \\ 0 \\ 0 \end{bmatrix} v_{in} \quad (5)$$

During on:

$$\begin{cases} i_{L1} = \frac{-1}{L_1} i_1 + \frac{v_{in}}{L_1} \\ i_{L2} = \frac{-R_2}{L_2} i_2 + \frac{1}{L_2} v_o \\ V_{C1} = \frac{i_1}{C_1} \\ V_{C2} = \frac{i_1}{C_2} - \frac{i_2}{C_2} - \frac{v_2}{RC_2} \end{cases} \quad (6)$$

$$V = AX + B\gamma \quad (7)$$

By using state space averaging method, the state space averaging model of SEPIC is given as:

$$\frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \\ v_{c1} \\ v_{c2} \end{bmatrix} = \begin{vmatrix} \frac{-1}{L_1} & 0 & \frac{-(1-d)}{L_1} & \frac{-(1-d)}{L_1} \\ 0 & \frac{-1}{L_2} & \frac{-d}{L_2} & \frac{1-d)}{L_2} \\ \frac{(1-d)}{C_1} & \frac{d}{C_1} & 0 & 0 \\ \frac{(1-d)}{C_2} & \frac{(1-d)}{C_2} & 0 & \frac{-1}{RC_2} \end{vmatrix} \begin{bmatrix} i_1 \\ i_2 \\ v_{c1} \\ v_{c2} \end{bmatrix} + \begin{bmatrix} i_1 \\ 0 \\ 0 \\ 0 \end{bmatrix} v_{in} \quad (8)$$

The output voltage:

$$V_{C2} = V_0 \quad (9)$$

where, V_o is the output voltage of SEPIC converter.

The PI control is designed to ensure the specifying desired nominal operating point for SEPIC, then regulating SEPIC, so that it stays very closer to the nominal operating point in the case of sudden disturbances, set point variations, noise, modeling errors and components variations. The PI control settings proportional gain (*Kp*) and integral Time (*Ti*) are designed using Zeigler-Nichols tuning method (Katsuhiko, 2005; Fang and Hong, 2004). By applying the step test to (8) and (9) to obtain S-shaped curve of step response of SEPIC as shown in Fig. 4. From the S-shaped curve of step response of SEPIC may be characterized by two constants, delay time L = 0.005 sec and time constant T = 0.052 sec. The delay time and time constant are determined by drawing a tangent line at the inflection point of the S-shaped curve and determining the intersections of the tangent line with the time axis and line output response U (t) as shown in Fig. 4. Ziegler and Nichols suggested to set the values of *Kp* = 9.36 and *Ti* = 0.016 sec according to the Table 1. The PI control optimal setting values (*Kp* and *Ti*) for POELC are obtained by finding the minimum values of Integral of Square of Error (ISE), Integral of Time of square of Error (ITAE) and Integral of Absolute of Error (IAE), which is listed in Table 2. The SIMULINK model of block of PI control section and its transfer function model are shown in Fig. 5. Error in output voltage and change in duty cycle of the power switch *S* (n-channel MOSFET) is, respectively the input and output of the PI control.

Table 1: Ziegler and nichols

Types of controller	Kp	Ti	Td
P	$\frac{T}{L}$	∞	0
PI	$\frac{0.9T}{L}$	$\frac{L}{0.3}$	0
PID	$\frac{1.2T}{L}$	2 TL	0.5 TL

Table 2: Parameters of SEPIC

Specification/parameter	Unit/symbol	Value/quantity
Input voltage	Vi	10
Output voltage Vo 36V	Vo	48
Inductor	L1, L2	1100 µH
Capacitors	C1, C2	5 µF, 30 µF
Nominal switching frequency	f_s	100 kHz
Load resistance	R	60 Ω
Range of duty cycle	d	0.3 to 0.9
Desired duty cycle	d	0.5

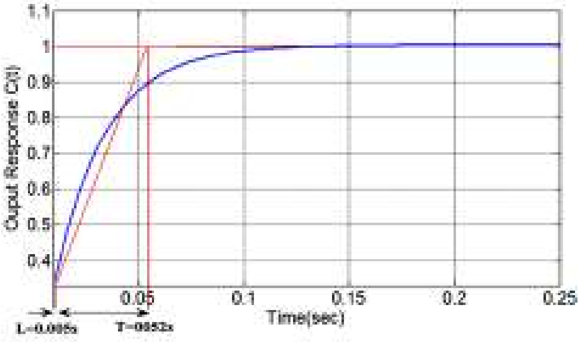

Fig. 4: Step response of SEPIC

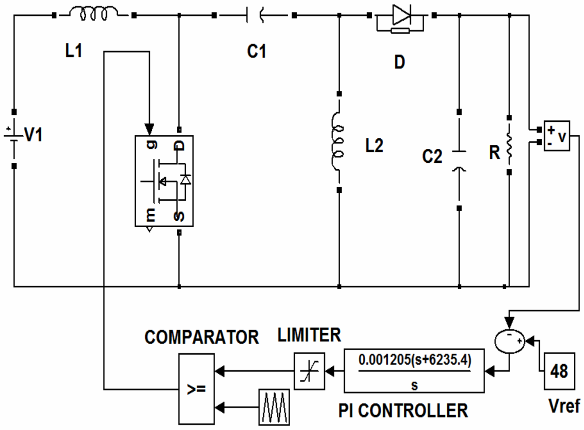

Fig. 5: MATLAB SIMULINK simulation model

SIMULATION STUDY

The validation of the system performance is done for five regions viz. transient region, line variations, load variations, steady state region and also components variations. Simulations has been performed on the SEPIC converter circuit with parameters listed in Table 2. The static and dynamic performance of PI control for the SEPIC is evaluated in MATLAB/SIMULINK. The MATLAB/SIMULINK simulation model is depicted in Fig. 5. It can be seen that error in outputs voltage of the power switch (MOSFET) of PI control input is obtained by the difference between feedback output voltage and feedback reference output voltage and output of PI control, change in duty cycle of the power switch (MOSFET).

Transient region: Figure 6 and 7 shows the output voltage and the inductor current of PI with SEPIC in the transient region.

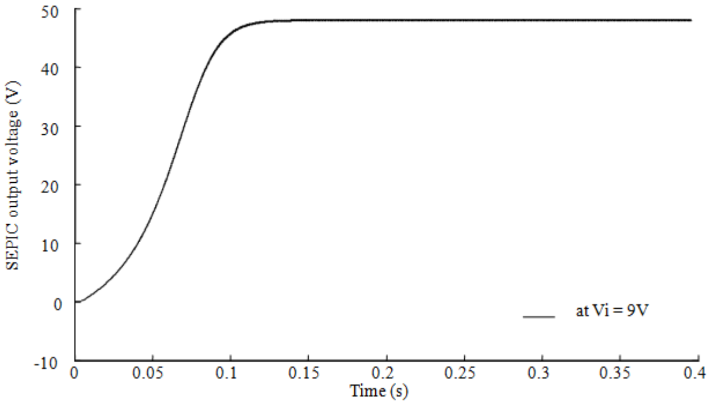

Fig. 6: Shows the output voltage at Vin = 9V

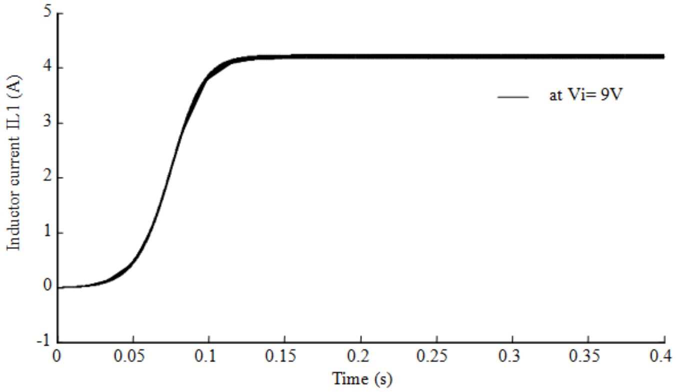

Fig. 7: Shows the inductor current at Vi = 9V

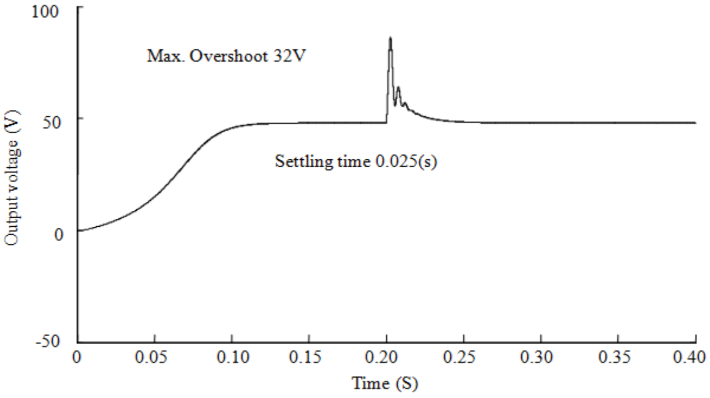

Fig. 8: Output voltage when input takes a step change from 10 to 16 V

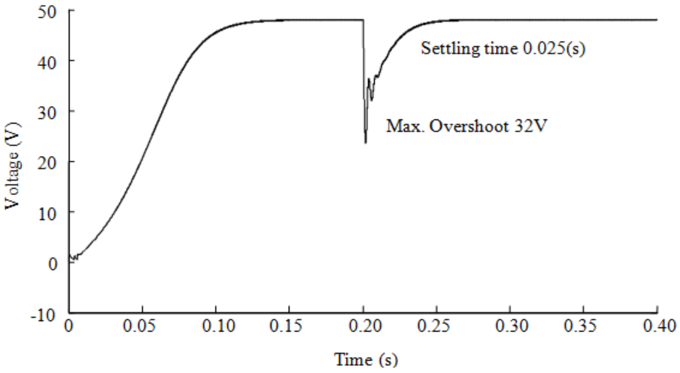

Fig. 9: Output voltage when input takes a step change from 16 to 10 V

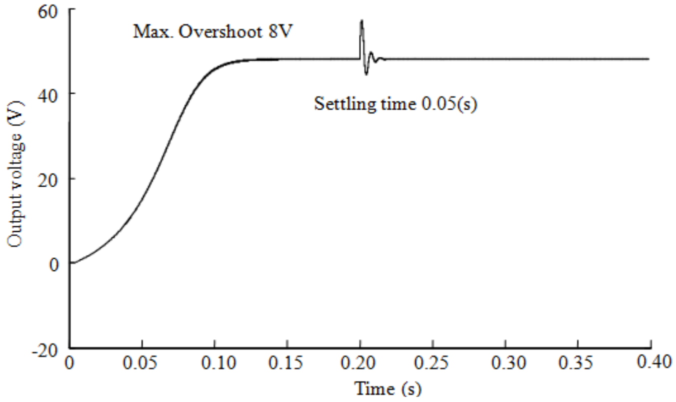

Fig. 10: Output voltage when load resistance makes a step changes from 50 to 60 Ω

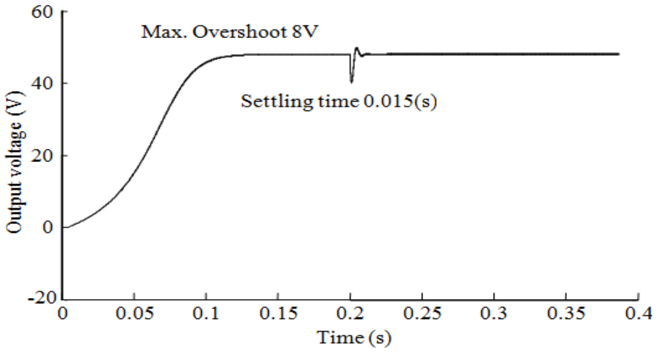

Fig. 11: Output voltage when load resistance makes a step changes from 50 to 40 Ω

It can be found that the converter output voltage and inductor current has a negligible overshoot and settled at time of 0.025 sec in this region with designed PI control.

Line variations: Figure 8 shows the variation of output voltage of PI control with SEPIC converter for the input voltage step change from 10 to 16 V (+27.5% line disturbance). It can be found that converter output voltage has a maximum overshoot of 32 V and 0.025 sec settling time with designed PI control. Figure 9 shows the output voltage variation for another input voltage step change from 16 to 10 V (-27.5% line disturbance). It can be seen that the converter output voltage has a maximum overshoot of 10 V and 0.025 sec settling time.

Load variations: Figure 10 shows the variation of output voltage with the step change in load from 60 to 40 Ω (-33.3% load disturbance). It could be seen that there is a small overshoot of 1.5 V and steady state is reached with a very less time 0.023 sec.

Figure 11 shows another variation of output voltage with step change in load from 60 to 40 Ω

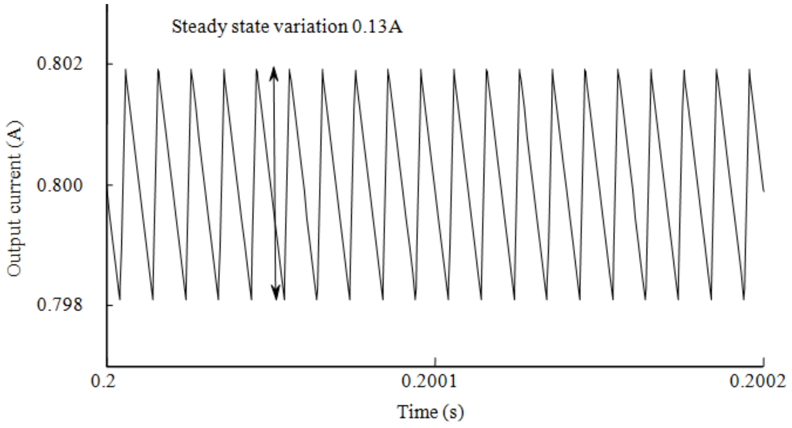

Fig. 12: Inductor current (iL1) in steady state region

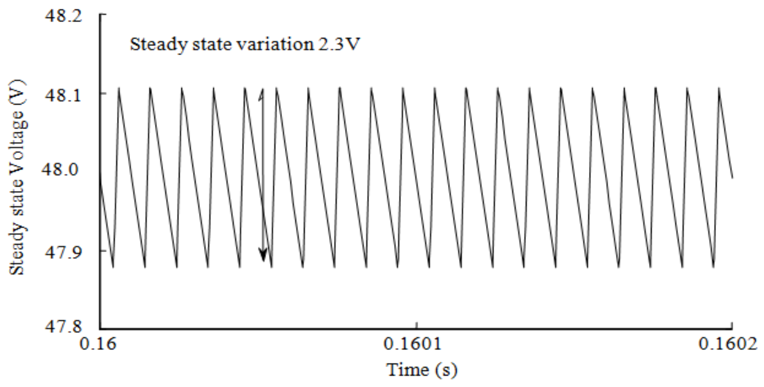

Fig.13: Output voltage (Vo) ripple at steady state region

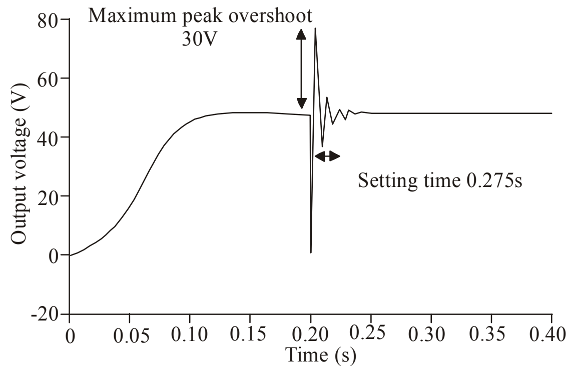

Fig. 14: Output voltage when capacitors variation from 30 to 100 µF

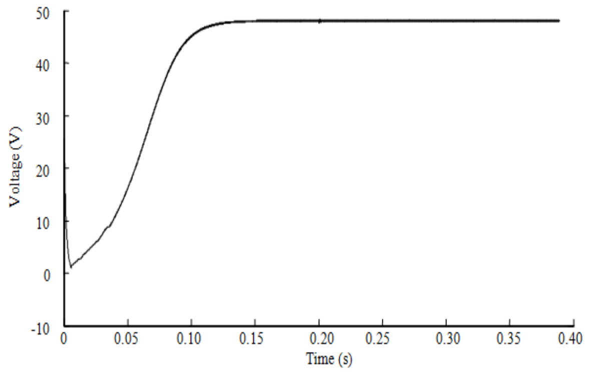

Fig. 15: Output voltage when inductor varies from 100 to 500 µH

(+33.3% load disturbance). It could be seen that there is a small overshoot of 0.5 V and steady state is reached with a very small time 0.015 sec.

Steady state region: Figure 12 and 13 show the instantaneous output voltage and current of the inductor current in the steady state. It is evident from the figure that the output voltage ripple is very small about 2.3 V and the peak to peak inductor current is 0.13 A while the switching frequency is 100 kHz.

Circuit components variations: An interesting result has been illustrated in Fig. 14, which shows response for the variation in capacitor values 30 to 100 µF. The PI control is very successful in suppressing effect of capacitance variation effect that a minute output ripple voltage. The capacitor change has no severe effect on the value of output voltage. Figure 15 shows the output voltage for inductor variation from 100 to 500 µH and the change has no severe effect on the converter behavior due to the efficient developed PI control.

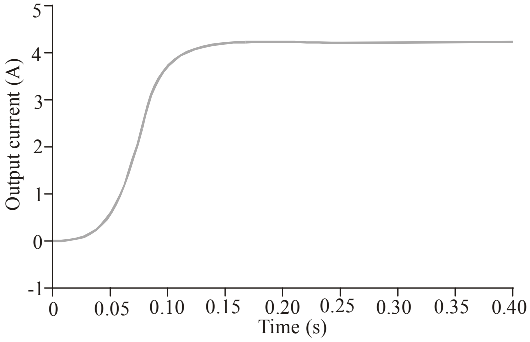

Fig. 16: Input current of SEPIC converter

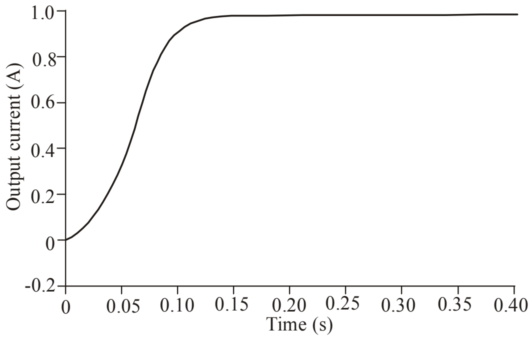

Fig. 17: Input current of SEPIC converter

Figure 16 and 17 show the average input current and average output current respectively. It is showed that the average input current is 4.2307 A and average output current is 0.9625 A which is closer to theoretical value. Using simulation analysis computes that the input and output power values are 50.76 and 46.442 W, respectively, which is closer to the calculated theoretical value. The efficiency is found that 96.41%.

CONCLUSION

The SEPIC performs the voltage conversion from positive source voltage to positive load voltage. Due to the time variations and switching nature of the power converters, their dynamic behavior becomes highly non-linear. This study has successfully demonstrated the design, analysis and suitability of PI controlled SEPIC converter. The simulation based performance analysis of a PI controlled SEPIC converter circuit has been presented along with its state space averaged model. The PI control scheme has proved to be robust and its triumph has been validated with transient region, line and load regulations, steady state region and also with circuit components variations. The SEPIC converter with PI control thus claims its use in applications such as computer peripheral equipment, switch mode power supply, medical equipments and industrial applications, especially for high voltage projects etc.

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