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Research Article

Design of a Novel Optimized MAC Unit using Modified Fault Tolerant Vedic Multiplier

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Abstract: In this study, the design of optimized Multiplication and Accumulation (MAC) unit with modified Vedic multiplier is presented. To design a MAC unit, efficient multiplier is used to increase speed and to reduce area and power. Conventional MAC is designed using without fault tolerant Vedic multiplier. But it consumes more area and power. And also less delay. So MAC unit is changed to design the efficient Vedic multiplier. Conventional MAC unit with regular Vedic multiplier is not working for some of the inputs condition. To overcome this fault, novel Vedic multiplier is proposed and designed using less half adder and Full Adder. Simulation is carried out using Modelsim 6.3c. Synthesis and Implementation is carried out using Xilinx and FPGA Spartan 3.

Keywords: Fault tolerant multiplier, FPGA spartan 3, MAC, vedic multiplier

INTRODUCTION

MAC unit is used in ALU block. As all of us know that the Computation unit is main unit of any technology (Cieplucha, 2013), which performs different arithmetic operations like as addition, subtraction and multiplication etc., also in some places it performs logical operations also like as AND, OR, INVERT, X-OR etc. which is dominant feature in the digital domain based applications (Deepak and Kailath, 2012). ALU is the execution unit which does not only perform Arithmetic operations but also logical operations. And that's why ALU is called as the heart of Microprocessor, Microcontrollers and CPUs. No technology can exist, without those operations which are performed by ALU (Shams *et al*., 1998). Every technology uses works upon those operations either fully or partially which are performed by ALU.

The DSP functions extensively make use of the Multiply Accumulate operation, for high performance Digital signal processing system (Itawadiya *et al*., 2013). A basic MAC architecture consist of a Multiplier and an accumulate adder organized as in Fig. 1. MAC unit compute the product of two numbers and adds the product to an accumulator register (Jaina *et al*., 2011). The output of register is fed back to one input of the adder as shown in Fig. 1 (Shanthala *et al*., 2009).

DESIGN OF MAC UNIT USING CONVENTIONAL VEDIC MULTIPLIER

Vedic multiplier can propose using different algorithm. In this study Urdhava-Tiryakbhyam algorithm is used to design the Vedic multiplier (Bansal *et al*., 2014). Urdhava-Tiryakbhyam is the common formula applicable to all cases of multiplication and also in the division of a huge number by another huge number. It means perpendicularly and diagonally (Huddar *et al*., 2013) (Fig. 2).

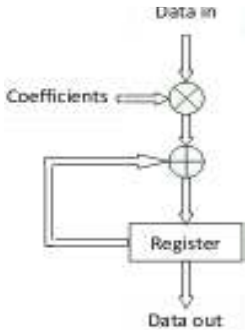

Fig. 1: Architecture of MAC unit

Conventional Vedic multiplier is constructed using Ripple Carry Adder (RCA). RCA consist of number of full adders and half adders. Conventional Vedic multiplier is not working properly, when the carry input has more than one number of ones. So it will be generate fault output, when the carry input consist of more number of one's (Kunchigi *et al*., 2012).

Proposed MAC unit using modified vedic multiplier: In this research study, Modified Vedic multiplier is proposed to reduce the total number of half adder and full adder in order to rectify the fault, when the carry is 1. From the conventional Vedic multiplier,

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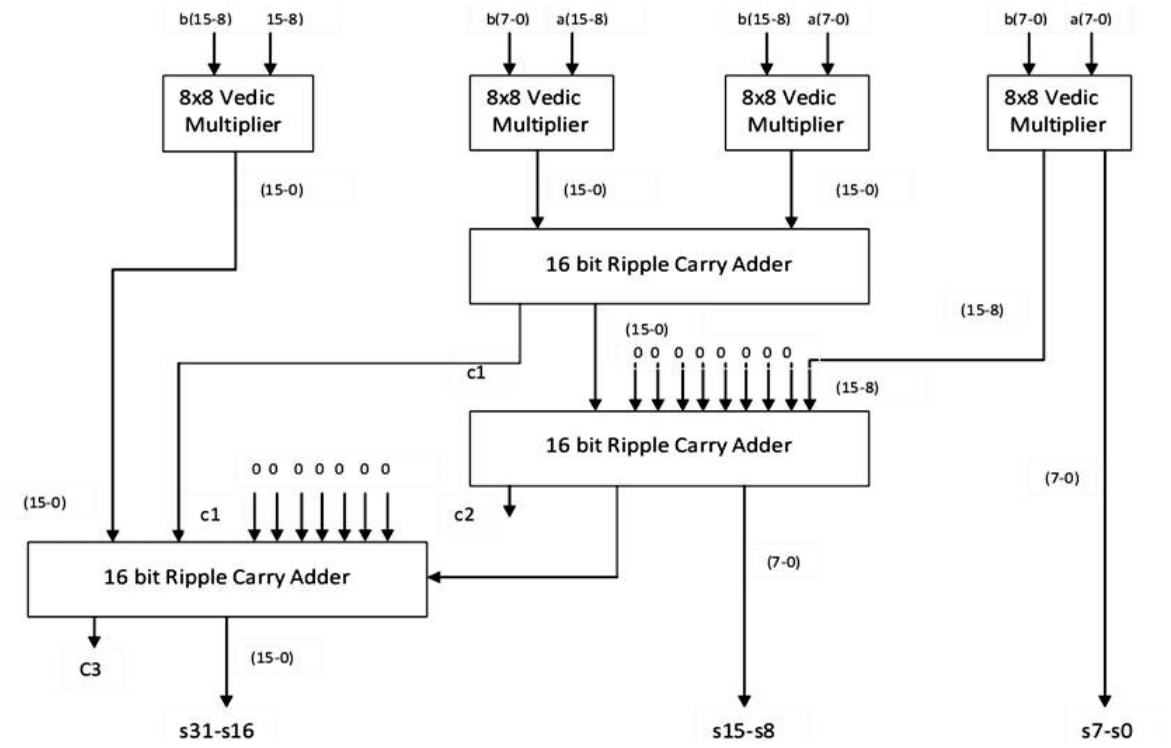


Fig. 2: Block diagram of conventional vedic multiplier for existing MAC unit

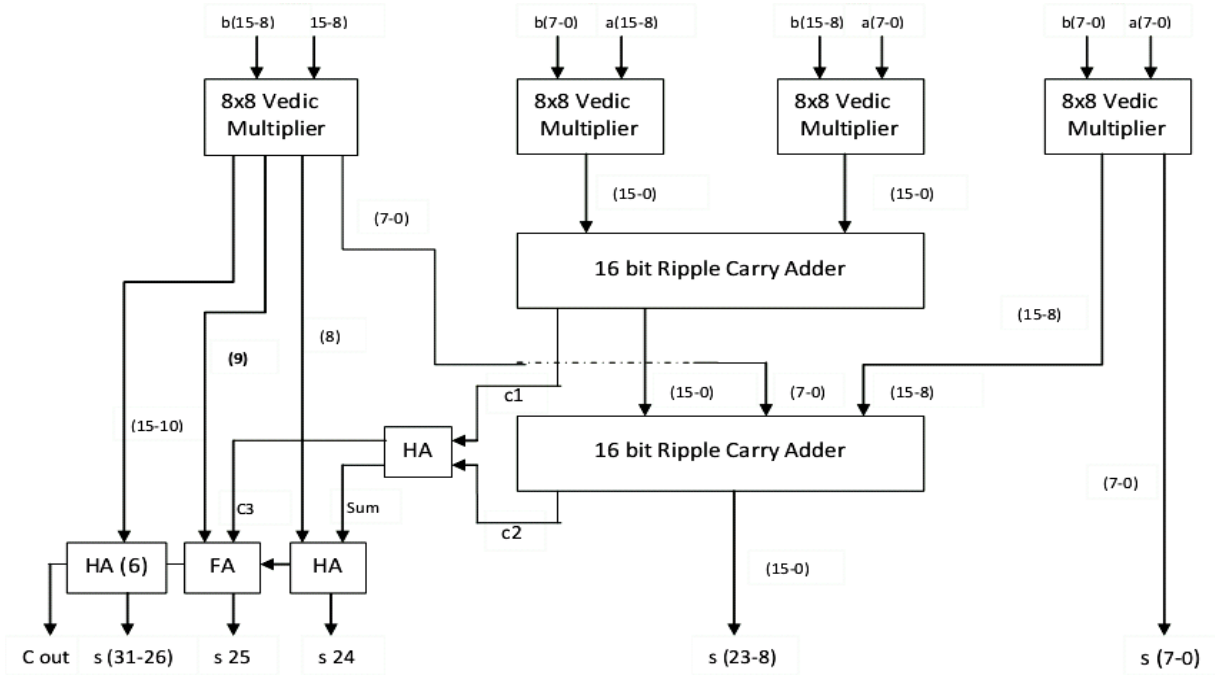


Fig. 3: Block diagram of modified vedic multiplier for proposed MAC unit

2nd and 3rd Ripple Carry Adder (RCA) block is changed in order to reduce the number of half adders and full adders. Modified Vedic multiplier is applied into the proposed MAC unit (Fig. 3).

MAC design with modified Vedic multiplier offers low area, delay and power compared to conventional MAC design with regular Vedic multiplier. Simulation results are illustrated as shown in the Fig. 4 and 5. Synthesis is performed to analyze the area, delay and power. Power can be evaluated using X-power analyzer. Synthesis results are given in the Fig. 6 to 8.

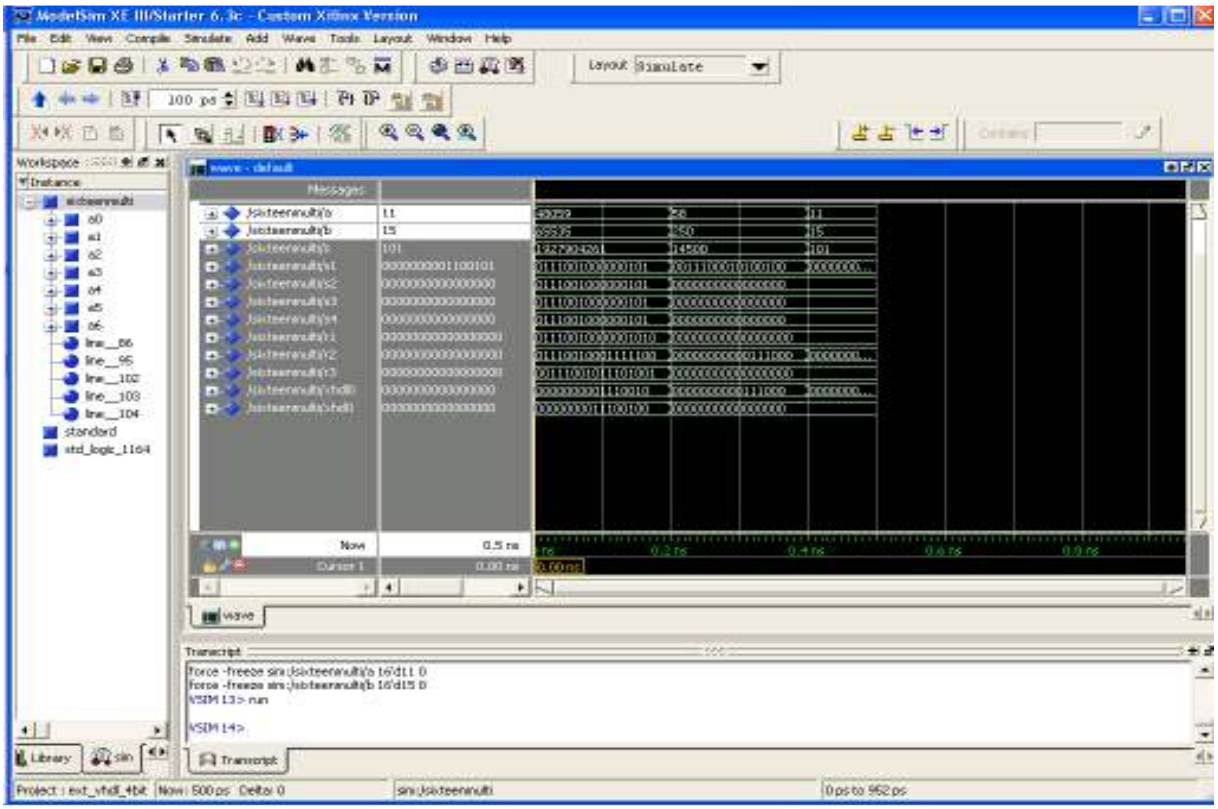


Fig. 4: Simulation result of conventional vedic multiplier with fault during carry = 1

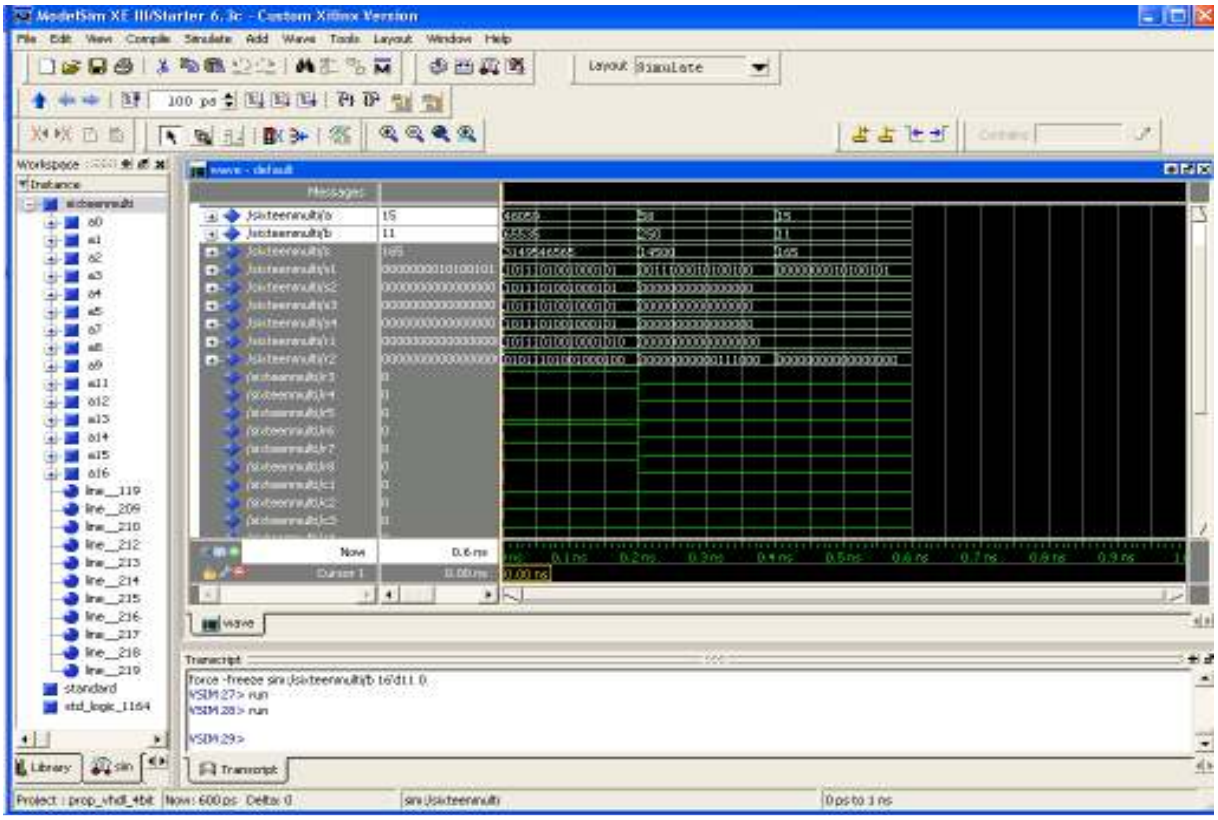
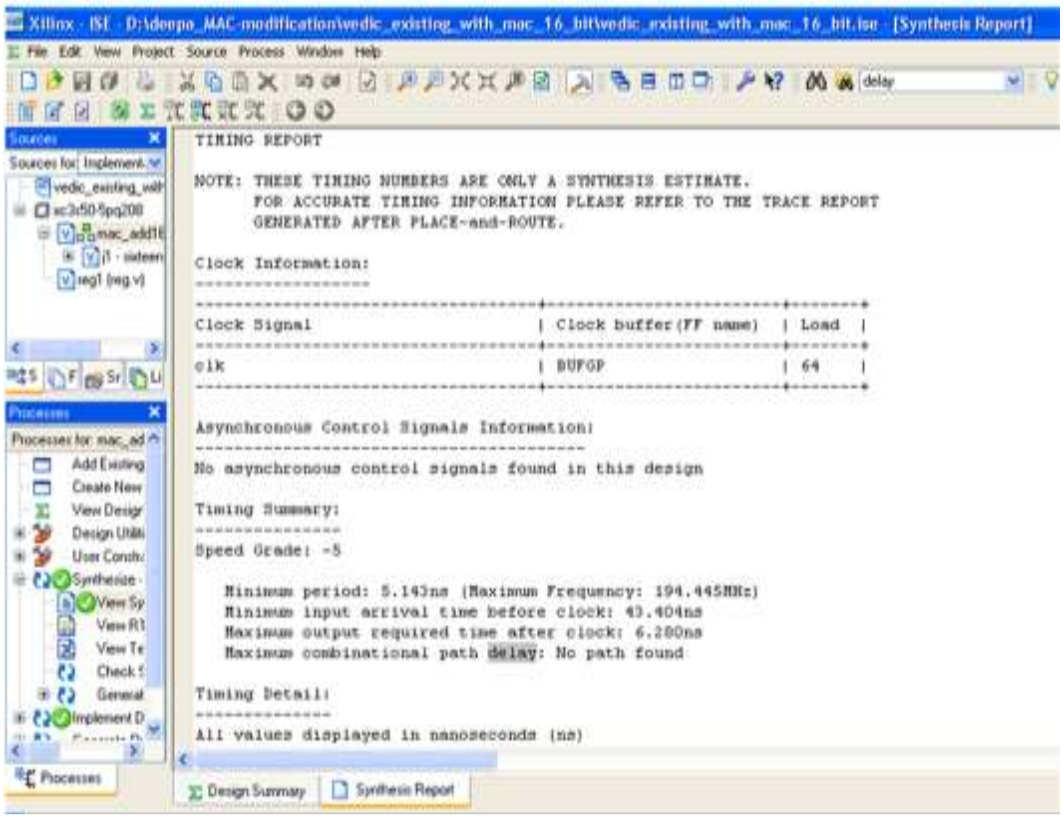
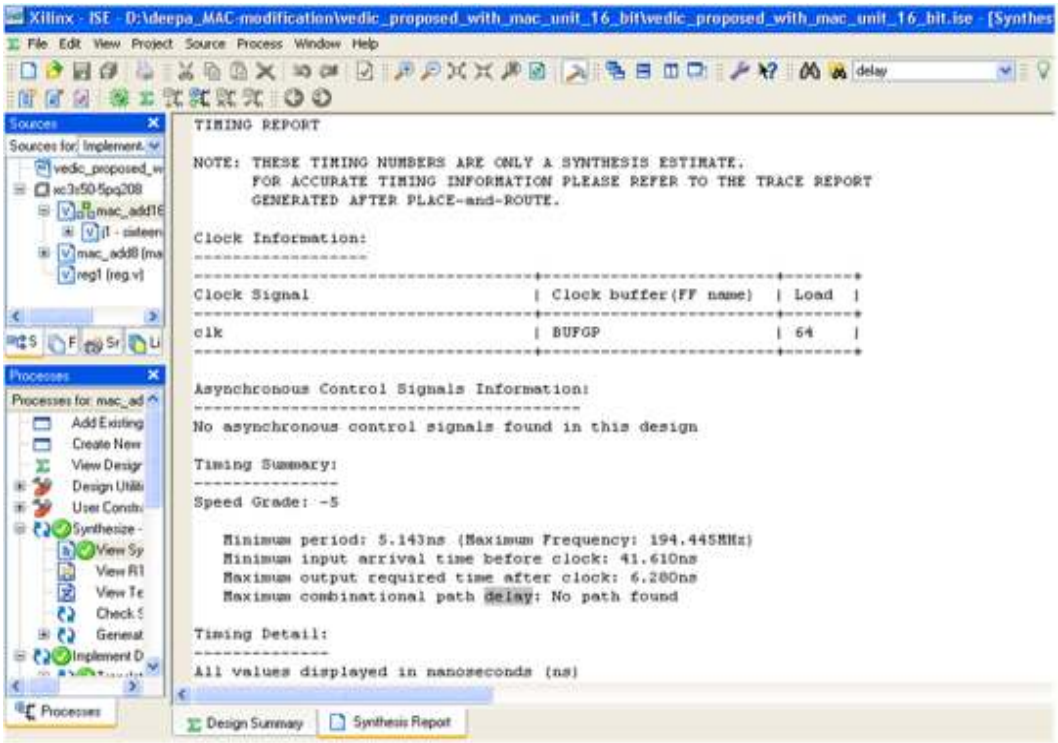


Fig. 5: Simulation result of proposed vedic multiplier without fault during carry = 1

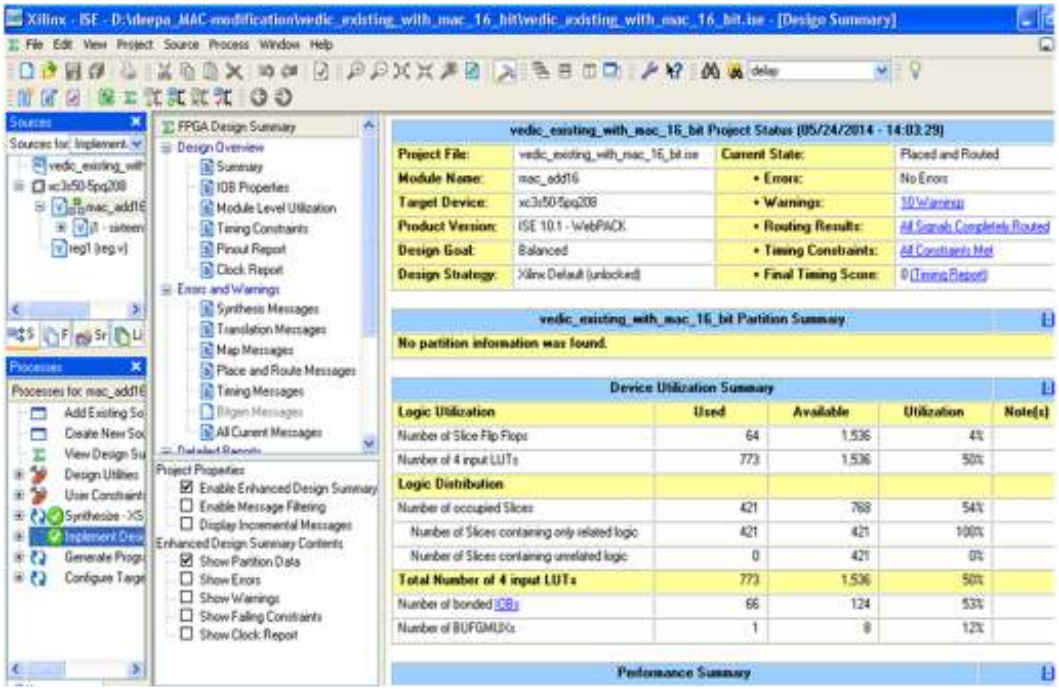


(a) Delay of conventional MAC unit with regular vedic multiplier

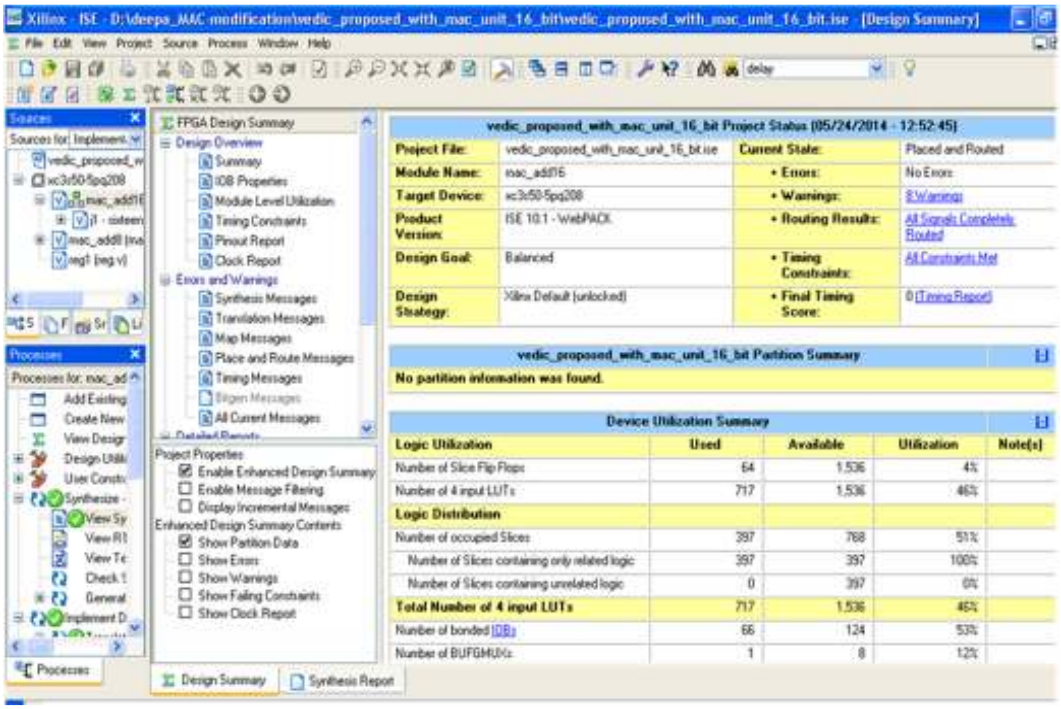


(b) Delay of proposed MAC unit using modified vedic multiplier

Fig. 6: Synthesis result of conventional and modified MAC unit for delay utilization



(a) Area of conventional MAC unit with regular vedic multiplier



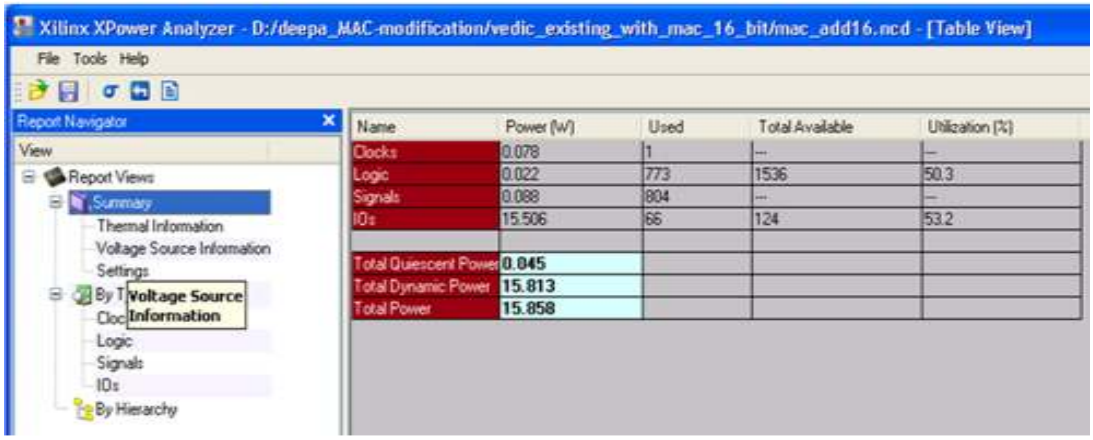
(b) Area of proposed MAC unit using modified vedic multiplier

Fig. 7: Synthesis result of conventional and modified MAC unit for area utilization

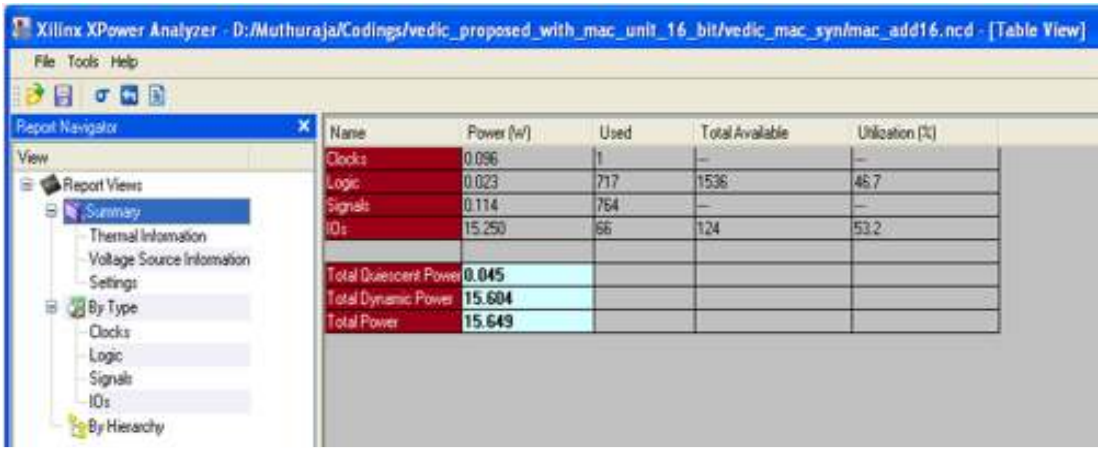
RESULTS AND DISCUSSION

Conventional Vedic multiplier, show the result in wrong, when 15×11, it give 105 instead of 165 due to carry output 1 is not processed. To overcome this fault, modified Vedic multiplier is proposed.

Simulation is done using Modelsim 6.3c. Simulation result of conventional Vedic multiplier is shown in below Fig. 4 and 5. Conventional MAC with



(a) Power utilization of existing MAC unit using regular vedic multiplier



(b) Power utilization of proposed MAC unit using modified vedic multiplier

Fig. 8: Synthesis result of conventional and modified MAC unit for power consumption

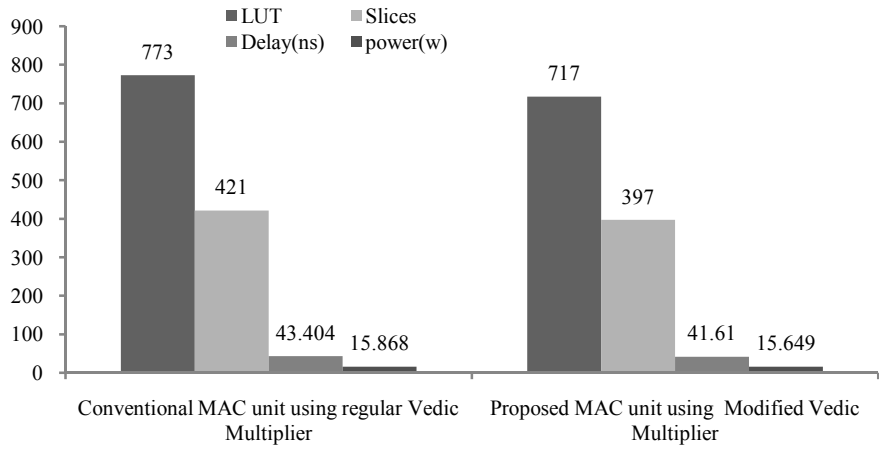


Fig. 9: Performance analysis of proposed modified MAC unit over existing MAC unit

Table 1: Comparison of different MAC unit using regular and modified vedic multipliers

Type	LUT	Slices	Delay (ns)	Power (w)
Conventional MAC unit using regular vedic multiplier	773	421	43.404	15.858
Proposed MAC unit using modified vedic multiplier	717	397	41.610	15.649

regular Vedic multiplier consists of 773 LUTs and proposed MAC with modified Vedic multiplier consists of 717 LUTs. Conventional MAC with regular Vedic multiplier consumes 15.858 w of power and proposed MAC with modified Vedic multiplier consumes 15.649 w of power. The number of occupied slices of existing MAC unit is 421 and of proposed MAC unit is 397 (Fig. 9).

Modified Vedic multiplier is shown in Fig. 3. It is used give the exact result, when the carry output is 1. Instead of 16 bit ripple carry adder (32 half adder), 8 half adder and one full adder is used in modified Vedic multiplier to reduce the area and delay than the conventional Vedic multiplier. So 22 half adder is reduced in the modified full adder and also when 15×11, it gives 165. This fault also rectifies using half adders (Table 1).

CONCLUSION

An efficient multiplier called modified Vedic multiplier has been proposed for MAC unit. The proposed multiplier provides low area and less delay by use of less number of full adder and half adder instead of ripple carry adder. In this study, hardware design and implementation of Field Programmable Gate Array based Multiplication and Accumulation (MAC) unit with modified Vedic multipliers is presented. The design was implemented on Xilinx Spartan 3 XC3S50 FPGA device. Comparative study of an efficient MAC unit with regular Vedic multiplier and modified Vedic multiplier was done. The Modified Vedic multiplier as compared to regular Vedic shows much more reduction in device Utilization. The proposed method offers 10% area, 10% delay and 5% power reduction than the existing architecture. Hence it is concluded that, modified Vedic multiplier based MAC unit provides an efficient method for reducing the power dissipation, delay and area. In future, the proposed MAC unit can be used in the digital FIR filter.

REFERENCES

Bansal, Y., C. Madhu and P. Kaur, 2014. High speed Vedic multiplier designs-A review. Proceeding of 2014 Recent Advances in Engineering and Computational Sciences (RAECS), pp: 1-6.

Cieplucha, M., 2013. High performance FPGA-based implementation of a parallel multiplier-accumulator. Proceeding of 20th International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES), pp: 485-489.

Deepak, S. and B.J. Kailath, 2012. Optimized MAC unit design. Proceeding of IEEE International Conference on Electron Devices and Solid State Circuit (EDSSC, 2012), pp: 1-4.

Huddar, S.R., S.R. Rupanagudi, M. Kalpana and S. Mohan, 2013. Novel high speed Vedic mathematics multiplier using compressors. Proceeding of International on Multi-Conference Automation, Computing, Communication, Control and Compressed Sensing (iMac4s), pp: 465-469.

Itawadiya, A.K., R. Mahle, V. Patel and D. Kumar, 2013. Design a DSP operations using Vedic mathematics. Proceeding of International Conference on Communications and Signal Processing (ICCSP, 2013), pp: 897-902.

Jaina, D., K. Sethi and R. Panda, 2011. Vedic mathematics based multiply accumulate unit. Proceeding of International Conference on Computational Intelligence and Communication Networks (CICN, 2011), pp: 754-757.

Kunchigi, V., L. Kulkarni and S. Kulkarni, 2012. High speed and area efficient Vedic multiplier. Proceeding of International Conference on Devices, Circuits and Systems (ICDCS, 2012), pp: 360-364.

Shams, A.M., W.M. Badawy and M.A. Bayoumi, 1998. An enhanced low-power computational kernel for a pipelined multiplier-accumulator unit. Proceeding of the 10th International Conference on Microelectronics (ICM '98), pp: 33-36.

Shanthala, S., C.P. Raj and S.Y. Kulkarni, 2009. Design and VLSI implementation of pipelined multiply accumulate unit. Proceeding of 2nd International Conference on Emerging Trends in Engineering and Technology (ICETET, 2009), pp: 381-386.